XE8-class M8050A 120 GBd High-Performance Bit Error Ratio Tester (BERT)

High-speed receiver characterization for error-free data transmission enabling your successful design deployments in 800G/1.6T Ethernet, OIF-CEI, PCIe, DisplayPort, and USB 3.2/4

Datasheet — Version 6.0

New features

- Added 1.6T Ethernet KP4 FEC encoding on M8042A pattern generator (8x200GE based on IEEE 802.3dj)
- Added USB 3.2 ×2 LTSSM support on M8042A pattern generator
- Added automatic de-emphasis optimization support using Keysight N1093A/B DCA-M
- Added DUT Control Interface (DCI) script examples for Keysight 1.6T functional BERTs such as Functional Interconnect Test Solutions FITS-8CH used as an error detector
- Extended maximum symbol rate for Keysight UXR used as an error detector up to 224 GBd

Introduction

The Keysight M8050A BERT enables success in high-speed SerDes chips and device deployments of 800G/1.6T Ethernet, OIF-CEI-112G/224G, PCIe, USB 3.2/4, and other leading technologies by providing an unmatched combination of 120 GBd signaling with uncompromised signal integrity.

KEYSIGHT

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List of Acronyms

Acronym	Full Name / Description
AC	Alternating Current
API	Application Programming Interface
AXIe	AdvancedTCA Extensions for Instrumentation (modular instrumentation platform)
AWG	Arbitrary Waveform Generator
BER	Bit Error Ratio
BERT	Bit Error Ratio Tester
BIST	Built-In Self-Test
BUJ	Bounded Uncorrelated Jitter
CDR	Clock Data Recovery
CTLE	Continuous-Time Linear Equalizer
DC	Direct Current
DCA	Digital Communications Analyzer (Keysight product name for sampling oscilloscopes)
DCI	DUT Control Interface
DFE	Decision Feedback Equalizer
DJ	Deterministic Jitter
DP	DisplayPort
DUT	Device Under Test
EMC	Electromagnetic Compatibility
FEC	Forward Error Correction
FFE	Feed-Forward Equalizer
FBER	First Bit Error Ratio (specific PCIe 6.x compliance metric defined by the PCI-SIG)
FIR	Finite Impulse Response
GAUI	Gigabit Attachment Unit Interface
GSa/s	Giga-Samples per Second
GUI	Graphical User Interface
HF-PJ	High-Frequency Periodic Jitter
IEEE	Institute of Electrical and Electronics Engineers
IoT	Internet of Things
ISI	Intersymbol Interference
ITOL	Interference Tolerance
JTOL	Jitter Tolerance
KP4	Reed-Solomon Forward Error Correction (RS-FEC) for 4-lane PAM4 Ethernet
LAN	Local Area Network
LF-PJ / LFPJ	Low-Frequency Periodic Jitter
LFPS	Low-Frequency Periodic Signaling
mUI	milli-Unit Interval
NRZ	Non-Return-to-Zero
OIF-CEI	Optical Internetworking Forum – Common Electrical I/O
PAM3/4/6/8	Pulse Amplitude Modulation (3/4/6/8 levels)
PCS	Physical Coding Sublayer

PCIe	Peripheral Component Interconnect Express
PLL	Phase-Locked Loop
ppm	parts per million
PRBS	Pseudo-Random Bit Sequence
PRTS	Pseudo-Random Ternary Sequence
Q-factor	Quality Factor
QPRBS	Quaternary Pseudo-Random Bit Sequence
RJ	Random Jitter
RMS	Root Mean Square
RS	Reed-Solomon
sRJ	Spectrally Distributed Random Jitter
SCPI	Standard Commands for Programmable Instruments
SER	Symbol Error Ratio
SNDR	Signal-to-Noise and Distortion Ratio
SSC	Spread Spectrum Clocking
TxEQ	Transmitter Equalization
UI	Unit Interval
USB	Universal Serial Bus
UXR	Ultra-High-Bandwidth Real-Time Oscilloscopes (Keysight product name)
Vpp	Peak-to-Peak Voltage
XML	eXtensible Markup Language

Introduction

The Keysight M8050A high-performance bit error ratio tester (BERT) platform enables accurate characterization of high-speed digital receivers used in next generation data center networks and server interfaces with symbol rates up to 120 GBd.

The M8050A high-performance BERT is part of the **Keysight M8000 Series of BER test solutions**. It can be combined with other hardware and software of the M8000 Series including modules from the M8040A platform such as the M8045A, M8046A, and M8054A modules.

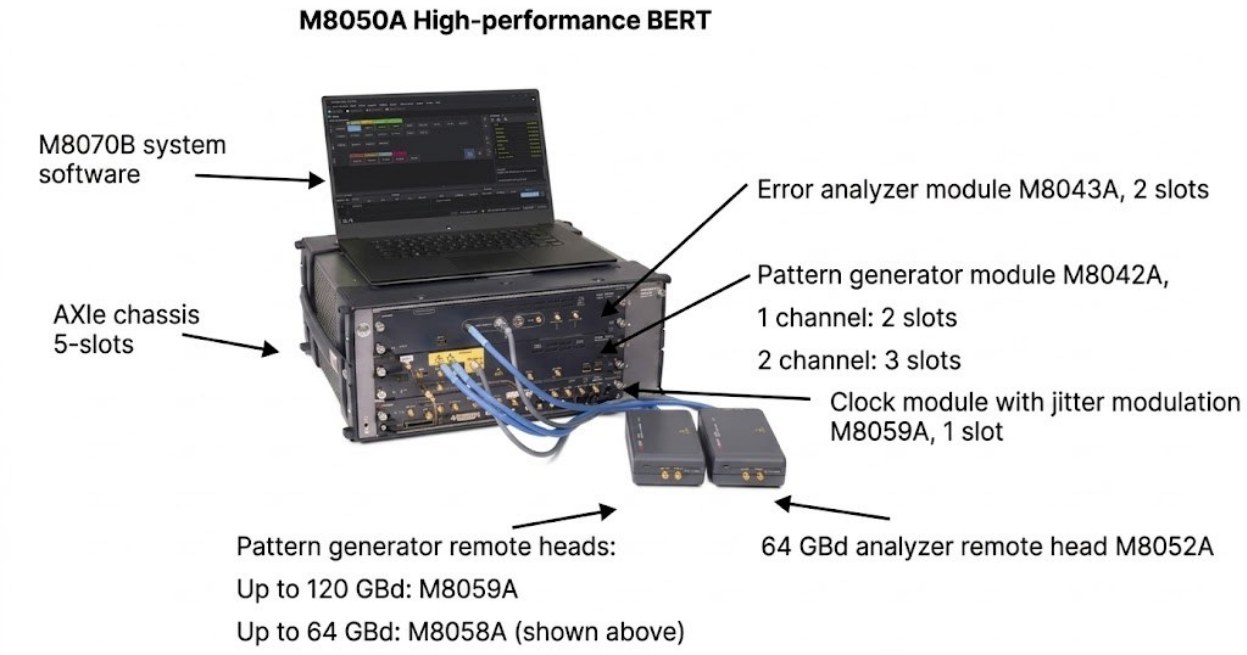


Figure 1. Overview of the M8050A high-performance BERT system example.

The following table shows M8050A modules and remote heads covered in this data sheet:

Description	AXIe slots	Product number
120 GBd pattern generator module with one data output channel	2-slot	M8042A-0G1
120 GBd pattern generator module with two data output channels	3-slot	M8042A-0G2
64 GBd remote head with cable connection to M8042A pattern generator module	–	M8058A
120 GBd remote head with cable connection to M8042A pattern generator module	–	M8059A
64 GBd high-voltage remote head with cable connection to M8042A pattern generator module	–	M8068A
120 GBd high-voltage remote head with cable connection to M8042A pattern generator module	–	M8069A
64 GBd error analyzer module	2-slot	M8043A
64 GBd remote head with cable connection to M8043A error analyzer module	–	M8052A

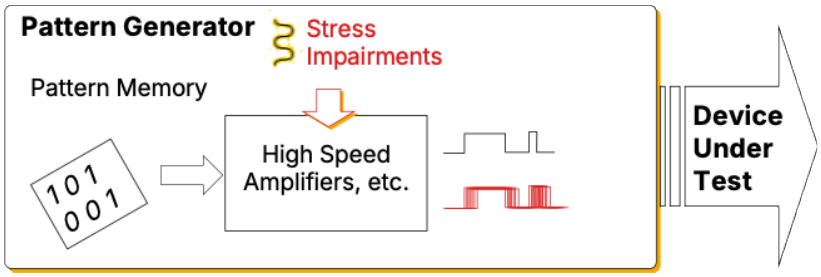
Part 1. Pattern Generation

Pattern generation (PG) provides a known and deterministic sequence of digital symbols that is transmitted into the device under test (DUT).

In bit error ratio (BER) testing, this known pattern serves as the reference against which the received data is compared. By supporting stress, long enough patterns such as PRBS, protocol-defined sequences, and custom user patterns, pattern generation enables realistic emulation of high-speed serial links and controlled excitation of the DUT across different operating conditions.

Precise timing, modulation, calibrated stress impairments, and signal control at the pattern generator are essential to ensure that measured errors reflect true DUT behavior rather than stimulus uncertainty.

Pattern generation involves creating a known sequence of digital bits transmit through a device under test. It is essential for bit error ratio testing as it provides a consistent and repeatable signal for measuring the device's performance.



Specifications of M8042A Pattern Generator Module with M8058A, M8059A, M8068A, and M8069A Remote Heads

Overview

The M8042A pattern generator module supports symbol rates from 2 to 120 GBd and is available in one-channel or two-channel configurations. Three symbol-rate ranges can be selected: up to 32 GBd, up to 64 GBd, and up to 120 GBd. The M8042A requires an M8009A clock module with jitter modulation capabilities and one remote head per data output channel. For operation above 64 GBd, a 120 GBd pattern generator remote head (M8059A or M8069A) is required.

Direct use of the P and N outputs of the M8042A without a connected remote head is not permitted. One M8009A clock generator module is required for each M8042A module.

Figure 2. The pattern generator module M8042A is available as a one-channel or a two-channel version. The one-channel version M8042A-0G1 occupies 2 slots in the AXIe chassis, and the two-channel version M8042A-0G2 occupies 3 slots.

The following options are required to enable the corresponding pattern-generator functions:

- **M8042A-G32** – Pattern generation up to **32 GBd** for **NRZ and PAM4**, default configuration
- **M8042A-G64** – Pattern generation up to **64 GBd** for **NRZ and PAM4**, module-wide license
- **M8042A-G12** – Pattern generation up to **120 GBd** for **NRZ and PAM4**, module-wide license
- **M8042A-0G1** – **One-channel** operation, default configuration
- **M8042A-0G2** – **Two-channel** operation, optional hardware configuration
- **M8042A-0G4** – **De-emphasis**, module-wide license
- **M8042A-0P3** – **PAM3** line encoding, required for USB4v2 interfaces, module-wide license
- **M8042A-0P6** – **PAM6** line encoding, module-wide license
- **M8042A-0P8** – **PAM8** line encoding, module-wide license
- **M8042A-0G9** – **FEC** encoding, module-wide license

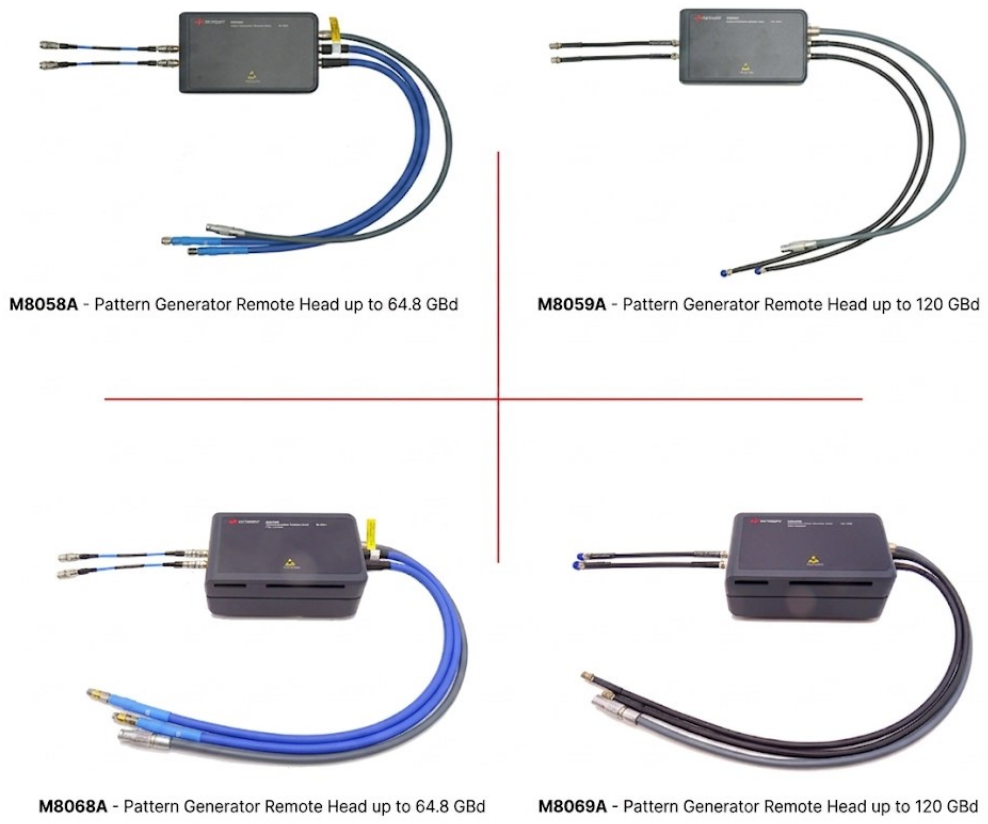


Figure 3. Four remote heads are available for the pattern generator module M8042A. On the right, the 120 GBd remote heads M8059A and M8069A are shown with 1.00 mm connectors to accommodate close connection to the device under test for symbol rates up to 120 GBd. The 64 GBd remote heads M8058A and M8068A are shown on the left, and these provide 1.85 mm connectors. The three cables on the back side of all remote heads are used to connect with the M8042A pattern generator module and are not removable.

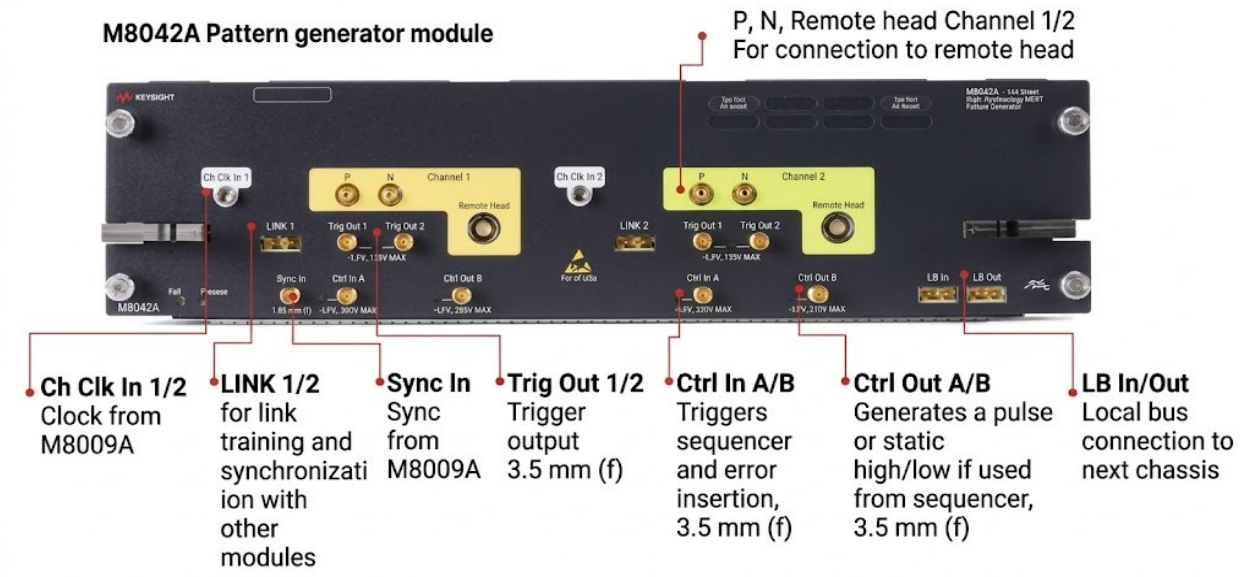


Figure 4. The M8042A pattern generator module provides many supplementary inputs and outputs. Shown here is the overview of all inputs and outputs for a two-channel version of the M8042A.

Data Output 1/2 (Data Out 1, Data Out 2)

Table 1. Data output characteristics for M8042A with M8058A/M8059A and high-voltage remote heads M8068A/M8069A. Values apply at the end of the reference cable at the outputs of the remote heads.

Parameter	Value (with M8059A / M8058A remote heads)	Value (with M8069A / M8068A high-voltage remote heads)
Symbol rate (applies for NRZ and PAM4)	2.0 to 120.0 GBd for M8042A-G12 (only with M8059A or M8069A) 2.0 to 64.8 GBd for M8042A-G64 2.0 to 32.4 GBd for M8042-G32	
Data formats	NRZ, PAM4 standard. PAM3 (requires M8042A-0P3/UP3). PAM6 (requires M8042A-0P6/UP6). The maximum supported symbol rate is 96 GBd, over-programming is possible. PAM8 (requires M8042A-0P8/UP8). The maximum supported symbol rate is 80 GBd, over-programming is possible.	
Channels per module	1 channel, 2 AXIe slots (option M8042A-0G1) 2 channels, 3 AXIe slots (option M8042A-0G2)	
Amplitude	**M8059A:** 100 mVpp to 1.6 Vpp differential 50 mVpp to 0.8 Vpp single-ended	**M8069A:** 1 Vpp to 3.6 Vpp up to 113.5 GBd differential 500 mVpp to 1.8 Vpp up to 113.5 GBd single-ended 1 Vpp to 3.4 Vpp from >113.5 to 116 GBd differential 500 mVpp to 1.7 Vpp from > 113.5 to 116 GBd single-ended
	M8058A: 100 mVpp to 1.8 Vpp differential 50 mVpp to 0.9 Vpp single-ended	**M8068A:** 1 Vpp to 5 Vpp differential 500 mVpp to 2.5 Vpp single-ended
Amplitude resolution	1 mV	3 mV
Amplitude accuracy	±10% ±10 mV typical (AC) [1]	±10% ±30 mV typical (AC) [1]
Symbol level resolution	PAM levels are adjustable in 0.1% steps of amplitude	
Coupling	DC/AC-coupled (selectable)	AC-coupled only
Output voltage window	–1 to +3.0 V depends on external termination voltage [2]	Not applicable
Common mode voltage accuracy	25 mV ± 12.5% [5]	Not applicable
External termination voltage	–1 to +3.0 V	
Termination modes	Balanced and unbalanced	Not applicable
Termination impedance range	To protect the output stage, the output is disabled when an unexpected voltage or termination impedance is detected. **DC-coupled mode:** Termination range for devices connected to data out: Unbalanced 50 Ω +15 Ω / –10 Ω Typical balanced 100 Ω ±30 Ω typical Operation into open is possible for following ranges when DC-coupled and	50 Ω +15 Ω / –10 Ω

Parameter	Value (with M8059A / M8058A remote heads)	Value (with M8069A / M8068A high-voltage remote heads)
	balanced termination modes are selected and M8042A module driver Output amplitude max. 450 mV Offset 0 to 370 mV	
Transition time (20% to 80%)	**M8059A:** 4 ps typical at 120 GBd 6.5 ps typical at 64 GBd 8 ps typical at 8 GBd	**M8069A:** 4.5 ps typical at 120 GBd 7.5 ps typical at 64 GBd 11 ps typical at 8 GBd
	M8058A: 7 ps typical at 64 GBd 8.5 ps typical at 8 GBd	**M8068A:** 6.5 ps typical at 64 GBd 9 ps typical at 32 GBd 10 ps typical at 8 GBd
Intrinsic total jitter [6]	**For M8009A with option -062:** 3.3 ps typical 6 ps typical for symbol rates from 2 to 20 GBd **For M8009A with option -061:** 3.3 ps typical in combination with M8009A-061 7 ps typical for symbol rates from 70 to 80 GBd 6 ps typical for symbol rates from 16 to 33 GBd 7 ps typical for symbol rates from 10 to 16 GBd 9 ps typical for symbol rates from 2 to 10 GBd	
Intrinsic random jitter [6] (NRZ)	**For M8009A with option -062:** 6 mUI rms typical for symbol rates from 2 to 40 GBd 7 mUI rms typical for symbol rates from 40 to 64.5 GBd 10 mUI rms typical for symbol rates from 64.5 to 110 GBd 12 mUI rms typical for symbol rates from 110 to 120 GBd	
	For M8009A with option -061: 10 mUI rms typical 15 mUI rms typical for symbol rates from 105 to 120 GBd 20 mUI rms typical for symbol rates from 99 to <105 GBd 40 mUI rms typical for symbol rates from 70 to 80 GBd 15 mUI rms typical for symbol rates from 30 to 33 GBd 7 mUI rms typical for symbol rates from 24 to 30 GBd	
Clock/2 jitter range	±50 mUI or ±4 ps typical (whatever is less) for symbol rates above 7.9 GBd. Note: this means that first eye can be up to 50 mUI or 4 ps longer or shorter than subsequent eye.	
Adjustable clock/2	For each channel independently	
SNDR with randomizer [3] off	**M8059A:** 53.125 GBd: 37 dB typical 106.25 GBd: 31 dB typical	**M8069A:** 53.125 GBd: 36 dB typical 106.25 GBd: 30 dB typical
	M8058A: 53 to 58 GBd: 37 dB typical	**M8068A:** 53 to 58 GBd: 37 dB typical
Level random noise	**M8059A:** 53.125 GBd: 4.75 mV rms differential typical 106.25 GBd: 6 mV rms differential typical	**M8069A:** 53.125 GBd: 14 mV rms differential typical 106.25 GBd: 20 mV rms differential typical

Parameter	Value (with M8059A / M8058A remote heads)	Value (with M8069A / M8068A high-voltage remote heads)
	M8058A: 53 to 58 GBd 5.5 mV rms differential typical	**M8068A:** 53 to 58 GBd: 16 mV rms differential typical
Data delay	Delay range 100 ns Delay accuracy: ± (maximum (1.5 ps or 25 mUI whatever is higher) + 1% of entered value) typical	
Skew between normal and complement	2 ps maximum at the end of the reference cable pair. Fixed. 1 ps maximum at connector of remote head Reference cable pairs M8059A-801 and M8058A-801 have 1 ps of skew	
Skew between data output 1 and 2 in one M8042A module	Repeatability: < 1 ps typical Absolute skew: < 10 ps measured	
Skew between data outputs of two M8042A modules	Repeatability: < 15 ps typical Absolute skew: < 15 ps measured	
Electrical idle (squelch)	The output transitions from full swing to 0 V amplitude and vice versa at constant offset within 1 UI. Normal and complement output have same level (Max – Min)/2.	
Squelch granularity	Pattern Editor (NRZ only): bit granularity When controlled from sequencer: sequencer block wise	
Automatic eye performance (de-emphasis) optimization by using an external oscilloscope	Yes, it requires the M8070ADVB plugin and an external Keysight DCA sampling oscilloscope (refer to the Automatic De-emphasis Optimization section).	
Connector type at data outputs of M8042A	1.00 mm, female	
Connector type at data outputs of remote head	**M8059A, M8069A:** 1.00 mm, female	**M8058A, M8068A:** 1.85 mm, female
Reference cables	**M8059A:** Matched cable pair 1.00 mm (m) to 1.00 mm (m), 150 mm length, 1 ps skew: M8059A-801 (also orderable as M8059-61621)	**M8069A:** Matched cable pair 1.00 mm (m) to 1.00 mm (m), 150 mm length, 1 ps skew: M8059A-801 (also orderable as M8059-61621)
	M8058A: Matched cable pair 1.85 mm (m) to 1.85 mm (m), 150 mm length, 1 ps skew: M8058A-801 (also orderable as M8199-61610)	**M8068A:** Matched cable pair 1.85 mm (m) to 1.85 mm (m), 150 mm length, 1 ps skew: M8058A-801 (also orderable as M8199-61610).
Recommended attenuators	Not applicable	In case you need to protect inputs of an oscilloscope, e.g. DCA module N1046A **For M8069A**: 10 dB attenuator with 1.00 mm connectors: 0955-4009. **For M8068A:** 10 dB attenuator with 1.85 mm connectors: 8490G.
Pre-requisites	Not applicable	M8042A module driver 4.5 or higher.

1. At 5 GBd measured with DCA-X N1046A and clock pattern and in the middle of the eye.
2. High level voltage range= 2/3* Vterm - 0.95 V < HIL < Vterm + 2 V. Low level voltage range= 2/3 * Vterm - 1 V < LOL < Vterm + 1.95 V.
3. Measurement procedure according to section 120D.3.1.6 of the IEEE 802.3 specification. The randomizer typically improves SNDR of for the M8059A and M8069A by 1 dB above 100 GBd. The randomizer is a scrambling process that

decorrelates data from hardware nonidealities, converting coherent, pattern-dependent distortion into broadband noise, which improves SNDR when the system is distortion-limited — especially at ultra-high symbol rates (>100 GBd).

4. Measured at 90% of maximum amplitude.
5. Common mode voltage = 0.5 * (measured offset at Normal + measured offset at Complement). Measured with the N1000A DCA with the N1046A module and a 10 dB attenuator.
6. Measured with the N1000A DCA with the N1060A module and PTB signal from RefClkOut 16G from M8009A, NRZ, PRBS15 @ BER 1e-12.

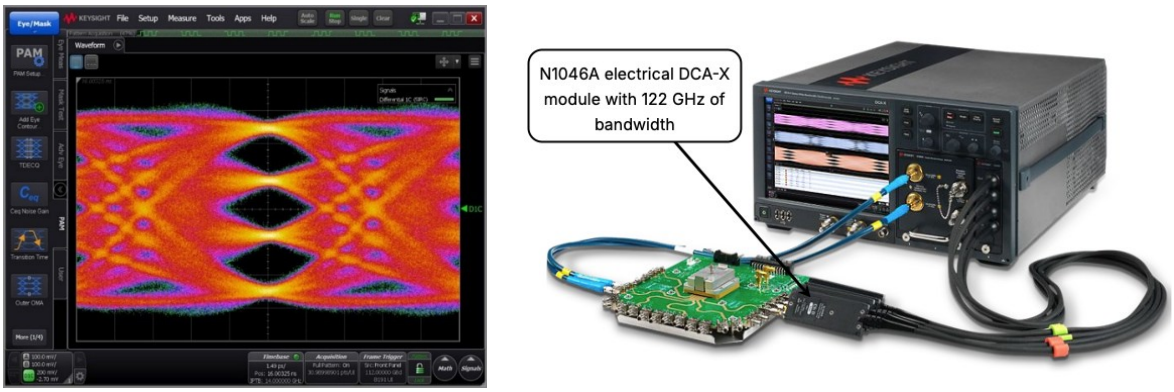


Figure 5. Clean 112 GBd PAM4 output signal of the M8042A pattern generator module with the M8059A 120 GBd remote head. Output amplitude is set to 1.0 Vpp differential and the pattern is PRBS 2^{15}-1. Measured with the DCA-X sampling oscilloscope N1000A with the N1046A electrical module.

De-emphasis

The M8042A high-performance pattern generator module provides built-in transmitter de-emphasis, enabling realistic signal conditioning directly at the pattern generator output. This capability allows users to compensate for channel loss and emulate transmitter behavior specified in high-speed serial standards without requiring external signal conditioning components.

The M8042A provides built-in de-emphasis with positive and negative cursors based on a Finite Impulse Response (FIR). Users can enter the de-emphasis in coefficient values.

Table 2. De-emphasis characteristics for M8042A. Requires Option -0G4.

De-emphasis	Range if used as cursor	Range if used as main cursor
De-emphasis taps	7, can be adjusted for each channel independently 1 UI spacing	
Preset table	50 presets editable in xml file	
Cursor (c0)	0.0 to ±0.45 [1]	
Cursor (c1)	0.0 to ±0.45 [1]	
Cursor (c2)	0.0 to ±0.45 [1]	0.3 to 1.0 [1]
Cursor (c3)	0.0 to ±0.45 [1]	0.3 to 1.0 [1]
Cursor (c4)	0.0 to ±0.45 [1]	0.3 to 1.0 [1]
Cursor (c5)	0.0 to ±0.45 [1]	
Cursor (c6)	0.0 to ±0.45 [1]	
Cursor coefficient resolution	0.004 Hardware capable resolution, user interface allows 0.001 steps	
Main cursor	Configurable position between c2 and c4	

1. Sum of all cursors absolute values may not exceed 1.0. Each absolute value of a cursor must be < than the value of the main cursor.

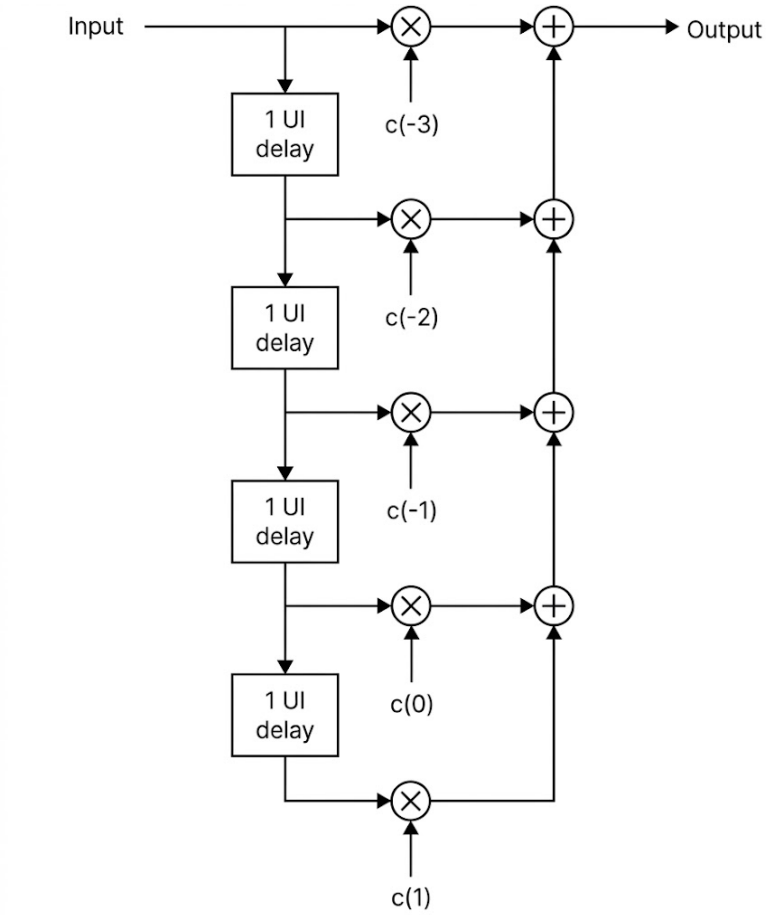


Figure 6. The pattern generator provides built-in de-emphasis to emulate a TX equalizer. The example shows a configuration for IEEE 802.3ck with three pre-cursors c(-3), c(-2), c(-1), the main cursor c(0), and one post cursor c(1).

Automatic De-emphasis Optimization

The Automatic De-emphasis Optimization feature (also referred to as “Auto De-emphasis”) optimizes the de-emphasis settings at the pattern generator output (remote head) to achieve optimal eye performance for NRZ or PAM4 signals. In addition, the feature supports cable and fixture de-embedding or embedding using imported S-parameter files.

To use this feature with the M8042A pattern generator module in combination with the M8058A, M8059A, M8068A, or M8069A remote head, the M8070ADVB Advanced Measurement Package plugin must be installed and licensed in the M8070B software.

One of the following DCA-X configurations is required:

- Keysight 86100D Infiniium DCA-X Wide-Bandwidth Oscilloscope equipped with the 86108B Precision Waveform Analyzer.
- Keysight N1000A DCA-X Wide-Bandwidth Oscilloscope Mainframe equipped with:
  - N1030A 65 GHz optical or one 65 GHz optical and one 95 GHz electrical channel module.
  - N1060A 50/85 GHz 64 GBd Precision Waveform Analyzer module.

    - N1046A 75/85/100 GHz, 1/2/4 Port, Electrical Remote Sampling Head module.
    - N1032A/B 90/120 GHz Single Channel Optical module.
- Keysight N1094A/B 2/4 Channel Electrical DCA-M Oscilloscope.
- Keysight N1092C DCA-M Sampling Oscilloscope (One Optical and Two Electrical Channels).
- Keysight N1092E DCA-M Sampling Oscilloscope (Two Optical and Two Electrical Channels).
- Keysight N1093A/B Single-Mode Optical DCA-M Sampling Oscilloscope.

For more details and how to set this configuration up, refer to the M8070ADVB Advanced Measurement Package User Guide.

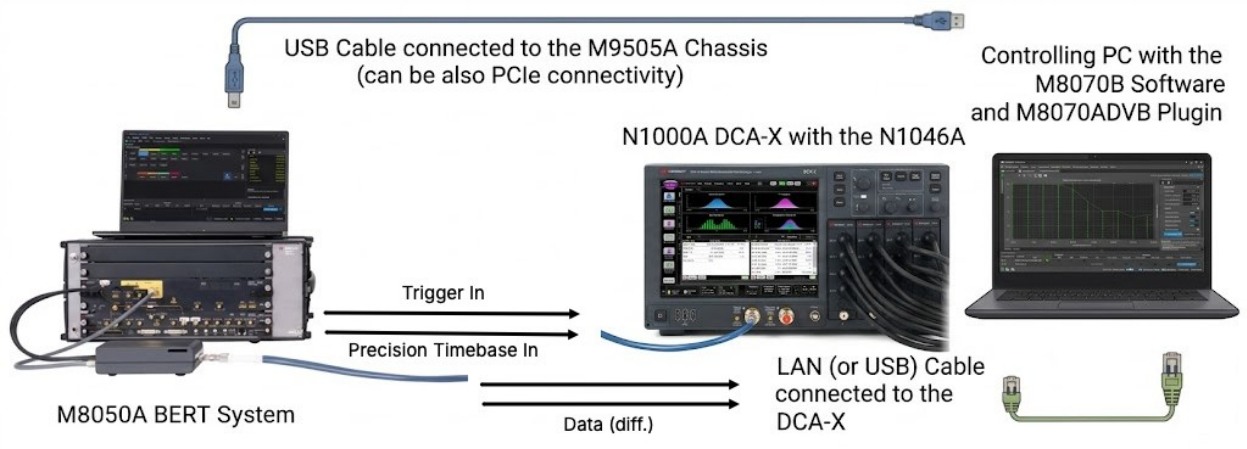


Figure 7. Principle connection diagram for automatic de-emphasis optimization using the M8042A pattern generator and N1000A DCA-X. Physical connections are simplified.

De-emphasis Presets for PCIe Testing

PCIe Tx equalization (TxEQ) de-emphasis presets are standardized transmitter-side settings that define predefined combinations of pre-cursor, main cursor, and post-cursor tap weights to compensate for frequency-dependent channel loss.

Introduced in Gen3 and used through Gen6 and beyond, these presets provide coarse transmit equalization options spanning short, low-loss links to long, highly lossy channels, enabling interoperable and fast link training without full continuous tuning. During link equalization, the transmitter advertises its supported presets, the receiver evaluates their signal quality and then selects (and optionally fine-tunes around) the best preset to minimize intersymbol interference (ISI) while maintaining constant signal swing, ensuring reliable eye opening and BER performance across diverse PCIe interconnect topologies.

In the M8070B software, if the PHY protocol mode PCIe3, PCIe4, PCIe5, or PCIe6 for the pattern generator sequence is selected, the de-emphasis capabilities are switched from the multi-tap FIR to the PCI Express type of FIR editor with coefficient entry as integers dependent of the selected full swing.

A full swing from 24 to 63 coefficient resolution steps can be selected.

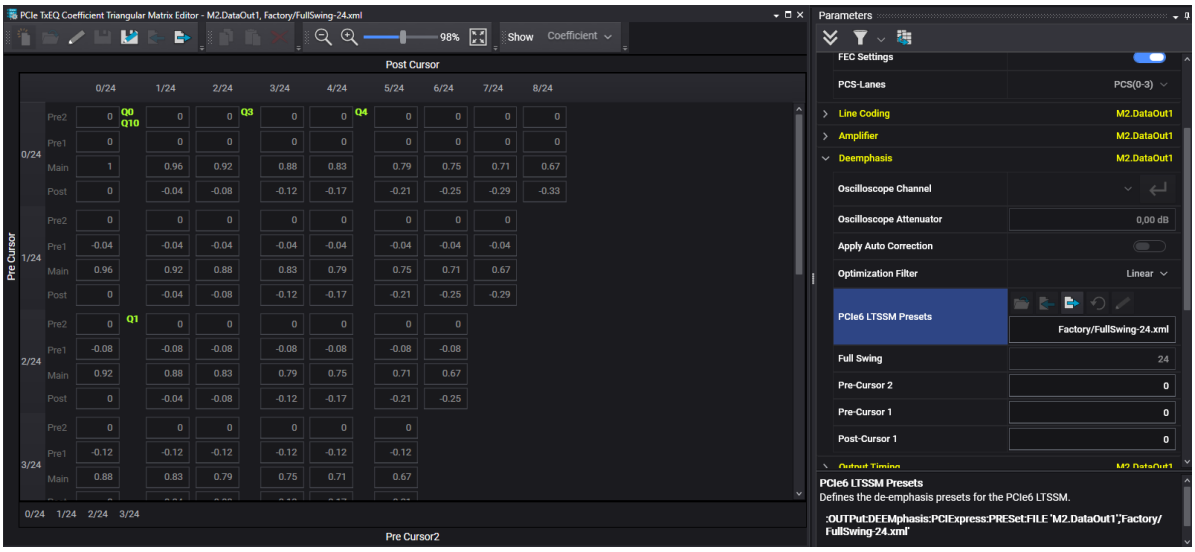


Figure 8. PCIe TxEQ matrix editor can be accessed if the PHY protocol mode PCIe3, PCIe4, PCIe5, PCIe6 is selected for the pattern generator sequence.

Forward Error Correction (FEC) Encoding

The Keysight M8042A pattern generator module supports native Forward Error Correction (FEC) encoding and precoding in accordance with IEEE 802.3cd and IEEE 802.3dj specifications, enabling realistic, PHY-compliant stimulus generation for advanced Ethernet interfaces. It implements Reed-Solomon FEC (RS-FEC) for 100GBASE-R, 200GBASE-KP4, and 2×400GBASE-KP4 at the PCS layer, including standards-compliant codeword framing, parity generation, and lane alignment. For KP4-based interfaces, mandatory precoding is supported to mitigate error propagation and improve post-FEC BER performance.

With option M8042A-0G9, users can inject errors pre- and post-FEC to validate receiver FEC decoding. The module operates at 53.125 GBd per lane for 100G-1 KP4, 200G-2 KP4, and 2×400G-4 KP4, and at 106.25 GBd per lane for 200GBASE-R with PAM4 line coding.

Table 3. Specifications for FEC (Forward Error Correction) encoding. Requires option M8042A-0G9.

Parameter	Value
FEC encoding	100GBASE-R, 200GBASE-KP4, 2×400GBASE-KP4
Reed-Solomon Code	RS (544,514)
Scrambler	PRBS 2^{58}-1
Pattern sequence	These patterns from pattern library can be FEC encoded: Remote faults, Scrambled idle
Line coding	PAM4
Symbol rate	53.125 GBd PAM4: 100GBASE (all PCS lanes), 200GBASE and 2×400GE (PCS 0→3 on PG1 and PCS 4→ 7 on PG2) 106.25 GBd PAM4: 200GBASE-R (clause 176, symbol multiplexing) (all PCS lanes)
FEC symbol error injection	Post-FEC engine error insertion
Pre-coder	PAM4: 1/ (1+D) mod4, can be switched on/off. Follows IEEE 802.3 Clause 135.5.7.2. for PAM4 encoded lanes.
Pre-requisites	M8042A with option 0G9

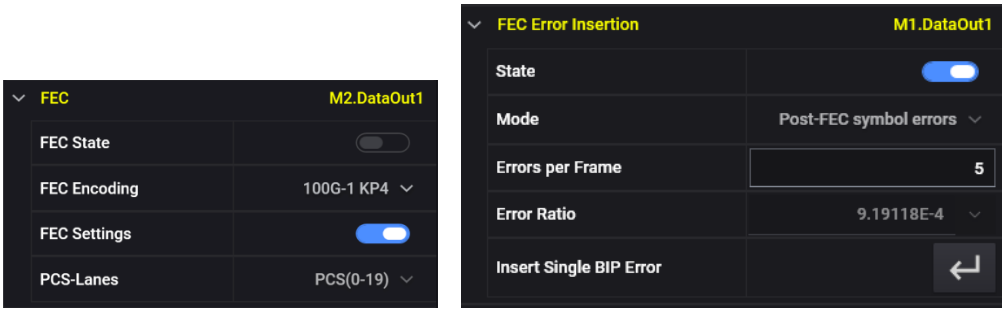


Figure 9. FEC encoding in M8042A (left) and FEC error insertion (right) shown in the M8070B software.

USB4 LFPS Generator

Low-Frequency Periodic Signaling (LFPS) in USB4 consists of low-speed electrical signaling bursts transmitted on the high-speed USB4 differential lanes when the link is not yet in normal data transmission mode. LFPS uses low-frequency square-wave–like pulses (typically in the few-MHz range) that can be reliably detected before clock recovery and high-speed equalization are established.

The USB4 LFPS Generator utility generates LFPS patterns with the M8070B software, allowing configuration of cycles, period, duty cycle, pre-data, and idle duration. Supported by the M8042A and M8045A modules, it handles USB4 Gen 2 (10 Gbps), Gen 3 (20 Gbps), and Gen 4 (25.6 GBd) data rates. The LFPS Generator offers Calibration and Rx testing modes, controllable with Start and Stop buttons.

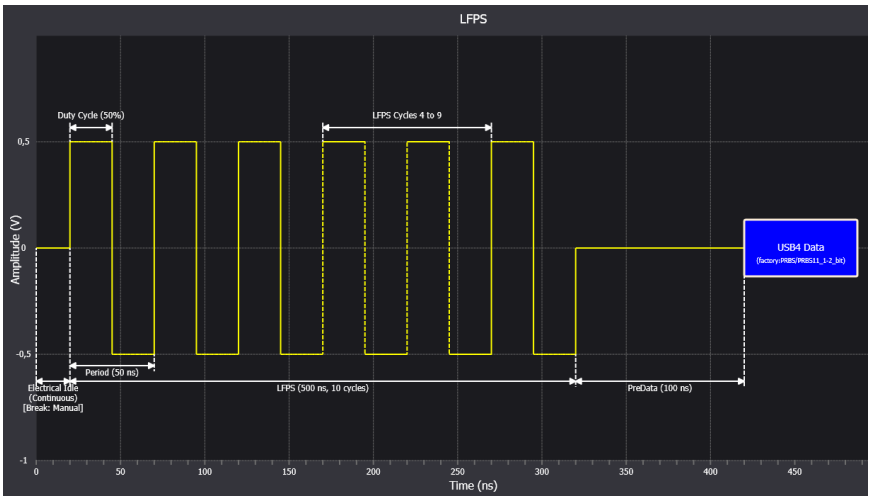


Figure 10. The USB4 LFPS generator utility shown in the M8070B software.

Trigger Output 1/2 (Trig Out 1, Trig Out 2)

The Trigger Output 1 and Trigger Output 2 connectors on the M8042A pattern generator module provide programmable digital trigger signals that allow the BERT to be synchronized with external instruments or system events during test and characterization. These outputs generate timing-accurate trigger pulses derived from internal BERT events, enabling precise correlation between bit-level behavior and external measurements.

The trigger outputs can be used in one of the different modes:

- Divided clock with dividers:
  - Max output frequency is 8.0 GHz, divider range 2 to 65000.
  - Minimum divider n is the next integer value above the symbol rate/ 8 GHz (Example: for a symbol rate of 53 GBd, n = 7, because it is the next higher integer of 53 / 8 = 6.625).
- Sequence block trigger
- Pulse mode triggered by sequencer (only if memory pattern is used)
  - Pulse width min 16 UI. Max block length
  - Offset min 0. Offset Max block length -1
- "Pulse on PRBS" mode (NRZ only). Matched pattern without ignoring defined bits (only if algorithmic pattern is used)
  - Pulse width: minimum 16 UI, maximum PRBS length.

The trigger signals are typically TTL/CMOS-level digital pulses, intended for direct connection to the trigger or external-reference inputs of oscilloscopes, logic analyzers, spectrum analyzers, or other test equipment.

The trigger output 2 is only available in the two-channel version of the M8042A module.

Table 4. Trigger output characteristics of the M8042A.

Parameter	Value
Amplitude	0.1 to 1.0 Vpp single-ended
Jitter injection	The injected jitter is always the same as the jitter at the Data Out (excluding clk/2)
Delay	Follows Data Out delay Relative Trigger to Data Out delay: Range: 0 to 1000 UI with 1 UI resolution
Skew between trigger output and data output of same channel	460 ps maximum (measured)
Output voltage window	–1 to 3 V [1] [2]
External termination voltage	–1 to 3 V
Impedance	50 Ω
Connector type	3.5 mm, female

1. High level voltage range= 2/3*Vterm – 0.9 V < HIL < Vterm + 2 V
2. Low level voltage range= 2/3 *Vterm – 1 V < LOL < Vterm + 1.9 V

Control Input A/B (Ctrl In A, Ctrl In B)

Control Input A and Control Input B on the M8042A provide external digital control interfaces that allow real-time interaction between the pattern generator and external equipment or test logic. These inputs enable external signals to control, gate, or switch internal M8042A functions with deterministic timing, allowing tight integration into automated or system-level test environments.

The control inputs accept TTL/CMOS-level digital signals and are sampled synchronously with the M8042A's internal timing, ensuring repeatable and cycle-accurate behavior.

Each control input can be selected as: sequence trigger, error insertion.

Table 5. Control input A/B characteristics.

Parameter	Value
Input voltage	–1 V to +3 V
Termination voltage	–1 V to +3 V
Termination voltage accuracy	± (25 mV +1%)
Threshold voltage	–1 V to +3 V
Delay repeatability to data output	±512 UI maximum
Absolute delay to data output	< 25 µs
Connector type	3.5 mm, female

Control Output A/B (Ctrl Out A, Ctrl Out B)

Control Output A and Control Output B on the M8042A provide programmable digital output signals that reflect internal pattern-generator events or states. They allow the M8042A to drive or notify external equipment with precise, deterministic timing derived directly from the BERT's internal clock domain.

The control outputs generate TTL/CMOS-level digital signals and can be independently configured, enabling flexible coordination with external instruments, DUT control circuitry, or automated test systems. These outputs provide a pulse or static high/low if used from sequencer.

Table 6. Control output A/B characteristics.

Parameter	Value
Amplitude [1]	0.1 to 2 V
Output voltage window [1]	–0.5 to 1.75 V
Delay to data output	±512 UI maximum
Connector type	3.5 mm, female

1. When terminated with 50 Ω into GND. Doubles when operating into open.

Link Interfaces Link 1/2 (Link 1, Link 2)

Link 1 and Link 2 are logical link interfaces within the M8050A BERT system that represent independent, bidirectional test links between the transmitter (Tx) and receiver (Rx). The link interface enables interactive, low-latency link training (such as PCIe or USB requires) between a pattern generator channel and the M8046A analyzer module.

Requires a 4-wire mini coax **M8051A-801** (also orderable as M8041-61601).

Link 2 is available only with the two-channel version of the M8042A.

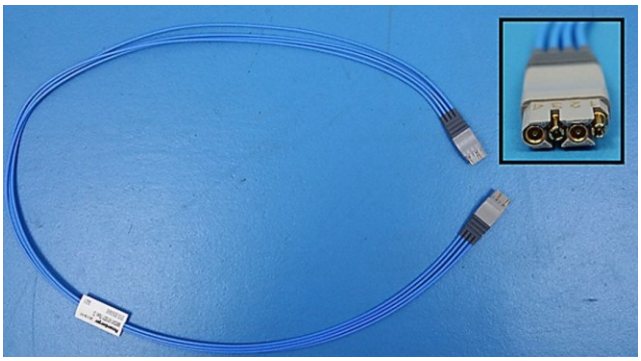


Figure 11. Link interface 4-wire mini coax M8051A-801.

Channel Clock Input 1/2 (Ch Clk In 1, Ch Clk 2)

Channel Clock Input 1 and Channel Clock Input 2 are used to supply the per-channel sampling clock from the M8009A clock module to the M8042A pattern generator. These clock inputs provide the timing reference required for precise symbol generation and deterministic operation at high data rates.

Channel Clock Input 2 is available only on the two-channel version of the M8042A and is used to provide an independent clock connection for the second pattern generator channel.

Connector type: 1.85 mm, female.

The following semi-rigid clock cables are supported for connecting the M8042A to the M8009A clock module:

- **M8042A-801** – Clock Semi-rigid Cable for Pattern Generator M8042A, Channel 1 (also orderable as M8042-61621)
- **M8042A-802** – Clock Semi-rigid Cable for Pattern Generator M8042A, Channel 2 (also orderable as M8042-61622)

Alternatively, a generic semi-rigid clock cable may be used, such as M8199A-810 – 450 mm semi-rigid clock cable, 1.85 mm (m) to 1.85 mm (m) (also orderable as M8199-61624, included in the M8042A-810 cable kit).

Synchronization Input (Sync In)

The Sync In input is used to connect the M8042A pattern generator to the M8009A clock module and provides a system-level synchronization reference. This input ensures deterministic alignment and timing coherence between the clock subsystem and the pattern generator, enabling stable operation and repeatable measurements, especially in multi-module or multi-channel configurations. The synchronization signal is essential for coordinated pattern generation and timing control within the M8050A BERT system architecture.

Connector type: 3.5 mm, female.

The following semi-rigid cable is supported for connecting the Sync In input of the M8042A to the Sync Out of the M8009A clock module:

- **M8042A-803** – Semi-rigid synchronization cable, 3.5 mm (also orderable as M8042-61623).

Local Bus Input/Output (LB In, LB Out)

Local Bus Input (LB In) and Local Bus Output (LB Out) provide local bus communication between adjacent AXIe chassis in a multi-chassis M8050A BERT configuration. LB In is used to receive local bus signals from the previous AXIe chassis, while LB Out forwards the local bus signals to the next AXIe chassis, enabling coordinated operation and system-level synchronization.

Connection is made using a 4-wire mini-coax local bus cable, M8051A-801 (also orderable as M8041-61601).

Specifications for Patterns and Sequences

The M8050A supports a wide range of built-in and user-defined patterns, including PRBS, fixed, and custom binary patterns, enabling comprehensive receiver testing. Patterns can be flexibly combined into programmable sequences to model realistic traffic, protocol behavior, and targeted stress conditions. Sequence control allows precise timing, looping, branching, and event-based triggering to emulate complex system scenarios. This capability enables efficient automation of test cases, corner-case analysis, and repeatable compliance and characterization measurements.

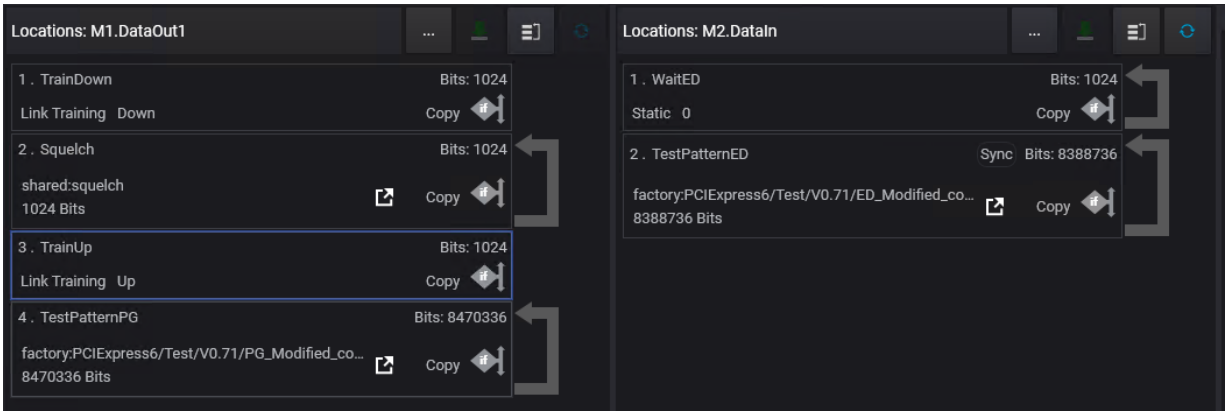


Figure 12. Sequence example in the M8070B for the M8042A pattern generator and M8046A error detector for PCIe 6.0 64 GT/s for the link training and LinkEQ receiver test.

Table 7. Specifications for patterns / sequences for M8042A pattern generator and M8043A error analyzer.

Parameter	Pattern generator M8042A	Error analyzer M8043A
PRBS (Odd)	2^n-1, n= 7, 10, 11, 15, 23, 23p, 31, 33, 35, 39, 45, 49, 51	Yes, same as M8042A.
PRBS (Even)	2^n, n=7, 10, 11, 13, 15	Yes, same as M8042A.
QPRBS	OIF-CEI: QPRBS13-CEI, QPRBS31-CEI IEEE 802.3: QPRBS13, PRBS13Q, PRBS31Q	Yes, same as M8042A.
PRTS [1]	3^n-1, n=17, 19, 23	No. For PAM3 support, please check the specifications of the M8046A from the M8040A datasheet.
User definable pattern memory	NRZ: 2 Gbit/ channel PAM3 and PAM4: 1 Gsymbol/channel PAM6 and PAM8: 1 Gsymbol/channel	Yes, same as M8042A.

Parameter	Pattern generator M8042A	Error analyzer M8043A
Pattern	Export, import, or factory patterns provided by the M8070B software.	Yes, same as M8042A.
Mark density	PRBS 1/8 to 7/8	
PAM4 coding	Gray coded Uncoded Custom mapping of bit combinations 00, 01, 10, 11 to symbols 0, 1, 2, 3.	Yes, same as M8042A.
Pre-coder	Yes (only for NRZ and PAM4)	No
PAM3 line coding	Uncoded Custom mapping of 00, 01,10, to symbols 0, 1, 2. 11 is interpreted as symbol 0. Memory based patterns only	No. Please check the specifications of the M8046A from the M8040A datasheet.
PAM6 line coding	Uncoded Custom mapping of 000, 001,010,011,100,101 to symbols 0, 1, 2, 3, 4, 5. 110 and 111 are interpreted as symbol 0. Editable XML file allows to map 5 bits to 2 symbols and 3 bits to 1 symbol. Memory based patterns only.	No. Please check UXR-based error analysis.
PAM8 line coding	Uncoded Custom mapping of 000, 001,010,011,100,101,110, 111 to symbols 0, 1, 2, 3, 4, 5, 6, 7. Editable XML file allows to map 5 bits to 2 symbols and 3 bits to 1 symbol. Memory based patterns only.	No. Please check UXR-based error analysis.
Scrambler	PAM3 only (according to USB4v2)	No
Vector / sequencer granularity	NRZ: 512 bit, PAM3/4/6/8: 256 Symbols	Yes, same as M8042A
Pattern capture	Not applicable	Yes, raw data Capture data starts on event User defined (minimum) amount of pre-event bits/ symbols and minimum capture bit/symbols Events: single error, user-defined error bursts, CTRL In, immediate Max 2 Gbit/ch capture data for NRZ, 1 Gsymbol / ch for PAM4 Save captured data: • With errors • As expected, data (ignores error content) • As PG data (ignores error content) • Export via pattern editor windows • Convert bits into all other codings and vice versa • Ability to mask error bits automatically. Display of captured data: • Display errors with color coding

Parameter	Pattern generator M8042A	Error analyzer M8043A
		• Navigate through error bits/symbols (find next/previous)
Pattern sequencer	3 counted loop levels, 1 infinite loop, # of blocks: 500 Minimum block length NRZ: 2048 Bits Minimum block length PAM3/4/6/8: 1024 Symbols	Same as M8042A for PAM3, PAM6, PAM8.
Error insertion	NRZ, PAM3/4/6/8: Single symbols, ratio variable/ fixed. [2] Error ratio range For PAM3: 10^n (n= -4 to -12) For NRZ/PAM4/8: 10^n (n= -1 to -12) Resulting SER For PAM3/4: 2 times the set error ratio. For PAM6/8: 3 times the set error ratio. Error insertion trigger: Manual, CTRL IN and sequencer break	Not applicable
Masking	Not applicable	Expected bits can be masked (ignored) during error counting. Bitwise and block-wise masking is possible.

1. PRTS – Pseudo-Random Ternary Sequence used in high-speed serial interfaces with three-level pulse amplitude modulation (PAM-3), which is adopted in recent standards such as USB4 Version 2.0.
2. For PAM6 resulting BER and SER do not match with set value. For PAM3 BER is around 1.33 times the set error ratio.

Specifications of M8009A Clock Generator Module with Jitter Modulation

Overview

The M8009A clock module provides high-performance, low-jitter clock generation for the M8050A BERT system. It supplies precise reference and channel clocks to pattern generator and analyzer modules and supports advanced jitter modulation for transmitter and receiver stress testing. The M8009A enables deterministic timing, system synchronization, and reliable operation across single- and multi-module BERT configurations.

The M8009A clock module with integrated jitter modulation capabilities operates in the frequency range from 4 to 60 GHz. It can be locked to external reference clocks.

Figure 13. The M8009A-062 clock module with jitter modulation is a 1-slot AXIe module. The M8009A clock module with option -061 has the same connectors, except that there is no Clk Out 32G.

The following functions require a dedicated module option (license):

- **M8009A-0G3** – Advanced jitter modulation for up to two channels, module-wide license.
- **M8009A-0G6** – Reference clock multiplier, module-wide license.

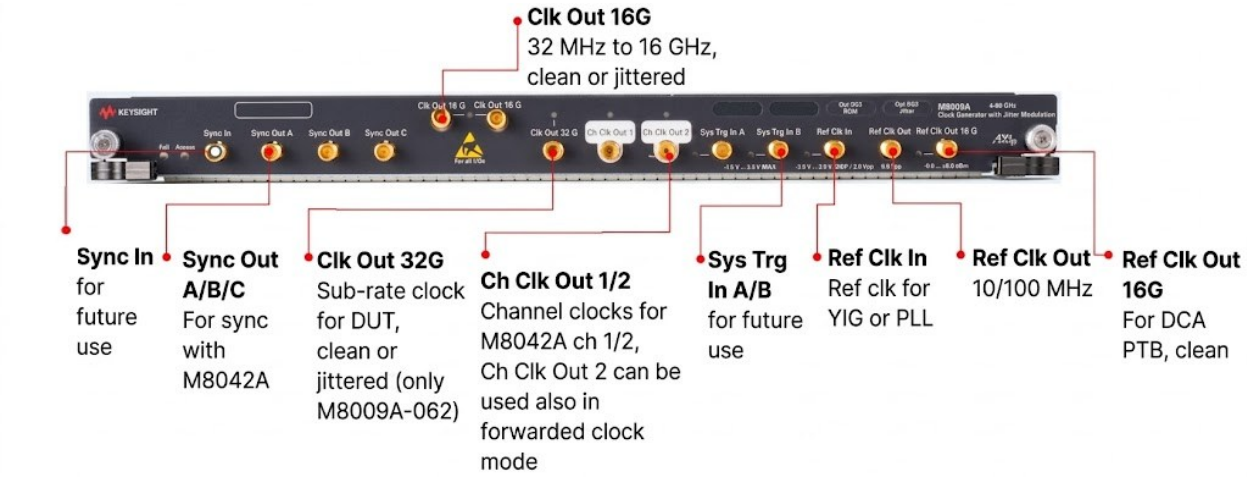


Figure 14. This figure gives an overview of all inputs and outputs of the M8009A-062 clock module with jitter modulation.

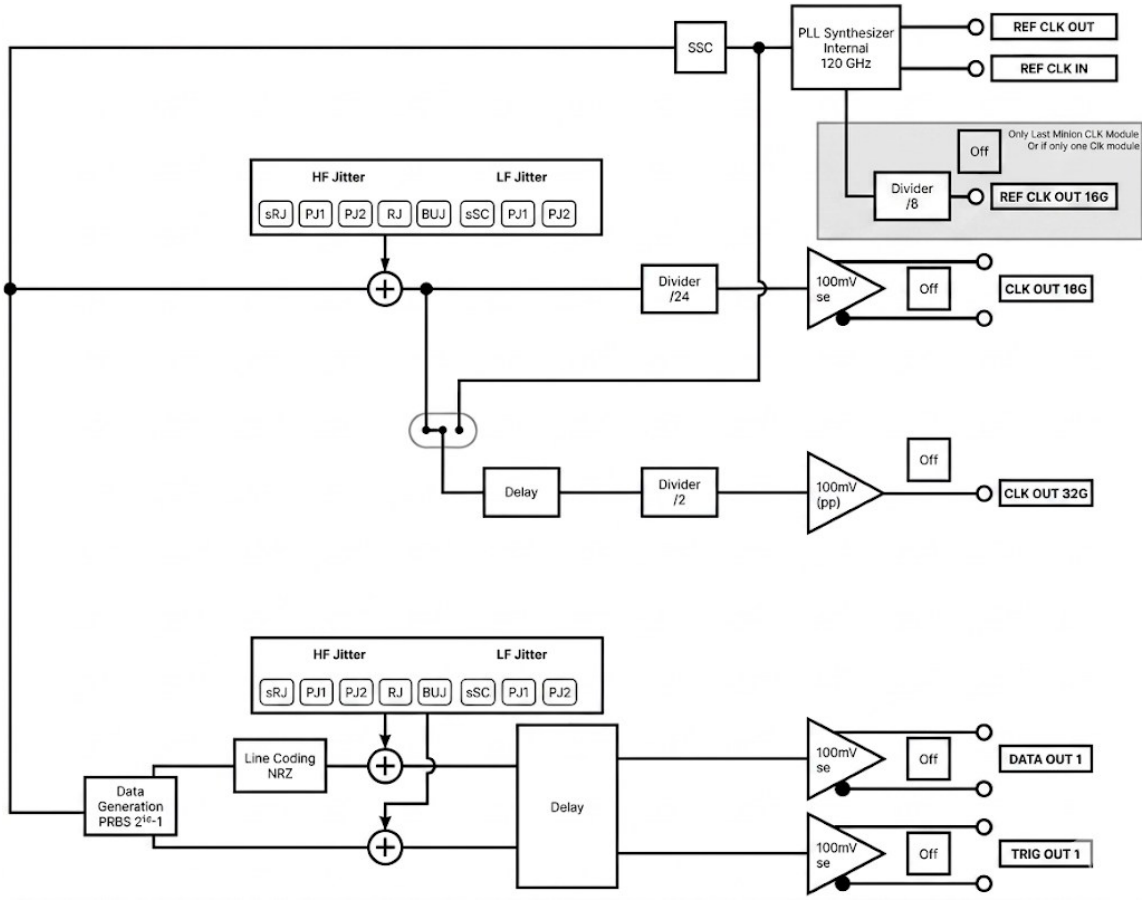


Figure 15. Simplified block diagram of the M8009A-062 clock module with jitter modulation and M8042A pattern generator module. Shown is a one channel configuration.

Internal Synthesizer and Clock Modes

Table 8. Internal synthesizer characteristics of the M8009A.

Parameter	Value
Frequency accuracy	±2 ppm
Frequency resolution	1 Hz

Table 9. Clock modes of the M8009A.

Clock mode	Clock generation	Input frequency range
Internal	PLL with internal reference	Not applicable
Reference clock	PLL with bandwidth < 100 kHz	10 or 100 MHz
Direct clock	No PLL. Maximum output frequency is 60 GHz	8 to 16.2 GHz
Reference clock with multiplier bandwidth	Multiplying PLL with m/n PLL with loop bandwidth: 100 kHz, others: see table 13, m, n = 1 to 12000	10 MHz to 16.2 GHz

Channel Clock Output 1 (Ch Clk Out 1)

Channel Clock Output 1 (Ch Clk Out 1) provides the low-jitter channel clock required for operation of the M8042A pattern generator module and supported AWG / interference source modules within the M8050A BERT system. This output delivers a precise and deterministic timing reference, ensuring accurate symbol generation and stable high-speed operation.

Ch Clk Out 1 must be connected to Channel Clock Input 1 (Ch Clk In 1) of the M8042A using a supported high-frequency clock cable. The clock signal supplied via this connection defines the symbol timing and directly impacts signal integrity and measurement repeatability. In multi-channel configurations, Ch Clk Out 1 serves as the primary clock source for the first pattern generator channel, enabling synchronized operation across the clocking and data generation subsystems.

Table 10. Channel Clock Output 1 characteristics.

Parameter	Value
Frequency range	4 to 60 GHz
Channels per module	1
Amplitude	Automatically adjusted for M8042A clock inputs
Frequency resolution	1 Hz
Frequency accuracy	±2 ppm typical (internal reference)
Data delay range	see M8042A
Intrinsic random jitter	For M8009A module with option -062: 3.0 mUI rms typical up to 20 GHz 3.5 mUI rms typical from 20 GHz to 32.25 GHz 5 mUI rms typical from 32.25 GHz to 60 GHz For M8009A modules with option -061 the following applies: 10 mUI rms typical @ 58 GHz 6 mUI rms typical @ 32 GHz

Parameter	Value
	8 mUI rms typical @ 16 GHz Refers to mUI of Ch Clk Out 1 frequency
Termination	50 Ω into GND. Do not operate into open. Unused outputs must be terminated.
Coupling	AC-coupled
Connector type	1.85 mm, female

Channel Clock Output 2 (Ch Clk Out 2)

Channel Clock Output 2 (Ch Clk Out 2) also provides a low-jitter channel clock for the second pattern generator channel within the M8050A BERT system. This output enables independent and deterministic clocking for dual-channel configurations, supporting accurate symbol timing and stable high-speed operation.

Ch Clk Out 2 must be connected to Channel Clock Input 2 (Ch Clk In 2) of the M8042A pattern generator module when the two-channel version is used. The clock signal supplied through this connection defines the timing reference for the second data output channel and ensures proper synchronization across the system.

Channel Clock Output 2 (Ch Clk Out 2) can be configured to operate in one of the two modes:

1. **Channel Clock mode**
   In this mode, Ch Clk Out 2 provides the clock signal for the second channel of the M8042A pattern generator. Ch Clk Out 2 must be connected to Channel Clock Input 2 (Ch Clk In 2) of the M8042A. An independent jitter profile can be applied to Ch Clk Out 2, allowing different jitter conditions from Channel Clock Output 1.
2. **Forwarded Clock mode**
   In this mode, Ch Clk Out 2 is intended to drive a DUT that requires a divided-data-rate clock. The output can carry identical jitter characteristics to Channel Clock Output 1. The forwarded clock remains synchronous to the data pattern; however, the phase relationship changes when the divider settings are modified.

Table 11. Channel Clock Output 2 characteristics in Channel Clock Mode.

Parameter	Value for the forwarded clock mode	Value for the channel clock mode
For M8009A modules with option -062 the following applies:		
Frequency range	4 to 60 GHz	4 to 60 GHz
Frequency divider factor	Symbol rate / clock divider is fixed, value 2	Not applicable
Intrinsic random jitter	3.0 mUI rms typical up to 20 GHz 3.5 mUI rms typical from 20 to 32.25 GHz 5 mUI rms typical from 32.25 to 60 GHz	3.0 mUI rms typical up to 20 GHz 3.5 mUI rms typical from 20 to 32.25 GHz 5 mUI rms typical from 32.25 to 60 GHz
For M8009A modules with option -061 the following applies:		
Frequency range	2 to 32.4 GHz	4 to 32.4 GHz
Frequency divider factor	Symbol rate / clock divider n with n = 2, 4, 8, 16, 32	Not applicable

Parameter	Value for the forwarded clock mode	Value for the channel clock mode
Intrinsic random jitter	10 mUI rms typical @ 16 and @ 32 GHz. Refers to mUI of Ch Clk Out 1 frequency	6 mUI rms typical @ 32 GHz 8 mUI rms typical @ 16 GHz Refers to mUI of Ch Clk Out 1 frequency
The following specifications are valid for both M8009A-061 and -062:		
Amplitude	0.5 to 1.2 Vpp typical, single-ended	Automatically adjusted
Duty cycle	50%, accuracy ± 10% typical	50%, accuracy ± 10% typical
Data delay range	Not applicable	See M8042A
Jitter delay range	±40 ns	±40 ns
Termination	50 Ω into GND. Do not operate into open.	50 Ω into GND. Do not operate into open.
Coupling	DC-coupled, use DC-blocks when non-GND termination voltages are present.	Not applicable
Connector type	1.85 mm, female	1.85 mm, female

Clock Output 32G (Clk Out 32G)

Clock Output 32G (Clk Out 32G) is intended to drive a DUT that requires a sub-rate clock. The output can carry identical jitter characteristics to Channel Clock Output 1, enabling consistent jitter conditions between data and clock domains. The clock signal is aligned to the data pattern.

Clock Output 32G is available only on M8009A modules with option -062.

Table 12. Clock output 32G characteristics (available on M8009A-062).

Parameter	Value
Frequency range	1 to 32.4 GHz
Frequency divider factor	Symbol rate / clock divider n with n = 2, 4, 8, 16, 32
Amplitude	Adjustable from 0.5 to 1.2 Vpp typical, single-ended
Duty cycle	50%, Accuracy ± 10% typical
Jitter source	Clean clock: no SSC, no jitter Follow Clk out 16G: jitter has same profile as Clk Out 16G
Intrinsic random jitter	3 mUI rms typical. Refers to mUI of Ch Clk Out 1 frequency
Delay range	0 to 100 ns relative to Ch Clk Out 1
Delay accuracy	± (maximum (1.5 ps or 25 mUI whatever is higher) + 1% of entered value) typical
Jitter delay range	±40 ns
Termination	50 Ω into GND. Do not operate into open.
Coupling	DC-coupled. Use DC-blocks when non-GND termination voltages are present.
Connector type	1.85 mm, female

Reference Clock Input (Ref Clk In)

The Reference Clock Input (Ref Clk In) allows the system clock to be locked to an external 10 MHz or 100 MHz reference clock instead of the internal oscillator, enabling improved frequency accuracy and synchronization with external test equipment.

Table 13. Reference clock input characteristics.

Parameter	Value
Input amplitude	0.2 to 2.0 Vpp
Input frequency	
Reference mode	10 MHz or 100 MHz (±1%), sinewave or square wave
Direct mode	8 GHz to 16.2 GHz, Sine wave or square wave, input amplitude should be 1.0 to 1.2 Vpp
Clock multiplier mode	10 MHz to 16.2 GHz, sine wave or square wave
Termination	Single-ended, 50 Ω, AC-coupled
Connector type	3.5 mm, female

Table 14. Reference clock multiplier/divider characteristics. Requires M8009A-0G6.

Ref clock	Standard	Target symbol rate	Multiplier/divider	PLL bandwidth
100 MHz	PCIe	32 GBd PAM4	320	2 MHz
100 MHz	PCIe	64 GBd PAM4	640	2 MHz
100 MHz	PCIe	16 / 32 Gbps NRZ	160 / 320	2 MHz
100 MHz	PCIe	2.5 / 5.0 / 8.0 Gbps NRZ	25 / 50 / 80	5 MHz
100 MHz	USB4 Gen2/3	10 / 20 Gbps NRZ	100 / 200	5 MHz
103.125 MHz	TBT3 Gen2	10.3125 Gbps NRZ	100	5 MHz
103.125 MHz	TBT3 Gen3	20.625 Gbps NRZ	200	5 MHz
19.2 MHz [1]	MIPI M-PHY	2.496 / 2.9184 / 4.992 / 5.8368 / 9.984 / 11.6736 Gbps NRZ	130 / 152 / 260 / 304 / 520 / 608	2 MHz
26 MHz [1]	MIPI M-PHY	2.496 / 2.912 / 4.992 / 5.824 / 9.984 / 11.648 / 19.968 / 23.296 Gbps NRZ	96 / 112 / 192 / 224 / 384 / 448 / 768 / 896	2 MHz
38.4 MHz [1]	MIPI M-PHY	2.496 / 2.9184 / 4.992 / 5.8368 / 9.984 / 11.6736 / 19.968 / 23.3472 Gbps NRZ	65 / 76 / 130 / 152 / 260 / 304 / 520 / 608	2 MHz
52 MHz [1]	MIPI M-PHY	2.496 / 2.912 / 4.992 / 5.824 / 9.984 / 11.648 / 19.968 / 23.296 Gbps NRZ	48 / 56 / 96 / 112 / 192 / 224 / 384 / 448	2 MHz

1. These reference clock multipliers are supported by the M8009A-062 option only.

Reference Clock Output (Ref Clk Out)

The Reference Clock Output (Ref Clk Out) provides a reference clock signal that can be used to lock and synchronize other instruments within the test setup.

Table 15. Reference clock output characteristics.

Parameter	Value
Clock frequencies	10 MHz or 100 MHz (100 MHz is not available when using external 10 MHz Ref Clk In). Note: always derived from selected clock source, except in direct & clock multiplier mode. Then Ref Clk Out is derived from internal oscillator.
Amplitude	900 mVpp typical single-ended into 50 Ω, AC-coupled square wave.
Impedance	50 Ω, nominal
Connector type	3.5 mm, female

Reference Clock Output 16G (Ref Clk Out 16G)

The Reference Clock Output 16G (Ref Clk Out 16G) provides a clean clock signal in the range of 8 GHz to 16 GHz, derived relative to the symbol rate. It can be used for the clock input or as a trigger input for the precision time base of a Keysight DCA sampling oscilloscope. This output provides a clock signal only and does not include data modulation.

Table 16. Reference clock output 16G characteristics.

Parameter	Value
Clock frequency range	8 to 16.2 GHz
Amplitude	1100 mVpp sinusoidal typical, AC-coupled
Intrinsic random jitter	150 fs rms typical
Impedance	50 Ω, nominal
Termination voltage range	±500 mV nominal
Connector type	3.5 mm, female

Clock Output 16G (Clk Out 16G)

Clock Output 16G (Clk Out 16G) provides a reference clock signal for a DUT. The output can be operated with or without jitter, supporting a wide range of test and stress scenarios. It delivers a differential clock with adjustable amplitude, offset, and termination to match DUT requirements.

This output is not phase-aligned to the data output.

Table 17. Clock output 16G characteristics.

Parameter	Value
Frequency range	31.25 MHz to 16.2499 GHz
Frequency divider factors	n * (1,2,3, to 256) n = 2, 4, 8
Amplitude	0.2 Vpp to 1 Vpp single-ended into 50 Ω
Voltage window	-1.0 V to 3.7 V into 50 Ω
Duty cycle	50%, accuracy ±10%, typical < 10GHz 50%, accuracy ±15%, typical 10GHz to 16.2499GHz
Intrinsic random jitter	350 fs rms typical clock divider = 1
Jitter injection	LF jitter: Can be set independently from Data Out. LF jitter parameters and range; same as for Data Out. Requires M8009A option -0G3 HF jitter: Same values as Data Out 1, individually selectable per jitter type SSC: Same as Data Out
Termination	50 Ω into GND or external termination voltage, differential. Do not operate into open.
Coupling	DC-coupled
Connector type	3.5 mm, female

System Trigger Input A/B (Sys Trg In A, Sys Trg In B)

System Trigger Input A and System Trigger Input B are reserved for future use. These inputs are not currently used or supported by the M8050A BERT system.

Table 18. System trigger input A/B characteristics.

Parameter	Value
Input voltage range	–1 V to +3 V
Termination voltage	–1 V to +3 V
Threshold voltage	–1 V to +3 V
Connector type	3.5 mm, female

Synchronization Input (Sync In)

In a 4-channel configuration, the Synchronization Input (Sync In) on the secondary M8009A clock module is used to receive the synchronization signal from the primary M8009A clock module, ensuring coherent and deterministic operation across all channels.

A 4-channel configuration is supported only with the M8009A option -062.

Table 19. Synchronization input characteristics.

Parameter	Value
Cable required	M8199-61620. It is included in the M8042A-810 cable kit.
Connector type	3.5 mm, female

Synchronization Output A/B/C (Sync Out A, Sync Out B, Sync Out C)

Synchronization Outputs A, B, and C (Sync Out A/B/C) are used to transmit the synchronization signal to different M8042A pattern generator modules.

In a 4-channel configuration, these outputs are also used to forward the synchronization signal from the primary M8009A clock module to the secondary M8009A clock module, ensuring coherent system operation.

A 4-channel configuration is supported only with the M8009A-062.

Table 20. Synchronization output A/B/C characteristics.

Parameter	Value
Cable required	M8199-61620 (it is included in the M8042A-810 cable kit)
Amplitude	0.6 Vpp typical square wave into 50 Ohm
Connector type	3.5 mm, female

M8009A Jitter Specifications

The M8009A clock module features integrated and calibrated jitter sources, enabling precise and repeatable jitter generation for transmitter and receiver stress testing. It supports controlled injection of deterministic and random jitter components, allowing users to accurately emulate real-world operating conditions and standard-defined stress scenarios.

The calibrated jitter generation ensures high repeatability across test setups and measurement campaigns, providing confidence in correlation, margin analysis, and compliance testing. Tight integration with the M8000 BERT system software (M8070B) enables deterministic control, synchronization, and automation of jitter stress conditions within complex test environments.

Advanced jitter modulation functionality requires M8009A option -0G3.

Low-frequency jitter

Table 21. Specifications for low frequency periodic jitter (requires M8009A-0G3). Values shown are applicable at the data output of pattern generator remote heads M8058A and M8059A.

Parameter	Condition	Value
Amplitude range	For modulation frequencies of 100 Hz to 10 kHz	0 to 8000 UI see table below.
	For modulation frequencies between 10 kHz and 40 MHz and symbol rates < 3.95 GBd	0 to 20 MUI/s / Fmod
	For modulation frequencies between 10 kHz and 40 MHz and symbol rates between 3.95 and 7.9 GBd	0 to 40 MUI/s / Fmod
	For modulation frequencies between 10 kHz and 40 MHz and symbol rate > 7.9 GBd	0 to 80 MUI/s / Fmod
Frequency range	100 Hz to 40 MHz, sinusoidal modulation	
Jitter amplitude accuracy	±2% ±1 ps typical	
Adjustable	For each data channel independently, same LFPJ for data and trigger. Clk Out 16G can be set independently.	

Table 21. Low frequency (LF) periodic jitter ranges.

Symbol Rate	Max UI at modulation frequency 100 Hz to 10 kHz	Max UI at modulation frequency of 10 MHz	Max UI at modulation frequency of 40 MHz
2.0 to 3.95 GBd	2000 UI	2.0 UI	0.5 UI
3.95 to 7.90 GBd	4000 UI	4.0 UI	1 UI
7.90 to 120.00 GBd	8000 UI	8.0 UI	2.0 UI

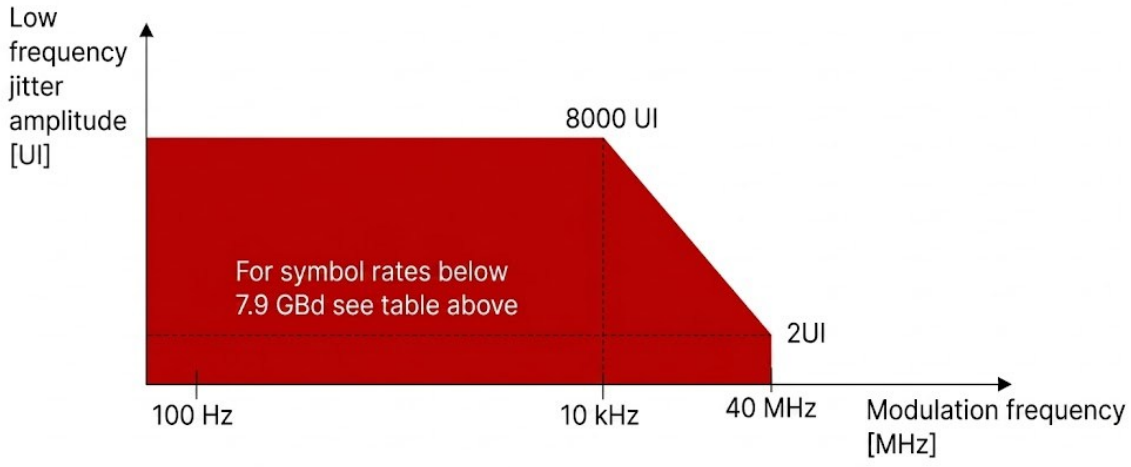


Figure 16. The multi-UI low frequency jitter range depends on selected baud rate and jitter modulation frequency. The graph shows the available range for symbol rates above 7.9 GBd when SSC is disabled.

High-Frequency Jitter

High-frequency (HF) jitter sources enable accurate emulation of high-frequency jitter components required for transmitter and receiver stress testing in high-speed serial applications. HF jitter is applied directly to the channel clock outputs, ensuring tight correlation between data and clock signals.

Table 23. High frequency jitter range (requires M8009A-0G3). This is the maximum sum of RJ, sRJ, HF-PJ1, HF-PJ2, and BUJ. Values shown are peak-peak and applicable at the data output of pattern generator remote heads M8058A and M8059A.

For symbol rates	Applicable for	Maximum sum
≥ 7.9 GBd	sRJ/ RJ/ BUJ/ HF-PJ1 [2]/ HF-PJ2 [2]	For M8009A-062: 1 UI For M8009A-061: 1 UI For 99 to 105 GBd: 0.3 UI [1]
3.95 GBd to < 7.9 GBd	sRJ/ RJ/ BUJ/ HF-PJ1 [2]/ HF-PJ2 [2]	0.5 UI
< 3.95 GBd	sRJ/ RJ/ BUJ/ HF-PJ1 [2]/ HF-PJ2 [2]	0.25 UI

1. For ambient temperatures <28 ºC.
2. The range is applicable when HF PJ modulation frequency is 500 MHz. For lower HF PJ modulation frequencies, see the specifications below.

The sum of RJ, sRJ, BUJ, HF-PJ1 and HF-PJ2 is calculated as follows: (A= jitter amplitude. f = jitter modulation frequency:

$$A_{BUJ} + A_{RJ} * 14 + A_{sRJHF} * 14 + A_{sRJLF} * 14 + \frac{A_{HFPJ1}}{\min\left(4, \frac{500\,\text{MHz}}{f_{HFPJ1}}\right)} + \frac{A_{HFPJ2}}{\min\left(4, \frac{500\,\text{MHz}}{f_{HFPJ2}}\right)} \leq \begin{cases} 0.25\,\text{UI for 2.0 to 3.95 GBd} \\ 0.5\,\text{UI for 3.95 to 7.9 GBd} \\ 1.0\,\text{UI for 7.9 to 120 GBd} \end{cases}$$

The extended amplitude ranges for HF-PJ1 and HF-PJ2, shown in this formula, are supported.

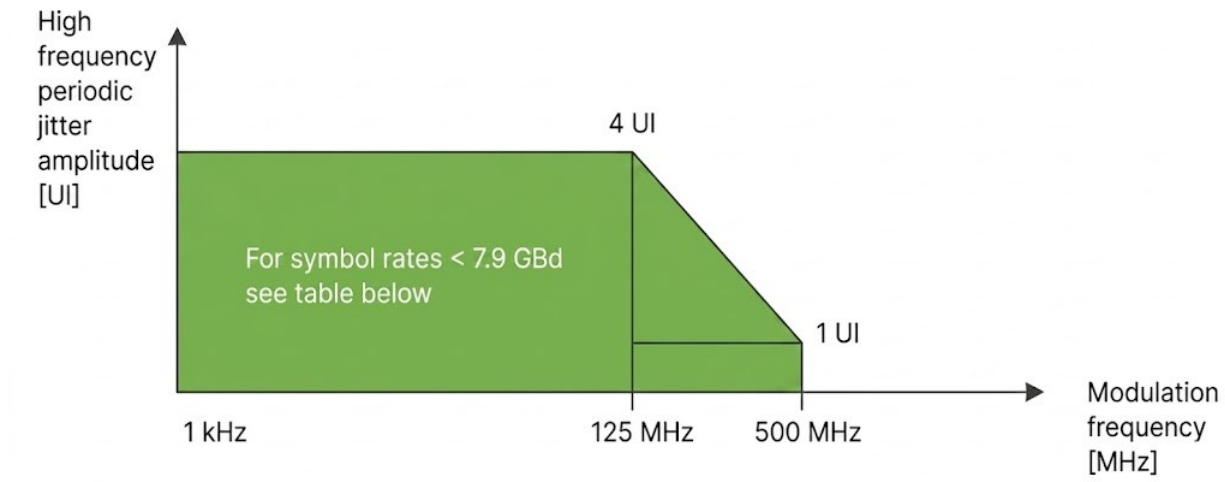


Figure 17. The high frequency jitter range depends on the selected symbol rate and the jitter modulation frequency. The graph shows the available range for one HF PJ source when all other HF jitter sources are off and for symbol rates above 7.9 GBd. For symbol rates below 7.9 GBd see table above.

Table 24. High-frequency periodic jitter modulation ranges (peak-peak).

Symbol rate	Max UI at modulation frequency between 1 kHz and 125 MHz	Max UI at modulation frequency of 250 MHz	Max UI at modulation frequency of 500 MHz
7.9 to 120.00 GBd	4.0 UI	2.0 UI	1.0 UI
3.95 to <7.9 GBd	2.0 UI	1.0 UI	0.5 UI
2.0 to <3.95 GBd	1.0 UI	0.5 UI	0.25 UI

Table 25. Specifications for high frequency periodic jitter, random jitter, bounded uncorrelated jitter.

Parameter	Condition	Value
High frequency periodic jitter (HF PJ1, HF PJ2)	Range	See HF jitter above [1]
	Frequency	1 kHz to 500 MHz. Two tones possible.
	Jitter amplitude accuracy	For M8009A-062: ±3 ps ±10% typical ±3 ps ±15% typical for symbol rates < 32.5 GBd and modulation frequencies > 100 MHz For M8009A-061: ±3 ps ±10% typical for symbol rates ≥ 32.5 GBd ±3 ps ±25% typical for symbol rates < 32.5 GBd
	Adjustable	For each channel independently
Random jitter (RJ)	Range	0 to 72 mUI rms max (1 UI p-p max) [1] See HF jitter above
	Jitter amplitude accuracy	For M8009A-062: ±300 fs rms ±10% typical for symbol rates ≥ 20.0 GBd ±300 fs rms ±20% typical for symbol rates < 20.0 GBd For M8009A-061: ±300 fs rms ±10% typical for symbol rates ≥ 32.5 GBd ±300 fs rms ±20% typical for symbol rates < 32.5 GBd
	Filters	High pass: 10 MHz and "off" Low pass: 100 MHz, 500 MHz, 1 GHz
	Adjustable	For each channel independently
	Crest factor	14 (peak-peak to rms ratio)
Spectrally distributed RJ according to PCIe Gen2 (sRJ)	Range	0 to 72 mUI rms max (1 UI p-p max) [1]
	Frequency	LF: 0.01 to 1.5 MHz, HF: 1.5 to 100 MHz
	Jitter amplitude accuracy	For M8009A-062: ±300 fs rms ±10% typical for symbol rates ≥ 20.0 GBd ±300 fs rms ±20% typical for symbol rates < 20.0 GBd For M8009A-061: ±300 fs rms ±10% typical for symbol rates ≥ 32.5 GBd ±300 fs rms ±20% typical for symbol rates < 32.5 GBd
	Adjustable	For each channel independently
Bounded uncorrelated jitter (BUJ)	Range	See HF jitter above [1]
	PRBS polynomials	2^n–1, n = 7, 8, 9, 10, 11, 15, 23, 31
	Filters	50/ 100/ 200 MHz low pass 3rd order

Parameter	Condition	Value
		150/ 300 MHz low pass first order (20 dB/ decade)
	Jitter amplitude accuracy	For M8009A-062: ±5 ps ±10% typical for settings shown in table below For M8009A-061: ±5 ps ±10% typical for symbol rates ≥ 32.5 GBd ±5 ps ±20% typical for symbol rates < 32.5 GBd for settings shown in table below
	Rate for PRBS generator	625 Mb/s, 1.25 Gbps, and 2.5 Gbps
	Adjustable	For each channel independently
Clock/2 jitter	See the M8042A data output specifications.	

1. Range of HF jitter applies to sum of RJ, HF-PJ1 and HF-PJ2, and BUJ. sRJ is mutually exclusive with RJ and BUJ. Valid if sRJ low pass filter is "on".

Table 26. BUJ accuracy applies for these conditions (requires M8009A-0G3).

Parameter [1]	Rate for PRBS generator	PRBS polynomial	Low pass filter
CEI 6G	1.25 Gbps	PRBS 2^9–1	100 MHz
CEI 11G	2.5 Gbps	PRBS 2^{11}–1	200 MHz
Gaussian	2.5 Gbps	PRBS 2^{31}–1	100 MHz
CEI 25G	2.5 Gbps	PRBS 2^{11}–1	200 MHz
CEI 56G	2.5 Gbps	PRBS 2^{11}–1	200 MHz
IEEE 802.3ck	2.5 Gbps	PRBS 2^7–1 PRBS 2^9–1	150 MHz
IEEE 802.3ck	2.5 Gbps	PRBS 2^7–1 PRBS 2^9–1	300 MHz
IEEE 802.3dj	2.5 Gbps	PRBS 2^7–1 PRBS 2^9–1	300 MHz

1. Other settings are not calibrated and do not necessarily generate the desired jitter histograms for all data rates of the PRBS generator.

Table 27. Specifications for spread spectrum clocking (SSC). SSC and segmented SSC are mutually exclusive. Requires M8009A-0G3 jitter modulation option.

Parameter	Condition	Value
SSC (spread spectrum clocking)	Symbol rate range for SSC	2 to 120 GBd
	Range [1] for center spread SSC	0 to 1% for symbol rates from 2 to 50 GBd For symbol rates from 50 to 120 GBd: max range is 50 GBd/ symbol rate * 1%. Example for 64 GBd: max SSC deviation is 50/64 *1% = 0.78%
	Range [1] for asymmetric, down-spread, up-spread SSC: Upper deviation range	0 to ± 1% for symbol rates up to 25 GBd For symbol rates from 25 GBd to 120 GBd: 25 GBd/ symbol rate * 1%. Example for 64 GBd: max SSC deviation = 25/64 *1% =0.39%

Parameter	Condition	Value
	Lower deviation range	
	Frequency	100 Hz to 200 kHz
	Modulation	Triangular and arbitrary modulation
	SSC amplitude accuracy	± 0.025% typical
	Outputs	Can be turned on/ off together for M8042A Data Out 1/2, Trg Out 1/2 and for M8009A Clk Out 16G and Channel Clk Out 1/2
Segmented SSC	Shape	Presets are available for: Universal Serial Bus (USB): USB4 10G, USB4 20G, USB4 40G, and DisplayPort (DP): DP RBR, DP HBR, DP HBR2, DP HBR3, DP UHBR10 User defined parameters: adjustable deviations from presets Custom: import of arbitrary waveforms for each segment
	Segments	Presets and user defined: 3 Custom: 1 to 4 Segment length: 32768 samples per segment
	SSC deviation range	See above range for asymmetric SSC
	SSC frequency	20 to 40 kHz
Residual SSC (rSSC)	Range	0 to 600 ps. Only for symbol rates ≤ 16 GBd.
	Modulation frequency	10 to 100 kHz
	Outputs	Can be turned on/off together for M8042A Data Out 1 and Trg Out 1 and for Data Out 2 and Trg Out2. Can be independently turned on/off for M8009A Clk Out 16G

1. Ranges are applicable when LF PJ and rSSC are turned off.

External Interference Sources

Overview

In high-speed digital links, the receiver must correctly recover data in the presence of intentional stress sources (interference) and unavoidable random disturbances (noise). Accurately emulating both is essential to validate receiver robustness, compliance, and real-world performance.

The Keysight M8053A and M8054A interference sources, together with the M8194A, M8195A, and M8196A arbitrary waveform generators (AWGs), can be used as external level-interference sources to generate sinusoidal interference (SI) and random interference (RI). The M8000 system software (M8070B) provides centralized control of key interference parameters, including amplitude, bandwidth, and crest factor.

Keysight offers matched coupler pairs, such as directional couplers and pick-off tees, for injecting SI or RI either before or after the channel, enabling flexible interference-injection topologies. The table below summarizes the supported configurations.

For additional details, refer to the datasheets of the M8053A, M8054A, M8194A, M8195A, and M8196A.

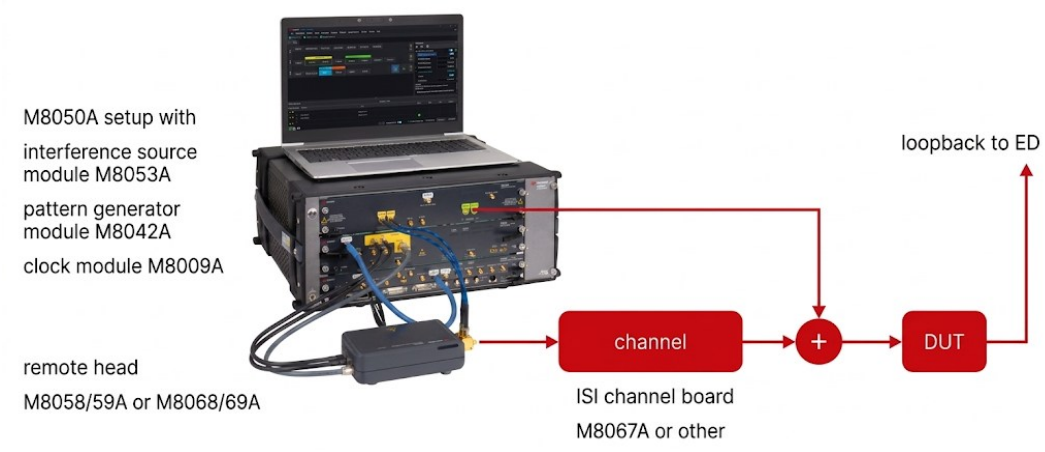


Figure 18. Keysight provides interference sources to be used in combination with M8050A to enable interference tolerance testing.

An overview of available interference sources from Keysight is shown in this table:

Model	Function	Description
M8053A Interference Source 64 GHz 	The Keysight M8053A interference source enables interference tolerance testing of highest-speed digital receivers supporting symbol rates above 64 GBd. Recommended for 1.6T Ethernet receiver (input) stress testing.	• RI and SI up to 64 GHz • 2 differential channels • 2-slot AXIe module • Control from M8070B
M8054A Interference Source 32 GHz 	The Keysight M8054A interference source, can be used as level interference source with sinusoidal and random modulation (also called gaussian or white noise). Recommended for USB, PCIe, SATA, SAS, 400GE receiver stress testing.	• RI and SI up to 32 GHz • 4 differential channels • 1-slot AXIe module • Control from M8070B
M8195A (25 GHz) / **M8196A** (32 GHz) / **M8194A** (40 GHz) Arbitrary Waveform Generators 	The Keysight M8195/6/4A AWGs are flexible sources with wide bandwidth suitable for multiple applications. They can also be used as level interference source with sinusoidal and random modulation.	• RI and SI up to 25 / 32 / 40 GHz • 4 differential channels • 1-slot AXIe module • Control from M8070B
81160A Pulse Function Arbitrary Noise Generator 500 MHz 	High precision pulse generators enhanced with versatile signal generation, modulation and distortion capabilities. Recommended for automotive Ethernet with symbol rates < 1 Gbps.	• Noise up to 160 MHz • Sinewave up to 500 MHz • Stand-alone instrument

Directional Couplers and Z-matched Pick-off Tees

In BER and receiver stress testing, external interference and noise sources are coupled into the victim data path to emulate real-world impairments such as crosstalk, power noise, and aggressor signaling. This is typically done using passive RF coupling components that preserve signal integrity while allowing controlled injection of disturbance signals. The two most common approaches are Z-matched pick-off tees and directional couplers.

Pick-off tees provide broadband, impedance-matched injection suitable for random noise and general receiver stress, while directional couplers offer controlled, directional coupling for deterministic interference and aggressor-victim scenarios. Both approaches are supported in Keysight M8050A BERT systems and are widely used in receiver compliance applications such as N5991x, N5992x, M8091x, and N4917x families, as well as in DCA accessory kits for high-speed electrical testing.

In some cases, power dividers or power splitters can be also used to combine stressed data signal and noise or to combine different noise and interference signals.

For the recommended options in concrete applications (Ethernet, PCIe, USB, etc.), please refer to the respective datasheets and/or configuration guides.

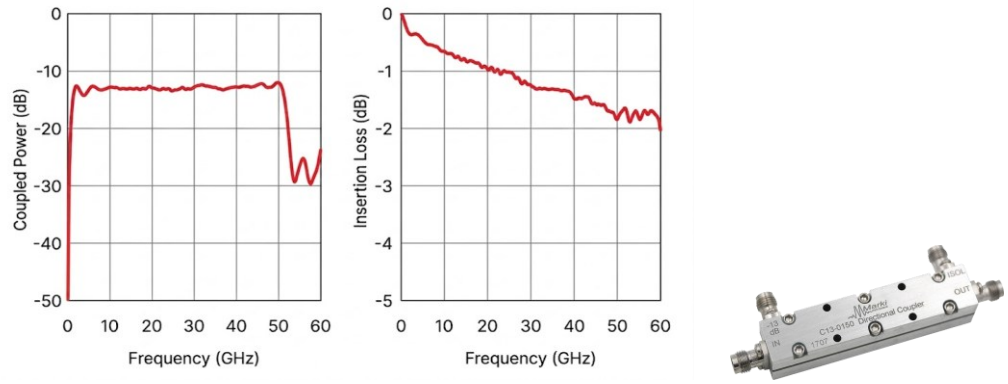


Figure 19. Example of the S-parameters for the M8045A-802 (matched directional coupler pair for external interference source, 50 GHz, 13 dB, 2.4 mm): insertion loss in the coupling path (left) and insertion loss in the through path (right).

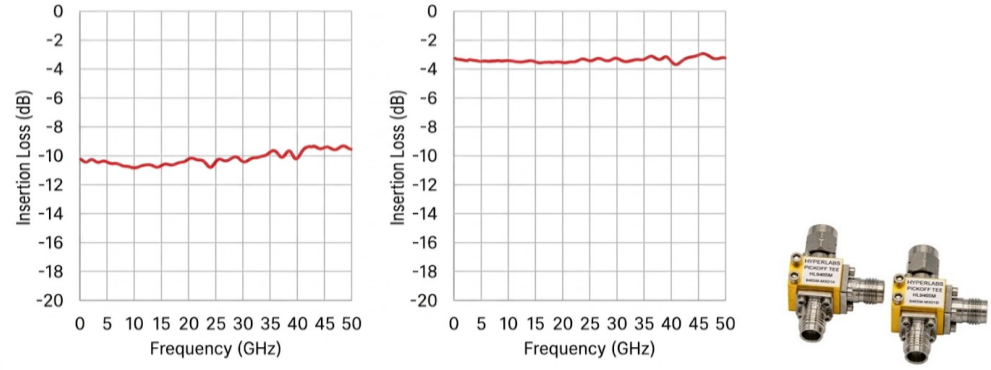


Figure 20. Example of the S-parameters for the M8045A-803 (matched coupler pair (Z-matched pick off tees) for external interference source, DC to 50 GHz, 12 dB, 2.4 mm): insertion loss in the coupling (pick-off) path (left) and insertion loss in the through path (right).

Below there are some common Keysight part numbers for directional couplers and pick-off tees used in high-speed digital testing.

- Directional couplers:
  - **M8045A-802** – Matched Directional Coupler Pair. Coupling (pick-off) path: DC to 50 GHz, coupling insertion loss 13 dB, connector type 2.4 mm, female. Through path: DC to 50 GHz, insertion loss 2.2 dB, connector type 2.4 mm, female (input), female (output).
- Pick-off tees:
  - **M8053A-803** – Matched Coupler Pair. Coupling (pick-off) path: DC to 64 GHz, coupling insertion loss 14 dB, connector type 1.85 mm, female. Through path: DC to 110 GHz, insertion loss 3.5 dB, connector type 1.00 mm, male/female.
  - **M8045A-803** – Matched Coupler Pair. Coupling (pick-off) path: DC to 50 GHz, coupling insertion loss 12 dB, connector type 2.4 mm, female. Through path: DC to 50 GHz, insertion loss 4 dB, connector type 2.4 mm, male/female.
  - **N1027A-2P2** – Matched Coupler Pair. Coupling path: 3.5 mm, female. Through path: 2.4 mm, male/female.
  - **N1027A-2P3** – Matched Coupler Pair. Coupling path: 3.5 mm, female. Through path: 2.92 mm, male/female.
  - **N1027A-2P8** – Matched Coupler Pair. Coupling path: 3.5 mm, female. Through path: 1.85 mm, male/female.
  - **N1027A-2P1** – Matched Coupler Pair. Coupling path: 3.5 mm, female. Through path: 1.00 mm, male/female.

Figure 21. N1027A-2P8 pick-off tees (matched pair). Refer to the "Technical Overview for DCA Accessories N1027A Kits and General-Purpose Parts" – publication number 5991-2340EN.

Intersymbol Interference

Intersymbol interference (ISI) is intentionally introduced in high-speed digital receiver testing to emulate channel impairments such as bandwidth limitation, reflections, and frequency-dependent loss. By injecting controlled ISI, receiver behavior can be evaluated under realistic and worst-case operating conditions.

ISI is typically generated using lossy channels, fixtures, cables, filters, or S-parameter–based channel emulation, degrading eye opening and increasing signal memory effects between consecutive symbols. This approach enables verification of receiver equalization performance, jitter tolerance, and overall robustness for NRZ and PAM4 signaling.

Keysight provides multiple approaches for injecting ISI to be used alongside the M8050A BERT.

Emulation of Adjustable ISI with M8070ISIB Plugin

The Adjustable ISI Software Package (M8070ISIB) simplifies receiver stress testing by providing a highly flexible method for emulating channel loss at baud rates of up to 120 GBd. Within a frequency range of up to half the symbol rate (SR/2), the pattern generator can emulate or de-embed a channel response by specifying target insertion loss values at defined frequency points.

This integrated channel emulation can be combined with physical ISI trace boards to construct a complete target test channel, enabling realistic and repeatable receiver stress conditions.

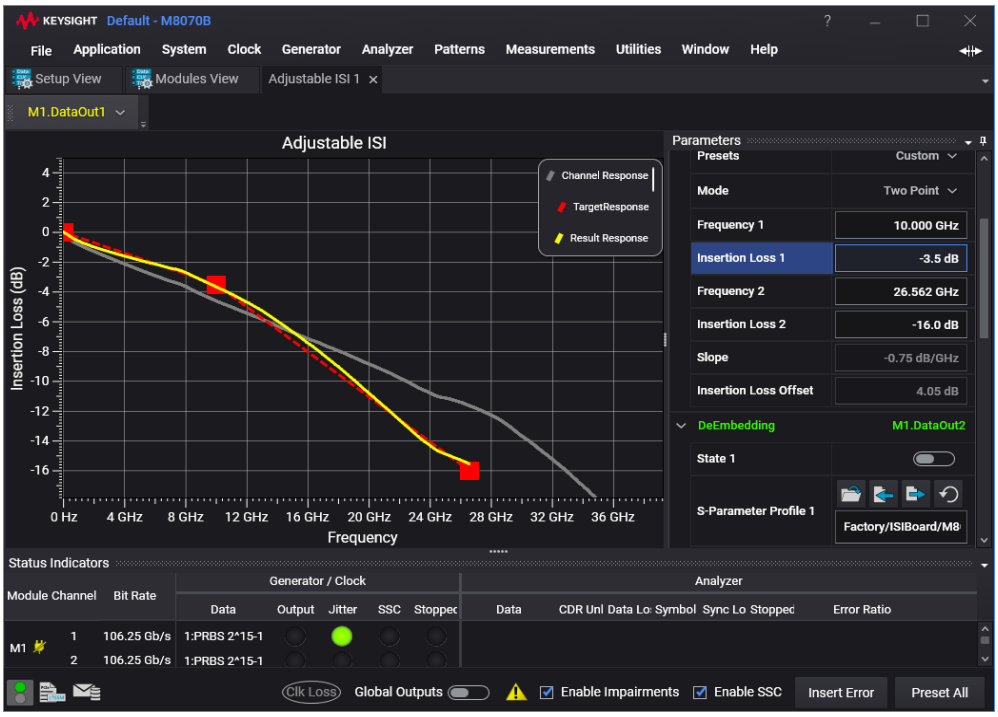


Figure 22. The adjustable ISI software package M8070ISI allows to emulate ISI internally with the M8042A pattern generator module. The example shows the insertion loss of an external ISI channel as channel response (gray). You can add or remove insertion loss (red for target response) at two frequency points.

Table 28. Specifications for the adjustable ISI when used with the M8042A pattern generator.

Parameter	Value	
Supported symbol rates	2.0 to 120.0 GBd for M8042A-G12 2.0 to 32.4 GBd for M8042A-G32 2.0 to 64.8 GBd for M8042A-G64	
Frequency range	A channel response can be emulated or de-embedded up to a maximum frequency range of symbol rate / 2 (Nyquist frequency).	
ISI modes	One Point Two Point S-Parameter from s2p or s4p file with adjustable weight	
ISI insertion loss	Range [1] at symbol rate / 2 Resolution Accuracy	-20 dB to +10 dB 0.1 dB 0.1 dB typical

Parameter	Value
De-embedding	Up to two s2p or s4p files with adjustable weight
Software download	For the latest version see: https://www.keysight.com/nl/en/lib/software-detail/computer-software/m8070isib-adjustable-isi-package.html.
License types	You can choose between node-locked, transportable, perpetual license, network, USB-dongle license types with different terms such as perpetual or 6/12/24-month subscriptions. The network license is only recommended when using multiple M8050A setups within one company.
Pre-requisites	Requires M8042A pattern generator module with de-emphasis option (M8042A-0G4) M8070B software revision 9.5.350.6 or higher M8070ISIB software revision 1.0.100.6 or higher M8042A module driver 2.5.50.0 or higher

1. The available loss range is referenced to the defined external ISI board or 0 dB if the external ISI board is set to NONE. It scales linearly from 0 Hz to symbol rate/ 2.

External ISI Channel Boards

Keysight offers external ISI channel boards to emulate realistic channel loss conditions for high-speed receiver testing.

M8049A ISI Channel Boards

For symbol rates below 32 GBd, the M8049A ISI channel boards are recommended. For detailed specifications and available channel profiles (S-parameters) for the M8049A, refer to the M8040A BERT datasheet.

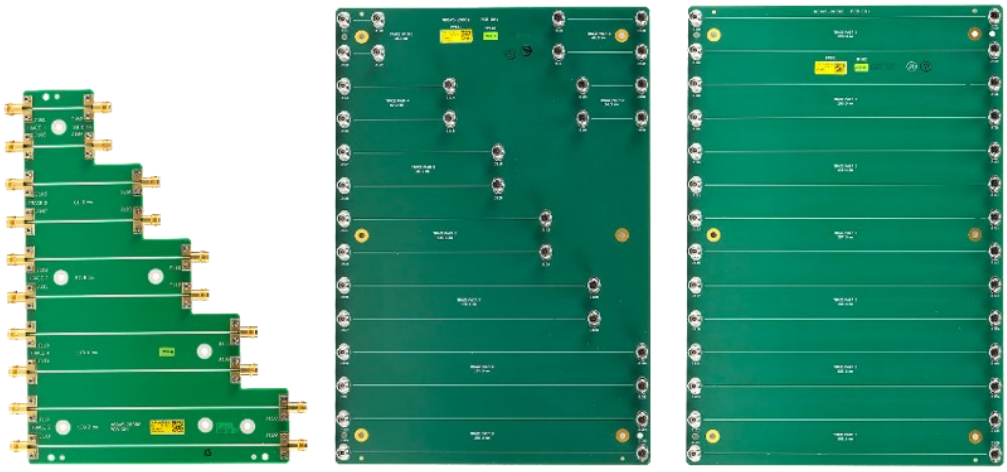


Figure 23. M8049A ISI channel boards.

M8067A ISI Channel Boards

The M8067A ISI channel boards support a wide range of channel loss profiles for symbol rates above 32 GBd, enabling accurate emulation of high-frequency interconnect impairments. The M8067A ISI channel boards provide well-characterized physical channels for emulating realistic intersymbol interference and channel loss in high-speed receiver testing at symbol rates up to 64 GBd and 120 GBd.

They offer multiple trace lengths and connector variants, enabling controlled insertion loss of approximately 5 dB to 30 dB across the relevant frequency range, with individual S-parameter models for accurate embedding.

The compact boards can be placed close to the DUT and are designed for repeatable, standard-oriented receiver stress and tolerance testing. For detailed specifications and available channel profiles for the M8067A, refer to the M8067A datasheet.

Figure 24. Keysight offers ISI channel boards M8067A-001, -002, -003, -004, and -005. The boards -001 and -002 offer 1.85 mm connectors and are suitable for emulating channel losses to characterize receivers that operate up to 64 GBd. For characterizing receivers that operate at symbol rates above 64 GBd and up to 120 GBd we recommend using the ISI channel boards M8067A-003, -004 or -005 with 1.00 mm connectors.

Part 2. Error Analysis

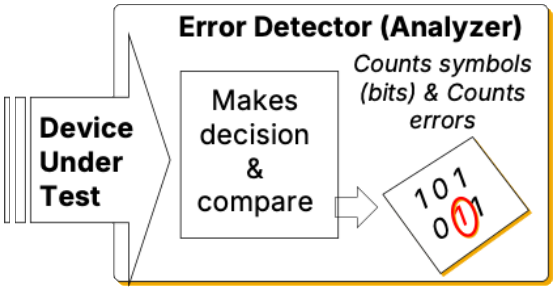
Error analysis evaluates the integrity of the received data by detecting and counting mismatches between the transmitted reference pattern and the recovered data from the DUT.

In BER testing, the error analyzer aligns to the incoming data stream, performs clock and data recovery as required, and statistically evaluates errors over very large numbers of bits.

Metrics such as BER, FBER, and error distributions allow quantitative assessment of link quality, margin, and compliance to standards such as PCIe and Ethernet.

Accurate error analysis is fundamental to validating receiver robustness, equalization effectiveness, and overall system reliability at very low error rates.

Error analysis involves detecting and counting errors in the received bit (symbol) sequence. It is crucial for bit error ratio testing as it quantifies the reliability and accuracy of the device under test.



Specifications of M8043A Error Analyzer Module with M8052A Remote Head

Overview

The Keysight M8043A and M8046A error analyzer modules support flexible receiver test configurations and can be used either standalone or in combination with the M8042A pattern generator. For symbol rates above 64 GBd, a real-time oscilloscope-based error analysis approach (using the Infiniium UXR-Series) is supported and fully automated through the M8070B system software. In addition, a DUT's internal error counter can be accessed via the DUT Control Interface (DCI), enabling automated receiver measurements such as jitter tolerance testing.

The following table provides an overview of available error analysis choices for the M8050A BERT platform:

Parameter	M8043A Error Analyzer	M8046A Error Analyzer	Infiniium UXR Real-time Oscilloscope
Supported symbol rates @ PAM4	2.4 to 64 GBd	2.4 to 58 GBd	14 to 224 GBd
Applications	400G and 800G Ethernet, PCIe 7.0 128 GT/s [1]	PCIe up to 6.x 64 GT/s and lower, USB 3.2, USB4	1.6T, 3.2T Ethernet
Line coding	NRZ, PAM4	NRZ, PAM3, PAM4	NRZ, PAM3, PAM4, PAM6, PAM8
Filtering of filler symbols	PCIe 128 GT/s	PCIe 2.5, 5, 8, 16, 32, 64 GT/s USB 5 and 10 Gbps, dual lane	No
Interactive link training	No	PCIe 8, 16, 32, 64 GT/s USB 5 and 10 GT/s, dual lane	No

1. The support is limited to the base specification only (no SSC).

For detailed specifications of the M8046A error analyzer, refer to the M8040A BERT datasheet.

The M8043A error analyzer module supports symbol rates from 2.0 to 64.4 GBd and requires the M8052A remote head. A built-in clock recovery function is included as standard and operates over the full symbol-rate range. Integrated equalization and de-embedding using FIR, FFE, and CTLE are available as optional features.

Figure 25. The error analyzer module M8043A provides one channel and occupies 2 slots in the AXIe chassis.

Figure 26. The analyzer remote head M8052A is required to operate the error analyzer module. The two cables on the back side of the remote head are used to connect with the M8043A error analyzer module.

Figure 27. The M8043A analyzer module occupies two slots of the AXIe chassis. It requires it to be operated with the remote head M8052A.

Using the remote head input of the M8043A error analyzer without the M8052A remote head connected is not permitted.

The following analyzer options are available:

- **M8043A-A32** – Error analysis up to **32.4 GBd for NRZ and PAM4**, including internal clock recovery (CDR), default configuration
- **M8043A-A64** – Error analysis up to **64.4 GBd for NRZ and PAM4**, including internal clock recovery (CDR), module-wide license
- **M8043A-0A3** – Equalization and De-embedding, module-wide license
- **M8043A-0S2** – SKP OS filtering for PCIe 7.0 with 128GT/s, module-wide license

Keysight also offers additional software packages for advanced measurements and error distribution analysis when used with the M8043A error analyzer. Refer to the M8070ADVB and M8070EDAB sections for more information.

Data Input

All data input specifications apply at the input of the matched cable pair M8058A-801 (150 mm length, 1.85 mm connectors) when connected to the M8052A remote head.

Table 29. Data input characteristics of M8043A with M8052A. Only valid with the M8052A remote head.

Parameter	NRZ	PAM4
Symbol rate	M8043A-A32: 2.0 GBd to 32.4 GBd M8043A-A64: 2.0 GBd to 64.4 GBd	
Channels per module	1	
Line coding	NRZ, PAM4	
Input sensitivity, single-ended [1, 2]	For NRZ eye height: 26.5625 GBd: 15 mV typical 32.0 GBd: 15 mV typical 53.125 GBd: 18 mV typical 64.0 GBd: 20 mV typical All values for a BER of 10^{-12}	For PAM4 eye height: 26.5625 GBd: 16 mV per eye typical 32.0 GBd: 16 mV per eye typical 53.125 GBd: 22 mV per eye typical 64.0 GBd: 27 mV per eye typical All values for a BER of 10^{-12}
Input amplitude range	100 mVpp to 1.2 Vpp, differential 50 to 600 mVpp, single-ended	
Input voltage range	-1.0 V to +3.0 V	
Input impedance	Differential: 100 Ω ± 4 Ω typical Single-ended: 50 Ω ± 2 Ω typical. Terminate unused input with 50 Ω.	
Input coupling	Selectable: AC/DC-coupled	
Termination voltage range	-1.0 V to +3.0 V Termination must be within a window of DC common voltage ± 1.5V	
Input bandwidth, 3 dB	Symbol rate / 1.8 (nom.). Example: 64.4 GBd / 1.8 = 35.8 GHz (nom). The bandwidth is limited by a digital filter with Raised Cosine characteristic	
Timing resolution	1 mUI (nom.)	
Sampling point	Manual/automatic. Finds optimum voltage range, threshold, and sampling point delay. Delay accuracy: ± 1 ps (nom.) One sampling edge per UI.	
Decision threshold range	-1.0 V to +3.0 V; full input voltage range	
Threshold resolution	1 mV (nom.)	
Equalization	Yes, requires M8043A option -0A3. See table below.	
Phase margin [1, 2, 3]	26.5625 GBd: 0.83 UI typical 32.0 GBd: 0.83 UI typical 53.125 GBd: 0.80 UI typical 64.0 GBd: 0.63 UI typical All values for a BER of 10^{-12}	26.5625 GBd: 0.30 UI typical 32.0 GBd: 0.30 UI typical 53.125 GBd: 0.25 UI typical 64.0 GBd: 0.10 UI typical All values for a BER of 10^{-12}
Connector type	1.85 mm, female	

1. Measured with a PRBS 2^{15}-1.
2. For single-ended operation: Terminate unused input externally with 50 Ω to GND.

3. With M8042A pattern generator. Amplitude of input signal: 450 mVpp, single-ended or 900 mVpp, differential.
4. Loss generated using a combination of M8067A ISI Channel Boards and Adjustable ISI Software Emulation M8070ISIB.
5. Loss compensated using a combination of S-parameter based de-embedding and automatic coefficient optimization offered with M8043A-0A3.
6. Differential operation.

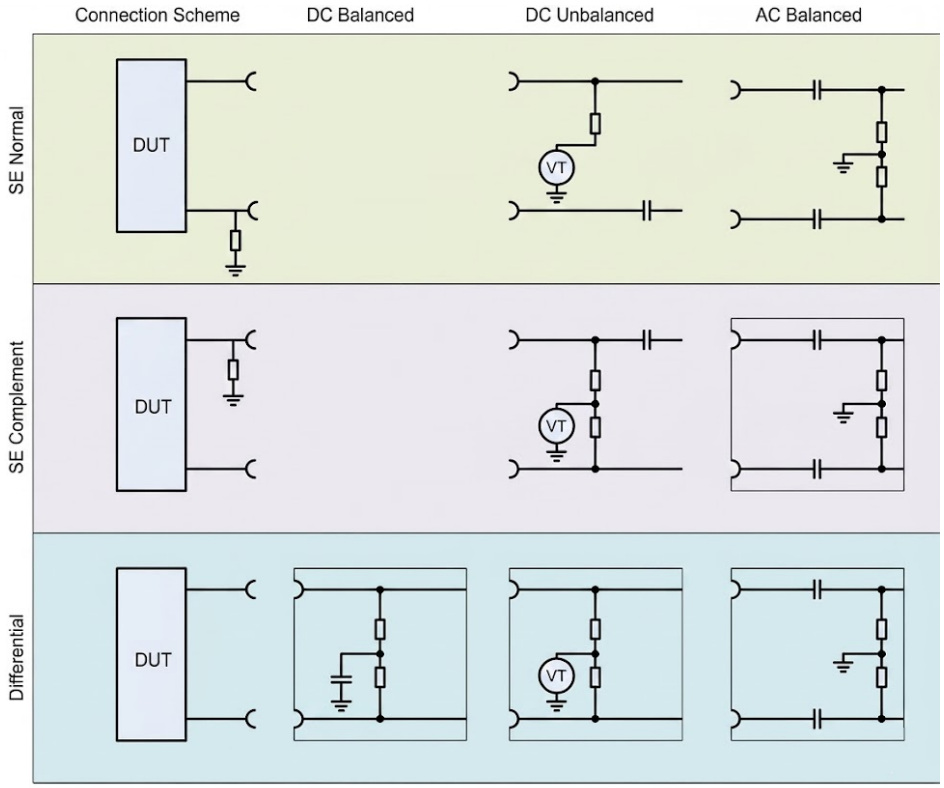


Figure 28. Connection and termination schemes for M8043A. To avoid floating offset: In "DC balanced, differential" mode, it is recommended to drive the input DC-coupled.

Equalization and De-embedding

The M8043A architecture incorporates advanced equalization and de-embedding capabilities to effectively compensate for channel impairments and insertion loss in the backchannel, enabling accurate receiver testing under real-world conditions.

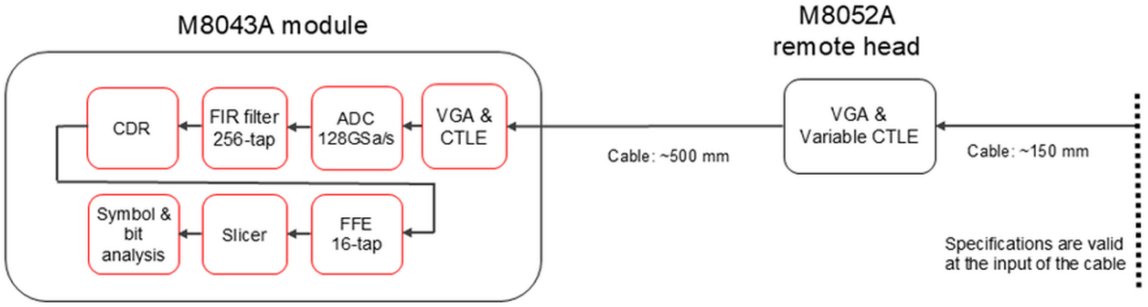


Figure 29. Block diagram of the M8043A error analyzer module with the M8052A remote head.

Equalization

For equalization of the backchannel between the DUT and the M8043A inputs, the M8043A employs a multi-stage equalization architecture. This architecture combines a 256-tap finite impulse response (FIR) filter operating at 128 GSa/s with a 16-tap feed-forward equalizer (FFE) running at the recovered symbol rate. Together, these equalization stages effectively compensate for frequency-dependent loss and distortion introduced by the backchannel.

To enable the equalization capability, the M8043A-0A3 equalization license is required.

Table 30. Equalization characteristics for M8043A with M8052A (requires M8043A-0A3).

Parameter	Value
Equalizer modes	Manual coefficient entry of the FFE. Automatic coefficient optimization of the FFE. Presets. Affects FIR filter
Manual FFE coefficient setting	16 filter coefficients numbered from 0 to 15. Coefficient 2 is the main course and cannot be changed. The available value range is: Coefficient 0: -0.25 to + 0.25 Coefficient 1: -0.5 to + 0.5 Coefficient 2: 1.0 Coefficient 3: -0.5 to +0.5 Coefficient 4: -0.25 to + 0.25 Coefficient 5: -0.125 to +0.125 Coefficient 6 to 15: -0.0625 to +0.0625 The sum of all 16 coefficients may not be 0.
Automatic coefficient optimization	Requires an input signal with random-like pattern. It's an iterative procedure to minimize BER.
Pre-configured equalizer settings (presets)	The following pre-configured equalizer settings are available: PCIe 3.0 @ 8 GBd NRZ: -12 dB to -6 dB, Resolution: 0.1 dB PCIe 4.0 @16 GBd NRZ: -12 dB to -6 dB, Resolution: 0.1 dB PCIe 5.0 @ 32 GBd NRZ: -15 dB to -5 dB, Resolution: 0.1 dB PCIe 6.0 @ 32 GBd PAM4: -15 dB to -5 dB, Resolution: 0.1 dB PCIe 7.0 @ 64 GBd PAM4: -15 dB to -5 dB, Resolution: 0.1 dB CEI-112G @ 56 GBd PAM4: -12 dB to -2 dB, Resolution: 0.1 dB IEEE 802.3 200GAUI-4: -9 dB to -1 dB, Resolution: 0.1 dB
Loss compensation [1, 2, 3, 4, 5] for a BER of 10^{-12}	**NRZ:** 26.5625 GBd: >30 dB (meas.) channel loss at 13.28 GHz 32.0 GBd: >30 dB (meas.) channel loss at 16.0 GHz 53.125 GBd: 30 dB (meas.) channel loss at 26.5625 GHz 64.0 GBd: 27 dB (meas.) channel loss at 32.0 GHz **PAM4:** 26.5625 GBd: 21 dB (meas.) channel loss at 13.28 GHz 32.0 GBd: 20 dB (meas.) channel loss at 16.0 GHz 53.125 GBd: 11 dB (meas.) channel loss at 26.5625 GHz 64.0 GBd: 10 dB (meas.) channel loss at 32.0 GHz

1. Measured with a PRBS 2^{15}-1. Differential operation.
2. With M8042A pattern generator. Amplitude of input signal: 450 mVpp, single-ended or 900 mVpp, differential.
3. Loss generated using a combination of M8067A ISI Channel Boards and Adjustable ISI Software Emulation M8070ISIB
4. Loss compensated using a combination of S-parameter based de-embedding and automatic coefficient optimization of the FFE offered with M8043A-0A3
5. It's possible to combine equalization and de-embedding capabilities. Using the combination, loss compensation cannot be significantly improved beyond the specifications in table 32.

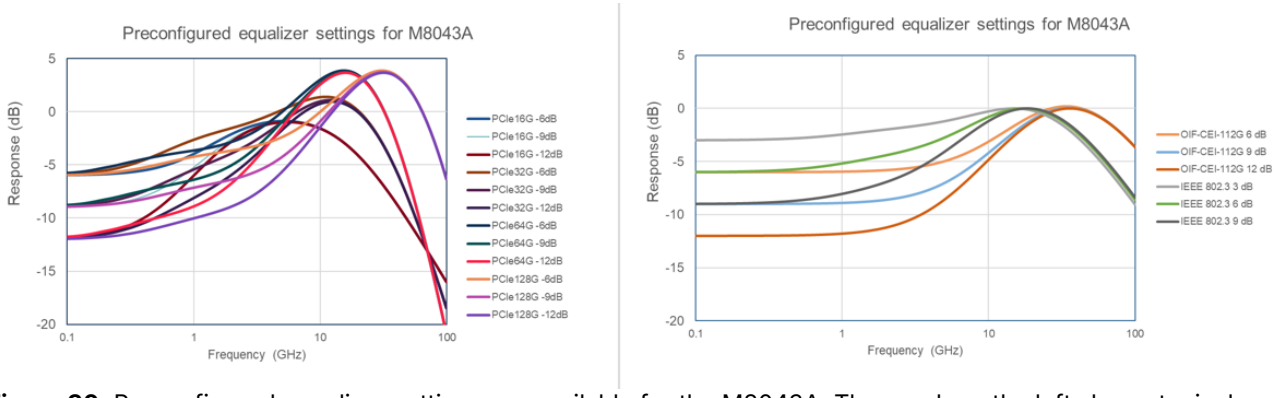


Figure 30. Preconfigured equalizer settings are available for the M8043A. The graph on the left shows typical PCIe responses for selected gains. Ethernet and OIF-CEI response characteristics are shown for selected gains in the graph on the right side. The gain can be adjusted in 0.1 dB steps over a wide range, as shown in the table above.

De-embedding

For de-embedding of the backchannel between the DUT and the M8043A inputs, the M8043A employs a combination of continuous-time linear equalization (CTLE) and a 256-tap finite impulse response (FIR) filter operating at 128 GSa/s. The high-resolution digital FIR filter provides powerful and highly accurate de-embedding of channel loss and distortion. The accuracy of the FIR-based de-embedding is determined by the filter length and coefficient resolution.

The de-embedding capability of the M8043A requires the M8043A-0A3 option.

Two de-embedding modes are supported:

- **Load S-parameters**: Channel characteristics are de-embedded using imported S-parameter files. The achievable loss compensation accuracy depends on the quality and accuracy of the provided S-parameter data.
- **Measure channel response**: The M8043A automatically measures the frequency response of the backchannel and applies the corresponding de-embedding.

Load S-parameters mode

Table 31. De-embedding capabilities for the M8043A by loading S-parameters (requires M8043A-0A3)

Parameter	Value
De-embedding [1]	The following functionality can be enabled or disabled: S-Parameter profile 1, .s2p or .s4p with adjustable weight S-Parameter profile 2, .s2p or .s4p with adjustable weight

1. De-embedding affects analog performance of data input such as e.g., sensitivity or phase margin.

Measure channel response mode

For de-embedding, the M8043A measures the frequency response of the backchannel. The measured response is used to calculate the coefficients of the 256-tap FIR filter, enabling compensation of channel loss and minimization of bit error ratio (BER).

During the channel response measurement, a predefined test pattern must be applied to the M8043A. To ensure correct operation of the algorithm and achieve optimal results, signal impairments such as spread-spectrum clocking (SSC), periodic jitter (PJ), and intersymbol interference (ISI) must be disabled.

The channel response measurement typically needs to be performed only once per test setup. The measurement includes the input characteristics of the M8043A. To maintain optimal backchannel loss compensation, the input range of the M8043A must not be changed while de-embedding based on the measured channel response is enabled.

After the channel response measurement of the backchannel is completed, the M8043A can analyze any pattern, including PRBS patterns and complex sequences. Signal impairments can also be applied after the measurement.

Table 32. De-embedding capabilities for M8043A with M8052A in the "Measure channel response" mode.

Parameter	NRZ [1, 2, 3, 4, 5]	PAM4 [1, 2, 3, 4, 5]
Measure channel response mode	Automatic coefficient optimization of the FIR filter and CTLE. Enable or disable	
Predefined pattern	Requires an input signal with a predefined pattern with the following characteristics: Minimum length: 1023 Symbols Maximum length: for symbol rate < 16 GBd: 8192 symbols for symbol rate 16 GBd to 64.4 GBd: 32 ksymbols NRZ or PAM4 Transition density: ~0.5 Max. run length of zeroes and ones: 31	
Execution time for "Measure channel response"	26 GBd to 32 GBd: PRBS 2^{10}-1: 95 s (meas.) 26 GBd to 32 GBd: PRBS 2^{15}-1: 320 s (meas.) 53 GBd to 64 GBd: PRBS 2^{10}-1: 90 s (meas.) 53 GBd to 64 GBd: PRBS 2^{15}-1: 200 s (meas.) Values apply for PAM4 line coding	
Channel loss compensation (for a BER of 10^{-12})	26.5625 GBd: >36 dB (meas.) at 13.28 GHz 32.0 GBd: >36 dB (meas.) at 16.0 GHz 53.125 GBd: 34 dB (meas.) at 26.5625 GHz 64.0 GBd: 30 dB (meas.) at 32.0 GHz	26.5625 GBd: 26 dB (meas.) at 13.28 GHz 32.0 GBd: 26 dB (meas.) at 16.0 GHz 53.125 GBd: 24 dB (meas.) at 26.5625 GHz 64.0 GBd: 24 dB (meas.) at 32.0 GHz
Channel loss compensation (for a BER of 10^{-9})	26.5625 GBd: >36 dB (meas.) at 13.28 GHz 32.0 GBd: >36 dB (meas.) at 16.0 GHz 53.125 GBd: >36 dB (meas.) at 26.5625 GHz 64.0 GBd: 35 dB (meas.) at 32.0 GHz	26.5625 GBd: 27 dB (meas.) at 13.28 GHz 32.0 GBd: 27 dB (meas.) at 16.0 GHz 53.125 GBd: 26 dB (meas.) at 26.5625 GHz 64.0 GBd: 26 dB (meas.) at 32.0 GHz
Channel loss compensation (for a BER of 10^{-6})	26.5625 GBd: >36 dB (meas.) at 13.28 GHz 32.0 GBd: >36 dB (meas.) at 16.0 GHz	26.5625 GBd: 34 dB (meas.) at 13.28 GHz 32.0 GBd: 34 dB (meas.) at 16.0 GHz

Parameter	NRZ [1, 2, 3, 4, 5]	PAM4 [1, 2, 3, 4, 5]
	53.125 GBd: >36 dB (meas.) at 26.5625 GHz 64.0 GBd: 36 dB (meas.) at 32.0 GHz	53.125 GBd: 29 dB (meas.) at 26.5625 GHz 64.0 GBd: 29 dB (meas.) at 32.0 GHz

1. Measured with a PRBS 2^{15}-1. Differential operation.
2. With M8042A pattern generator. Amplitude of input signal: 450 mVpp, single-ended or 900 mVpp, differential.
3. Loss generated using a combination of M8067A ISI Channel Boards and Adjustable ISI Software Emulation M8070ISIB.
4. Loss compensated using 'Measure Channel response' mode offered with M8043A-0A3.
5. It's possible to combine equalization and de-embedding capabilities. Using the combination, loss compensation cannot be significantly improved beyond the specifications in this table.

Clock Data Recovery (CDR) and Source-Synchronous Modes of Operation

CDR Mode of Operation: The M8043A features an integrated clock data recovery (CDR) that is always enabled during operation. The CDR supports symbol rates from 2.0 to 64.4 GBd and provides robust clock recovery across the full operating range, ensuring reliable data analysis in clock-embedded signaling environments.

Source-Synchronous Mode of Operation: The M8043A supports source-synchronous operation at symbol rates of 8, 16, 32, and 64 GBd. In this mode, a reference clock is provided externally in parallel with the data signal. By applying the same spread-spectrum clocking (SSC) profile to the data input as to the clock input of the M8043A, data streams with large SSC deviations can be analyzed reliably. In source-synchronous mode, the CDR remains enabled and is used to automatically compensate for residual SSC components, as well as for any skew between the clock and data inputs, ensuring optimal sampling even under stressed conditions.

CDR Specifications

Table 32. Clock data recovery characteristics for M8043A with M8052A remote head.

Parameter	Value
Clock recovery supported symbol rate range	M8043A-A32: 2.0 to 32.4 GBd for NRZ and PAM4 M8043A-A64: 2.0 to 64.4 GBd for NRZ and PAM4
Loop bandwidth	1.1 MHz (nom.)
Transition density	25% to 100% (nom.)
Capture range	For symbol rates 2.0 to 7.9 GBd: ± 500 ppm typical For symbol rates 7.9 to 15.8 GBd: ± 300 ppm typical For symbol rates 15.8 to 31.6 GBd: ± 150 ppm typical For symbol rates 31.6 to 64.4 GBd: ± 75 ppm typical
SSC tracking range[1]	For symbol rate: 16 GBd: Deviation ± 1500 ppm measured For symbol rate: 32 GBd: Deviation ± 750 ppm measured For symbol rate: 64 GBd: Deviation ± 250 ppm measured SSC tracking range in source-synchronous mode is shown in table 34
CDR freeze	Provided

1. SSC type: Center spread; SSC frequency: 33 kHz. All values for a BER 10^{-12}.

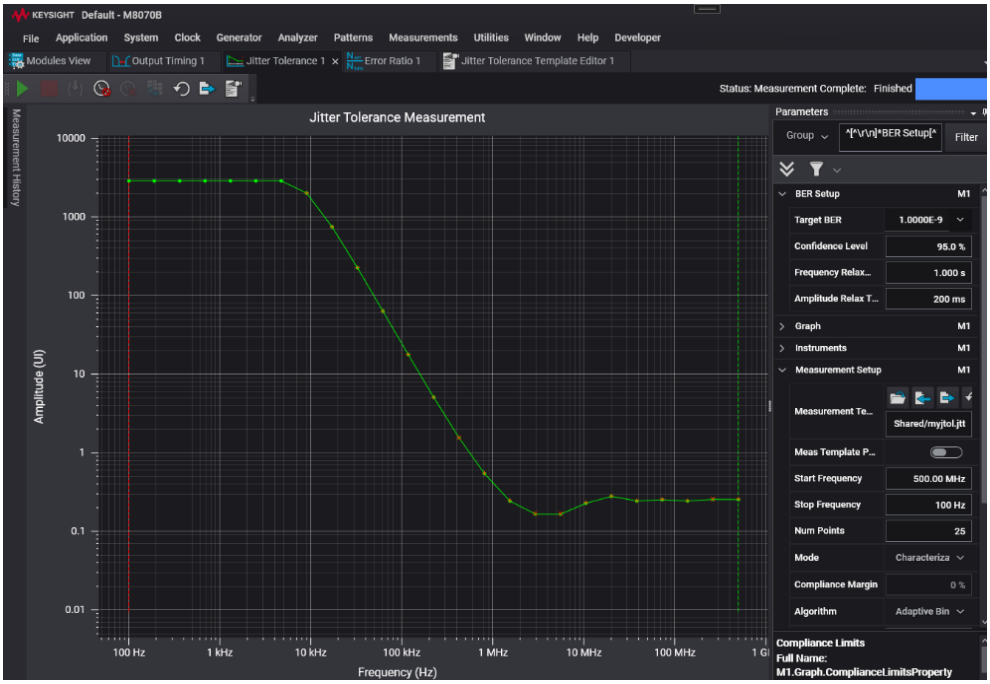


Figure 31. The M8042A can be used for jitter tolerance measurements. The example shows a jitter tolerance measurement at 53.125 GBd PAM4 PRBS pattern in direct loopback from the M8042A pattern generator when all other impairments are turned off. This measurement uses CDR mode. Source-synchronous mode is not enabled.

Source-Synchronous Mode Specifications

This clock input is designed for source-synchronous operation of the M8043A. This mode enables the M8043A to analyze data streams with spread-spectrum clocking (SSC). In this mode, the M8043A's integrated clock data recovery (CDR) remains enabled and is used to compensate for skew and residual jitter between the clock and data inputs.

For optimal SSC tracking by the M8043A, residual jitter must be minimized by adjusting the relative delay between the clock and data signals. This ensures that the phase of the SSC profile is aligned at both the Data Input and Clock Input of the M8043A.

The clock and data signals applied to the M8043A can be generated directly by the device under test (DUT). Alternatively, source-synchronous operation can be achieved by connecting the Clock Input of the M8043A to the 32-GBd clock output of the M8009A clock module. In this configuration, data generated by the M8042A pattern generator is applied to the DUT, and the DUT returns the data to the M8043A error detector for analysis.

Clock Input operation requires an M8043A with a serial number greater than MY64A01000.

Table 33. Clock Input characteristics for M8043A.

Parameter	Value
Input frequency	Selectable: 4 GHz, 8 GHz or 16 GHz
Frequency accuracy	- 3000 ppm to + 500 ppm (typ.)
Input level	502 mV_{pp} (-2 dBm) to 1.4 V_{pp} (+7 dBm) (typ.)

Parameter	Value
Input impedance	50 Ω (nom.), AC-coupled
Connector type	SMA, female

Table 34. Source-synchronous mode of operation of M8043A.

Parameter	Value
Symbol rates	8 GBd, 16 GBd, 32 GBd or 64 GBd for NRZ and PAM4
SSC tracking range [1]	Deviation: - 6000 ppm to + 1000 ppm (typ.)

1. SSC frequency: 33 kHz. All values for a BER 10^{-12}. SSC phase delay between Clock In and Data in less than ± 10ns

Control Input (Ctrl In)

The Control Input (Ctrl In) provides external event control for the M8043A error detector. Depending on the selected configuration, the Ctrl In can be used to support advanced measurement synchronization and capture functions.

The functionality of the Control Input can be configured as one of the following:

- **Sequence Trigger:**
  In this mode, the Ctrl In accepts an external trigger signal to start, stop, or synchronize a measurement sequence. This enables precise coordination of BER measurements with external test events, such as DUT state changes or pattern transitions.
- **Pattern Capture Event:**
  When configured as a pattern capture event, the Ctrl In triggers the capture of data or error information at a precisely defined moment. This is useful for analyzing specific events, error bursts, or pattern-dependent behavior within the received data stream.

The Control Input allows tight integration of the M8043A into automated test setups and enables deterministic correlation between external stimuli and error detector measurements.

Table 35. Control input characteristics for M8043A.

Parameter	Value
Input voltage range	–1 V to +3 V
Termination voltage range	–1 V to +3 V
Termination voltage accuracy	± 25 mV ± 1 %
Threshold	Range: –1 V to +3 V Accuracy: ± 50 mV typical
Response time	In pattern capture mode: 64 GBd: ~ 30 ns (measured) up to < 0.7 µs (measured) at 2 GBd In pattern sequencer control mode: 64 GBd: ~ 2.5 µs (measured) 2 GBd: ~ 2.5 µs to 3.2 µs (measured)
Input impedance	50 Ω (nom.)
Connector type	SMA, female

Control Output (Ctrl Out)

The Control Output (Ctrl Out) provides status and event signaling from the M8043A error detector to external equipment. It can be used to indicate error conditions or to generate programmable output signals for test automation and synchronization.

When configured for error signaling, the Ctrl Out outputs a pulse upon the detection of a bit error. This enables real-time error indication and can be used to trigger external instruments, capture devices, or system-level monitoring functions.

When controlled by the internal sequencer, the Ctrl Out can be configured to generate either a pulse or a static logic high or low level. This allows the Control Output to be used as a flexible marker or control signal, for example to indicate measurement states, sequence events, or pass/fail conditions within automated test setups.

The Control Output supports tight integration of the M8043A into complex and automated test environments by providing deterministic, externally observable measurement events.

Table 36. Control output characteristics.

Parameter	Value
Amplitude	Range: 0.1 to 2 V Accuracy: ± 10 mV ± 2 % typical
Output voltage range	–0.5 to 1.75 V
Delay from data input	64 Gbps NRZ: ~ 1 µs ± 30 ns (measured) 2 Gbps NRZ: ~ 4 µs ± 0.7 µs (measured) For PAM4 line coding values are slightly smaller
Output impedance	50 Ω (nom.)
Connector type	SMA, female

Communication Link (LINK)

The Communication Link (LINK) interface is reserved for future use. It is currently not enabled and has no functional role in the present operation of the M8043A.

Calibration Output (Cal Out)

The Calibration Output (Cal Out) is used exclusively for factory calibration procedures at Keysight facilities. This output is not intended for customer use and is not supported in user test setups or field calibration.

Measurement Capabilities

Table 37. Measurement capabilities for the M8043A and M8046A when used with the M8042A pattern generator. For measurements with the UXR-based error analysis see the table below.

Measurement	Parameters	M8070B Baseline	M8070ADVB Plugin	M8070EDAB Plugin
BER, SER	Accumulation and instantaneous	Yes	Not applicable	Not applicable
Jitter tolerance		No	Yes	Not applicable
Counters	Compared bits, errored bits Compared 0 bits, errored 0 bits Compared 1 bit, errored 1 bit Compared symbols, errored symbols Compared symbols 0, 1, 2, 3 Errored symbols 0, 1, 2, 3	Yes	Not applicable	Not applicable
BER Scan with RJ, DJ separation		No	Yes [1]	Not applicable
Output level and Q-factor		No	M8043A: Yes. NRZ only. M8046A: No	Not applicable
Sampling point view		Yes	Not applicable	Not applicable
BER versus parameter automated sweep		No	Yes	Not applicable
BER Based Deemphasis	Optimize PG de-emphasis to minimize BER (via error analyzer or DCI)	No	Yes	Not applicable
Error distribution analysis	See M8070EDAB details below.	No	No	M8043A: Yes M8046A: Yes
Pattern capture		Yes	Not applicable	Not applicable
Masking	Expected bits can be masked during error counting. >Bitwise and block-wise masking is possible.	Yes	Not applicable	Not applicable
Eye diagram, histogram based		No	M8043A: Yes. PAM4 and NRZ M8046A: No	Not applicable
Eye diagram, BER based		No	M8043A: Yes. NRZ only M8046A: No	Not applicable

1. The measurement is available in the user interface, but just for debugging/troubleshooting purposes. The accuracy of jitter separation results is unspecified in the case of NRZ and invalid in case of PAM4 signals.

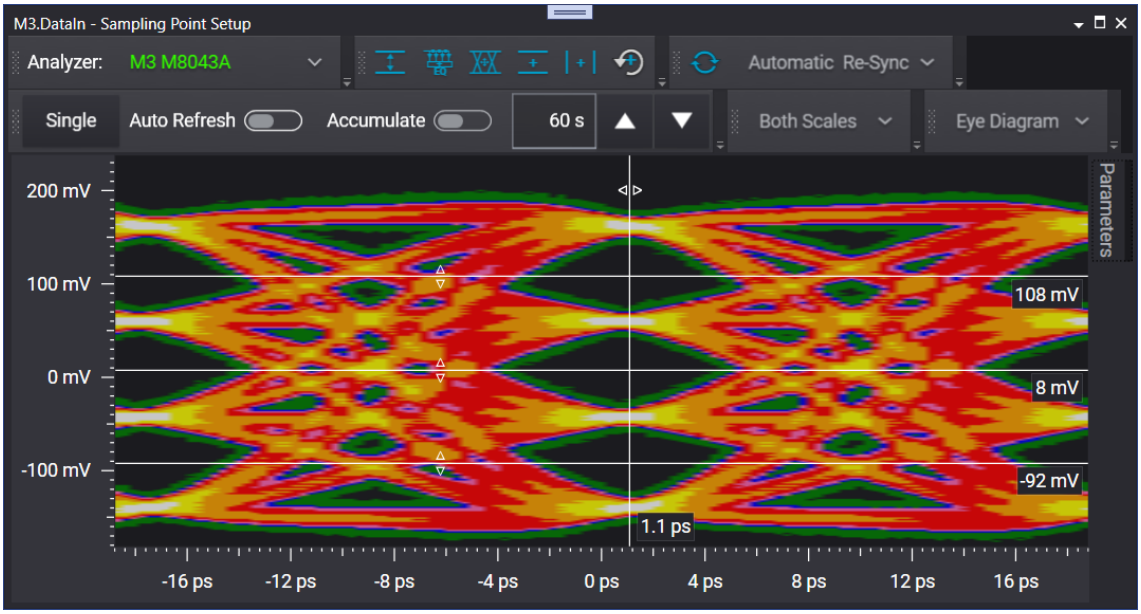


Figure 32. You can monitor the eye diagram based on a histogram with M8043A and the M8070ADVB measurement package. The example shows a 53.125 GBd PAM4 signal from a direct loopback to the pattern generator M8042A.

Error Analysis Above 64 GBd Using Infiniium UXR-Series Oscilloscopes

For symbol-pattern error analysis up to 64 GBd, the M8043A error analyzer module can be used. For symbol rates up to 58 GBd with support for PCIe® interactive link training, the M8046A error analyzer module is available.

For symbol rates above 64 GBd, the M8000 system software (M8070B) supports the use of Keysight Infiniium UXR-Series real-time oscilloscopes. In this configuration, the oscilloscope captures the high-speed waveform, which is then decoded into a pattern stream. The M8000 system software uploads the acquired data, performs pattern synchronization, and compares the received data against the expected pattern, including long PRBS polynomials such as PRBS31Q.

This approach enables measurement of target BERs down to approximately 10^{-6} to 10^{-7} at symbol rates up to 224 GBd within typical measurement times of around one minute. The Infiniium UXR-Series oscilloscope provides highly configurable equalization and integrated clock recovery supporting symbol rates up to 224 GBd. Pattern-based equalization is also supported, allowing users to define a known pattern and optimize equalization parameters for accurate high-baud-rate error analysis.

Typical key capabilities of the Infiniium UXR-Series real-time oscilloscopes include:

- **Analog bandwidth:** Up to **110 GHz**, enabling direct capture of ultra-high-speed serial signals.
- **Real-time sampling rate:** Up to **256 GSa/s**, providing high time resolution for accurate waveform reconstruction and jitter analysis.

- **ADC resolution:** High-resolution **10-bit** ADC architecture, supporting improved vertical resolution and better noise performance.
- **Integrated clock recovery:** Built-in clock recovery supporting symbol rates up to **224 GBd**, suitable for NRZ and PAM4 signaling.
- **Advanced equalization:** Configurable CTLE, FFE, and decision-feedback equalization (DFE), including pattern-based equalization, optimized for very high baud rates.
- **Deep acquisition memory:** Supports long record lengths (up to **2 Gpoints**) to enable sustained BER measurements, rare-event analysis, and decoding of long PRBS sequences.

These capabilities make the Infiniium UXR-Series oscilloscopes well suited for extending M8000-based error analysis beyond 64 GBd while maintaining deterministic pattern comparison and BER measurement at extreme data rates.

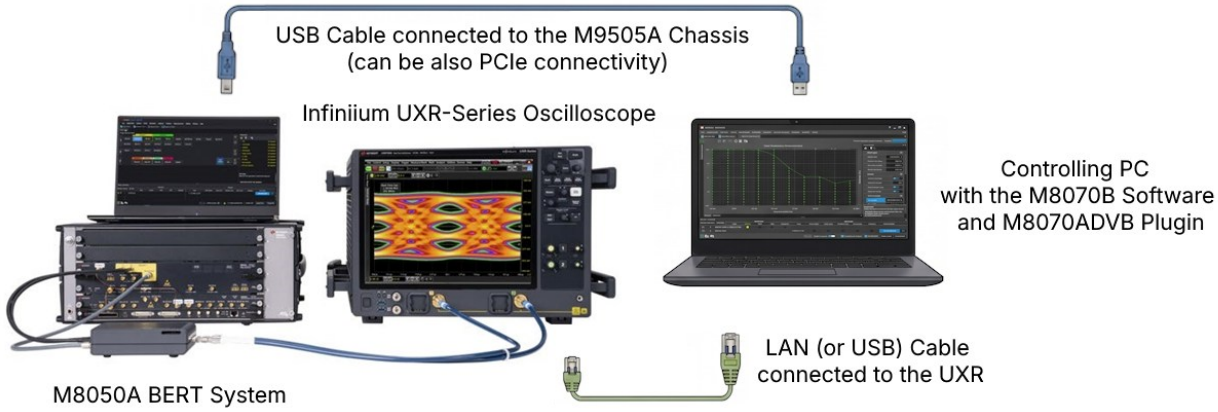


Figure 33. The M8070ADVB controls the UXR-Series oscilloscope and uploads the decoded pattern streams for synchronization and comparison with expected patterns.

Table 38. Conditions for error analysis with M8070ADVB using a real-time oscilloscope.

Parameter	Value
Supported real-time oscilloscope models	Keysight UXR-Series, all models from 59 to 110 GHz (2 or 4 channels), A, B, AP, and BP model numbers
Symbol rates	Maximum symbol rate is limited by the UXR model: 14 GBd to 60 GBd for UXR03344A or B 14 GBd to 60 GBd for UXR0402/4A, AP, B, or BP 14 GBd to 75 GBd for UXR0502/4A or B 14 GBd to 96 GBd for UXR0592/4A, AP, B, or BP 14 GBd to 105 GBd for UXR0702/4 A, AP, B, or BP 14 GBd to 160 GBd for UXR0802/4A or B 14 GBd to 180 GBd for UXR0802/4A or B with the 90 GHz bandwidth upgrade 14 GBd to 200 GBd for UXR1002/4A or B 14 GBd to 224 GBd for UXR1102/4A or B
Hardware acceleration	Hardware acceleration is active for 256 GSa/s UXR models when parameters are set in the M8070B with M8070ADVB to meet all of the following conditions: Symbol rate: 51.2 GBd to 224 GBd CDR type: 2nd order PLL CDR loop bandwidth:

Parameter	Value
	Symbol rate / 2655 to Symbol rate / 500 Measurements are: 1.8 times faster (meas.) for JTOL measurements 2.5 to 3.5 times faster (meas.) for BER measurements When hardware acceleration is active. Display shall be turned OFF to achieve fastest measurement times. Factor of acceleration depends on parameter settings of the UXR such as e.g., line coding, baud rate, bits per acquisition and is provided as an estimation.
Target BER	Hardware acceleration active: ~10^{-7} Hardware acceleration inactive: ~10^{-6}
Coding	NRZ, PAM4, PAM6, and PAM8
Pattern capture	Yes
Masking	Expected bits can be masked (ignored) during error counting. Bitwise and block-wise masking is possible.
Expected patterns	User definable: PRBS 2^n-1 with n = 7, 9, 10, 11, 13, 15, 23, 31, 33, 35, 39, 41, 45, 47, 49, 51 Memory patterns with max. pattern length of 256 kbit
Measurements	Jitter tolerance, BER and SER Error distribution analysis (restrictions with respect to memory depth of UXR to be able to capture maximum frame length may apply) Automated parameter sweep versus BER
Measurement time	Depends on: • Expected pattern type • Expected pattern length (in case of memory patterns) • Symbol rate • Equalizer usage and parameters • Acquisition depth in UI • Target BER and confidence level
BER and symbol counters	BER counters: • Compared bits • Errored bits • Compared 0 bits, compared 1 bit • Errored 0 bits, errored 1 bit Symbol counters: • Compared symbols • Errored symbols • For each symbol level: • Compared symbols • Errored symbols
Error distribution statistics	Yes, for details see table 41. Requires M8070EDAB license.
Parameters	• Acquisition ○ Number of bits per acquisition. (Note: The maximum number of bits per acquisition is limited by the oscilloscope's acquisition memory depth, symbol rate and clock recovery setting.) ○ Global acquisition bandwidth limit ○ Channel bandwidth limit and filter type ○ Pattern capture up to 100 Mbit • Horizontal reference clock: internal, external 10 MHz and 100 MHz • Clock: Follow Sys Clock, symbol rate • Line Coding: ○ Coding (NRZ, PAM4, PAM6, PAM8)

Parameter	Value
	○ Symbol mapping (uncoded, Gray, custom) ○ Custom symbol mapping • Comparator: ○ Compare mode (single-ended / differential) ○ Polarity (non-inverted / inverted) ○ Auto-set thresholds ○ User-defined thresholds • Equalizer ○ FFE - Number of taps and pre-taps ○ FFE - Auto-set coefficients ○ CTLE - DC gain ○ CTLE - Frequency pole #1, Frequency pole #2, ○ CTLE - Frequency zero #1 ○ DFE- Taps ○ DFE - Auto-set coefficients • Clock Recovery (2nd Order CR) ○ Loop bandwidth ○ Symbol rate divider ○ Damping factor ○ Sample delay (PAM4 only) • Auto alignment ○ Covers thresholds, sample delay and equalizer coefficients • Automatically set scope parameters: ○ Thresholds ○ FFE coefficients (cannot be changed by user) ○ Sample delay position (in case of NRZ)
Software pre-requisites	UXR: Infiniium version 11.40.00202 or higher M8070B: M8000 system software. See table 41 for minimum required software revision M8070ADVB advanced measurement package software. See table 41 for minimum required software revision.
Measurement packages	Following licenses are required on the oscilloscope in addition: D9020PAMA or D9320PAMA Pulse Amplitude Modulation PAM-N analysis software D9020ASIA or D9320ASIA Advanced signal integrity software (Equalization, InfiniiSim, Crosstalk Analysis)
Controlling connection to UXR	LAN recommended

User Interface and Remote Control

M8070B System Software Overview

The Keysight **M8070B system software** is the central control, configuration, and analysis platform for the M8000 series Bit Error Ratio Test (BERT) systems including the M8050A BERT platform. It provides a unified user interface and software framework for controlling pattern generators, error analyzers, clock modules, interference sources, and associated instruments within the M8000 ecosystem.

Designed for high-speed digital and optical interconnect validation, the M8070B supports symbol rates from low-speed applications up to 224 GBd, covering NRZ and PAM4 signaling, and enabling comprehensive physical-layer and link-layer test workflows.

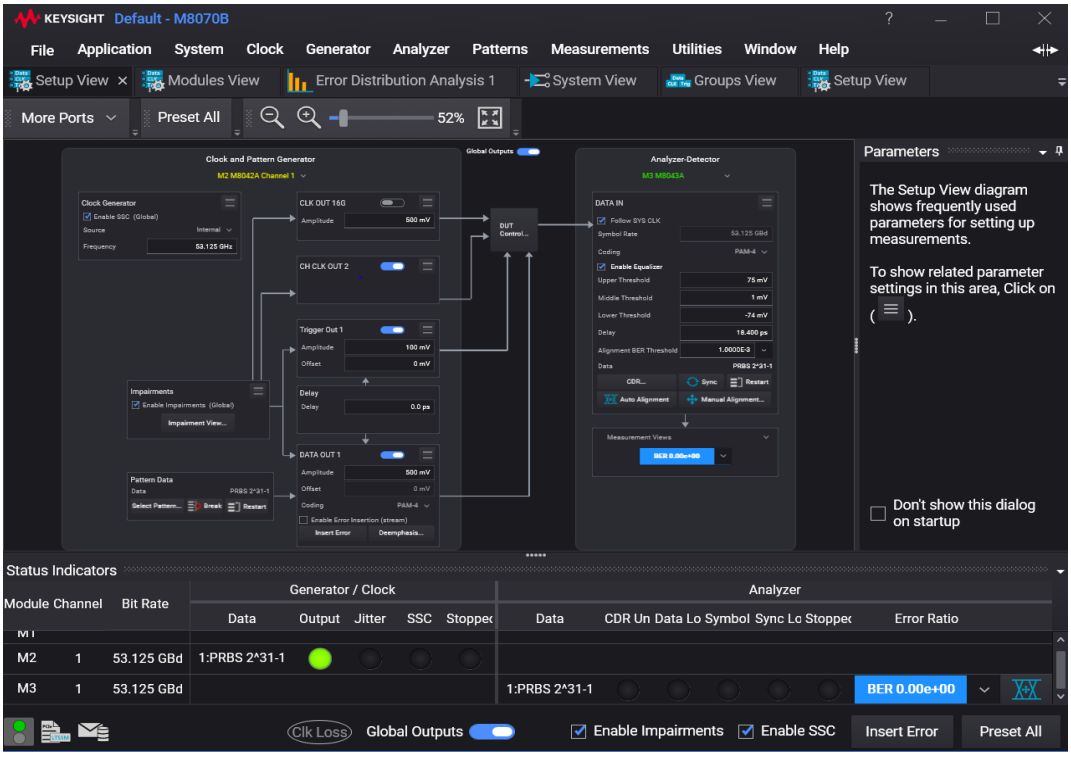


Figure 34. The M8070B system software is required to control the M8050A BERT. The user interface provides control of all parameters. It provides a graphical user interface and remote control via SCPI. Shown is the setup view with the M8009A clock module, M8042A pattern generator module, and M8043A error detector module.

Unified Instrument Control and Test Configuration

The M8070B software offers a single, coherent environment for configuring complex BERT test setups. It manages instrument discovery, parameter configuration, synchronization, and timing alignment across all connected M8000 modules and supported external instruments.

Key configuration capabilities include:

- Pattern selection and sequence control

- Error detector configuration and BER measurement setup
- Clocking, triggering, and synchronization control
- Interference and noise source coordination
- Equalization and de-embedding configuration

Pattern-Based BER Analysis and Measurement Automation

The M8070B supports advanced pattern-based BER measurements using hardware error analyzers as well as real-time oscilloscopes for very high symbol rates. The software handles pattern alignment, synchronization, and comparison against the expected data stream, including long PRBS sequences such as PRBS31Q.

Integrated automation features include:

- Sequencer-based test execution
- Measurement state control and conditional branching
- Automated sweeps and stress conditions
- Deterministic triggering and event handling

High-Speed Equalization and Channel Compensation

To support reliable error analysis across lossy and impaired channels, the M8070B provides software control of advanced equalization and compensation functions. This includes configuration of transmitter and receiver equalization, backchannel de-embedding, and pattern-aware optimization.

The software supports:

- Control of FIR, FFE, and CTLE-based equalization
- Channel response measurement and coefficient calculation
- Compensation of channel loss, skew, and dispersion
- Pattern-based equalization optimization at very high symbol rates

Support for External Instruments and Extended Baud Rates

For symbol rates beyond the capability of hardware error analyzers, the M8070B seamlessly integrates with Keysight Infiniium real-time oscilloscopes, including the UXR-Series. In this configuration, captured waveforms are decoded into pattern streams and analyzed by the M8070B using the same pattern-based BER framework.

Scalable Architecture and Future-Ready Design

The M8070B system software is designed as a scalable and modular platform, supporting current and future M8000 hardware modules and applications. Software options enable expansion from basic BER testing to advanced jitter tolerance, link training, and stress testing scenarios.

Its architecture supports:

- Multi-module and multi-channel test configurations
- Future feature and standard support via software updates
- Integration into automated test systems and lab environments

Table 39. User interface and remote-control interface via the M8070B.

Parameter	Value
Programming language	SCPI
Remote control interface	LAN
Save/Recall	Yes
Software update	Under the help menu the M8070B can show if there are newer SW revisions of M8070B, M8070ADVB, M8070EDAB, M8070ISIB, and M8042A, M8009A, M8043A module driver packages available for download from K.com.
SCPI recorder	Allows recording of the SCPI commands that correspond to the interactive control in the GUI. This includes: Parameter changes Sequence and pattern configuration Measurement creation, configuration and execution Group configuration Save and recall of settings The recorded SCPI commands can be copied to the clipboard or saved to a file for later playback.
Software download	For latest version of the M8050A module drivers see: https://www.keysight.com/nl/en/support/M8050A/120-gbd-high-performance-bert.html#drivers For latest version of the M8070B system software see: https://www.keysight.com/nl/en/lib/software-detail/computer-software/m8070b-system-software-3021035.html
Offline version	Yes. M8070B can be used without any M8000-series hardware connected to the controlling PC in order to simulate different module configurations.
License types	Not licensed. Free baseline software.

M8070ADVB Advanced Measurement Package

The M8070ADVB Advanced Measurement Package extends the M8000 system with advanced measurement capabilities for high-speed serial link analysis. It provides measurements such as jitter tolerance, CDR-related analysis, and advanced BER-based characterization, enabling in-depth evaluation of receiver robustness and system margins under stressed conditions.

The package supports automated measurement workflows and close interaction with M8000 hardware modules for detailed physical-layer validation.

Table 40. Features of the advanced measurement software package M8070ADVB.

Parameter	Value
Measurements	See table 37 for the measurement capabilities
Export of measurement results	Jitter tolerance results as *.csv file
Controlling other instruments via M8070B	Real-time oscilloscopes, e.g. Infiniium Z-Series and UXR-Series. DCA sampling oscilloscopes, e.g. N1000A with N1046A, N1060A, N1094A/B, 86108B modules or DCA-M N1092C/D, N1093A/B, etc.
Scripting interface	The built-in scripting engine is based on IronPython. It enables the control of the device under test as well as another test equipment. Function hooks are available to tailor your measurements, such as read-out of built-in error counters or initializing the device

Parameter	Value
DUT control interface (DCI)	Enables access to built-in error counters and status registers of a device under test (BIST) for use with automated measurements like accumulated BER and jitter tolerance. Can also be used to customize the measurements to DUT specific needs. IronPython scripting and .net libraries are supported to interface with the DUT
Auto-optimizing de-emphasis taps (refer to the “Automatic de-emphasis optimization” section of this datasheet)	De-emphasis taps are calculated for the best eye height. Output levels are adjusted to the measured amplitude on the reference plane. If necessary, external attenuators can be considered adjusting higher voltages. Can be combined with embedding/de-embedding of S-parameter files.
Software download	For the latest version see: https://www.keysight.com/nl/en/lib/software-detail/computer-software/m8070advb-advanced-measurement-package-for-m8000-series-of-bert-test-solutions-3019474.html
License types	You can choose between node-locked, transportable, perpetual license, network, USB-dongle license types with different terms such as perpetual or 6/12/24-month subscriptions. The network license is only recommended when using multiple M8050A setups within one company.

M8070EDAB Error Distribution Analysis Package

The M8070EDAB Error Distribution Analysis Package enables detailed analysis of where and how errors occur within a received data stream. It provides statistical evaluation of error distributions in time, phase, and symbol position, allowing correlation of error events with jitter, noise, and signal impairments. This package is used for root-cause analysis of BER degradation and for identifying systematic error mechanisms in high-speed links.

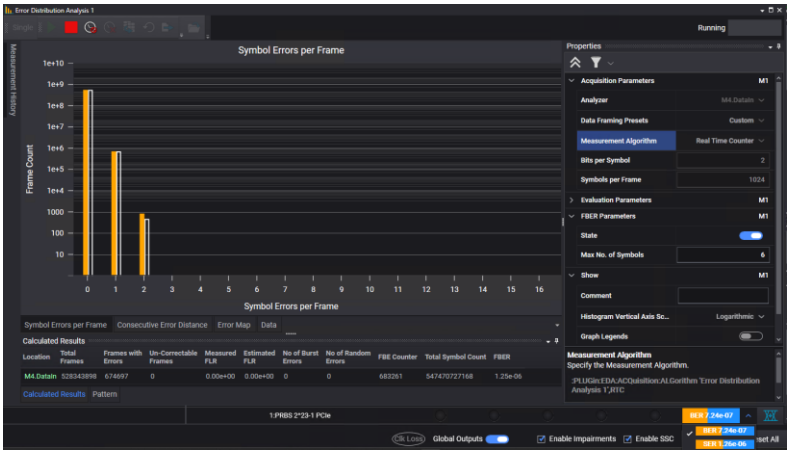


Figure 35. Error distribution analysis: PCIe 6.0 64 GT/s BER & FBER measurements before FEC Decoding.

Table 41. Features of the error distribution analysis package M8070EDAB.

Parameter	Value
Measurements	Frame loss ratio estimation (real-time update with M8046A & M8043A) Error map Symbol-errors per frame distribution (real-time with M8046A and M8043A)- Consecutive error distance distribution Error burst count, capture and analysis M8046A and M8043A) FBER Counter

Parameter	Value
Supported hardware	M8043A and M8046A Infiniium UXR-Series real-time oscilloscope (in combination with M8070ADVB plugin)
Software download	For latest version see: https://www.keysight.com/nl/en/lib/software-detail/computer-software/m8070edab-error-distribution-analysis-package-for-m8000-series-ber-test-solutions-3020058.html
License types	You can choose between node-locked, transportable, perpetual license, network, USB-dongle license types with different terms such as perpetual or 6/12/24-month subscriptions. The network license is only recommended when using multiple M8050A setups within one company.

System Requirements

Table 42. System requirements for M8050A and M8070B System Software.

Parameter	Value
M9537A 1-slot AXIe embedded controller requirements	Choose M8050A-BU3 or -BU5 for a pre-installed embedded controller M9537A including pre-installation of M8070B software and module licenses. M8050A-BU3 and -BU5 are pre-configured with Windows 10 IoT Enterprise. Otherwise: M9537A 1-slot AXIe embedded controller, choose options for Windows 10 IoT Enterprise, 8 or 16 GB RAM, SSD.
External PC	Connection to AXIe chassis: • USB 2.0 (Mini-B) recommended or • PCIe 2.0/8x for highest data throughput Memory: Minimum of 8 GB RAM recommended
Operating system	Windows 10 IoT Enterprise, Windows 11
Display resolution	Minimum requirement 1024 x 768
Software pre-requisites	Keysight IO Libraries Suite: Version 2024 Update 2 Build 21.1.17 or newer M9505A AXIe 5-slot chassis firmware: Version 2.1.6 or newer M9502A AXIe 2-slot chassis firmware: Version 2.1.6 or newer M8070B: Version 12.5 or newer M8070ADVB: Version 1.14.110.4 or newer M8070EDAB: Version 1.13.120.6 or newer M8070ISIB: Version 1.4.370.4 or newer M8042A module driver: Version 5.5 or newer M8009A module driver: Version 5.5 or newer M8043A module driver: Version 5.5 or newer

Automated Receiver Test Software

To simplify the compliance testing and characterization of high-speed digital receiver test, Keysight provides automated receiver test software for various electrical and optical interface standards to be used in addition to the M8070B system software.

Here is an overview of test automation software solutions available supporting the M8050A high-performance BERT or any of its modules.

Standard	Medium/Interface	Interface Variants	Test Automation Software
IEEE 802.3bs/cd	Electrical Chip-to-module (C2M), Chip-to-chip (C2C), Backplane (KR), copper cable (CR)	400GAUI-8 200GAUI-4 50GBASE-KR/CR 100GBASE-KR2/CR2 200GBASE-KR4/CR4	**M8091BSCB** (both the M8042A pattern generator and M8043A error detector are supported from the M8050A BERT platform)
IEEE 802.3bs/cd/db	Optical	200GBASE-FR4/-LR4/-DR4 400GBASE-FR8/-LR8/-DR4 50GBASE-FR/-LR/-SR 100GBASE-DR 100/200/400GBASE-SR/SR2/SR4 and MSAs	**N4917BSCB** (only the M8043A error detector from the M8050A BERT platform; M8045A pattern generator is supported from the M8040A platform)
IEEE 802.3ba	Optical receiver stress test (ORST)	100GBASE-SR4/LR4/ER4 and MSAs	**N4917BACA** (only the M8043A error detector from the M8050A BERT platform supported; M8045A pattern generator is supported from the M8040A platform)
IEEE 802.3ck (Draft 3.3)	Electrical Chip-to-module (C2M), Chip-to-chip (C2C)	Chip-to-Chip (C2C) 100GAUI-1, 400GAUI-4 Chip-to-Module (C2M) host and module input	**M8091CKCA** (both the M8042A pattern generator and M8043A error detector are supported from the M8050A BERT platform)
OIF CEI 4.0	Electrical Module-to-Host, Host-to-Module	OIF-CEI 56G-VSR-PAM4 OIF-CEI 56G-MR-PAM4 OIF-CEI 56G-LR-PAM4	**M809256CA** (no M8050A modules are supported. Refer to the M8040 BERT).
IEEE 802.3dj	Electrical Chip-to-module (C2M), Chip-to-chip (C2C), Backplane (KR), Copper cable (CR)	200GAUI-1 C2C 200GAUI-1 C2M 200GBASE-KR1 200GBASE-CR1 (can be also used for UALink 1.0)	**M8091DJCA** (only the M8042A pattern generator from the M8050A BERT platform supported)
IEEE 802.3dj/cu/cn	Optical receiver stress test (ORST)	100GBASE-SR 400GBASE-SR4 100GBASE-DR/-FR1/-LR1 400G-FR4/-LR4-6 400GBASE-DR4 200GBASE-DR1 1.6TBASE-DR8 800GBASE-FR4-500 800GBASE-FR4 and LR4	**N4917DJCA** (both the M8042A pattern generator and M8043A error detector are supported from the M8050A BERT platform)
OIF-CEI 5.0 OIF-CEI-LINEAR LPO-MSA	Electrical Module-to-Host, Host-to-Module	CEI-112G-MR-PAM4 CEI-112G-LR-PAM4 CEI-112G-VSR-PAM4 CEI-112G-LINEAR-PAM4	**M809212CA** (both the M8042A pattern generator and M8043A error detector

		100G-DR-LPO	are supported from the M8050A BERT platform)
PCI Express 5.0 Base Specification	Electrical ASIC Endpoint, Root complex	2.5, 5.0, 8.0, 16.0, 32.0 GT/s	**N5991PB5A** (only the M8042A pattern generator from the M8050A BERT platform supported; M8046A error detector is supported from the M8040A platform)
PCI Express 5.0 CEM Specification	Electrical CEM Add-in card, System	2.5, 5.0, 8.0, 16.0, 32.0 GT/s	**N5991PC5A** (only the M8042A pattern generator from the M8050A BERT platform supported; M8046A error detector is supported from the M8040A platform)
PCI Express 5.0 M.2 specification	Electrical M.2 connectorized devices	8.0, 16.0, 32.0 GT/s	**N5991PM5A** (only the M8042A pattern generator from the M8050A BERT platform supported; M8046A error detector is supported from the M8040A platform)
PCI Express 6.4 Base Specification	Electrical ASIC Endpoint, Root complex	2.5, 5.0, 8.0, 16.0, 32.0, 64.0 GT/s	**N5991PB6A** (only the M8042A pattern generator from the M8050A BERT platform supported; M8046A error detector is supported from the M8040A platform)
PCI Express 6.4 CEM Specification	Electrical CEM Add-in card, System	2.5, 5.0, 8.0, 16.0, 32.0, 64.0 GT/s	**N5991PC6A** (only the M8042A pattern generator from the M8050A BERT platform supported; M8046A error detector is supported from the M8040A platform)
PCI Express 7.0 Base Specification	Electrical ASIC Endpoint, Root complex	PCIe 128 GT/s	**N5991PB7A** (only the M8042A pattern generator from the M8050A BERT platform supported)
USB 3.2	Electrical device, host, redriver, retimer	USB 3.2 Gen1×1 – 5 Gbps USB 3.2 Gen2×1 – 10 Gbps USB 3.2 Gen1×2 – 10 Gbps USB 3.2 Gen2×2 – 20 Gbps	**N5992U32A** (only the M8042A pattern generator from the M8050A BERT platform supported; M8046A error detector is supported from the M8040A platform)
USB4 Version 2.0	Electrical router assembly	USB4 Gen2 – 10 Gbps NRZ USB4 Gen3 – 20 Gpbs NRZ USB4 Gen4 – 25.6 GBd PAM3 + asymmetric link Thunderbolt™ 3 compatible:	**N5992U42A** (only the M8042A pattern generator from the M8050A BERT platform supported)

		Gen2 – 10.3125 Gbps Gen3 – 20.625 Gbps	
DisplayPort 2.1	Electrical Sink	RBR – 1.62 Gbps per lane HBR – 2.70 Gbps per lane HBR2 – 5.40 Gbps per lane HBR3 – 8.10 Gbps per lane UHBR10 – 10.0 Gbps per lane UHBR13.5 – 13.5 Gbps per lane UHBR20 – 20 Gbps per lane	**N5992DP2A** (only the M8042A pattern generator from the M8050A BERT platform supported)

General Characteristics and Physical Dimensions

General Characteristics for the M8050A System

Table 43. General characteristics for M8042A, M8009A modules and M8058A, M8059A remote heads.

Parameter	Value
Operating temperature	For configurations using M8009A-062: 5 °C to 40 °C For configurations using M8009A-061: 5 °C to 35 °C
Storage temperature	–40 to +70 °C
Operating humidity	15 to 95% relative humidity at 40 °C (non-condensing)
Storage humidity	24 to 90% relative humidity at 65 °C (non-condensing)
Operating altitude	Up to 2000 m
Physical dimensions	See tables below
Weight net	See tables below
Weight shipping	See tables below
Power consumption	See tables below
Interface to controlling PC	PCIe or USB or Thunderbolt
Recommended recalibration period	2 years
Warm-up time	30 minutes
Cooling requirements	Slot air flow direction is from right to left. When operating the M8050A choose a location that provides at least 80 mm of clearance at each side. See also start-up guide for M9505A chassis.
EMC tested acc. to	IEC 61326-1
Safety tested acc. to	IEC61010-1, ANSI/UL61010, CSA22.2 No. 61010-1
Quality management	ISO 9001, 14001

Physical Dimensions / Power Requirements for M8042A

Table 44. Physical dimensions and power requirements of the M8042A pattern generator module.

Parameter	M8042A-0G1 (1 channel version)	M8042A-0G2 (2 channel version)
Form factor	2-slot AXIe module	3-slot AXIe module
Physical dimensions (W x H x D)	351 mm x 61 mm x 315 mm	351 mm x 92 mm x 315 mm

Parameter	M8042A-0G1 (1 channel version)	M8042A-0G2 (2 channel version)
Power requirements	300 W (nom.)	600 W (nom.)
Weight net	6.1 kg	8.5 kg
Weight shipping	9.6 kg	12.0 kg

Physical Dimensions for M8058A and M8059A

Table 45. Physical dimensions of the M8058A and M8059A generator remote heads.

Parameter	Value
Physical dimensions (W x H x D)	157 mm x 90 mm x 44 mm (remote head without cables) ~810 mm x 90 mm x 44 mm (remote head with cables) Length of cable connection between M8058A/59A and M8042A module: ~500 mm Length of M8058A/M8059A: 157 mm Length of cable between M8058A/M8059A and DUT: ~150 mm
Weight net	1.0 kg
Weight shipping	Shipment of one Remote Head 3.7 kg Shipment of two Remote Heads 4.7 kg

M8042A ~500 mm cable M8058A ~150 mm, 1.85 mm cable

M8042A ~500 mm cable M8059A ~150 mm, 1.00 mm cable

Physical Dimensions for M8068A and M8069A

Table 46. Physical dimensions and power requirements of the M8068A and M8069A generator remote heads

Parameter	Value
Physical dimensions (W x H x D)	157 mm x 101 mm x 59 mm (remote head without cables) ~810 mm x 101 mm x 59 mm (remote head with cables) Length of cable connection between M8068A/69A and M8042A module: ~500 mm Length of M8068A/M8069A: 157 mm Length of cable between M8068A/M8069A and DUT: ~150 mm
Weight net	1.3 kg
Weight shipping	Shipment of one Remote Head 4.0 kg Shipment of two Remote Heads 5.0 kg

M8042A ~500 mm cable M8068A ~150 mm, 1.85 mm cable

Parameter	Value

M8042A ~500 mm cable M8069A ~150 mm, 1.00 mm cable

Physical Dimensions / Power Requirements for M8009A

Table 47. Physical dimensions and power requirements of the M8009A clock module.

Parameter	Value
Form factor	1-slot AXIe module
Physical dimensions (W x H x D)	351 mm x 30 mm x 315 mm
Power requirements	200 W (nom.)
Weight net	3.9 kg (meas.)
Weight shipping	7.5 kg (meas.)

Physical Dimensions / Power Requirements for M8043A

Table 48. Physical dimensions and power requirements of the M8043A analyzer module.

Parameter	Value
Form factor	2-slot AXIe module
Physical dimensions (W x H x D)	351 mm x 60 mm x 305 mm
Power requirements	320 W (nom.), includes power for M8052A remote head
Weight net	4.8 kg (meas.)
Weight shipping	9.8 kg (meas.)

Physical Dimensions for M8052A

Table 49. Physical dimensions and power requirements of the M8052A analyzer remote head

Parameter	Value
Physical dimensions (W x H x D)	160 mm x 85 mm x 45 mm (remote head without cables) ~810 mm x 85 mm x 45 mm (remote head with cables) Length of cable between M8043A and M8052A module: ~500 mm Length of M8052A: 160 mm Length of cable between M8052A and DUT: ~150 mm
Weight net	1.0 kg, including cables
Weight shipping	3.5 kg

M8043A ~500 mm, 1.85 mm cable M8052A ~150 mm, 1.85mm cable

Physical Dimensions for M8050A-BU2, -BU3, -BU4, and -BU5 Bundles with AXIe Chassis

Table 50. Physical dimensions and power for M8050A bundles with AXIe chassis.

Parameter	Value
Form factor	Modules are pre-installed in M9505A 5-slot AXIe chassis
Physical dimensions (W x H x D)	Depth including semi-rigid cables without remote heads: M8050A-BU2 / -BU3: 462 mm x 193 mm x 485 mm M8050A-BU4 / -BU5: 462 mm x 384 mm x 485 mm
Weight net	Without modules, without packaging material, without filler panels: M8050A-BU2: 13.3 kg (M9505A) M8050A-BU3: 2.9 kg (M9537A) +13.3 kg (M9505A) M8050A-BU4: 26.6 kg (2 x M9505A) M8050A-BU5: 2.9 kg (M9537A) + 26.6 kg (2 x M9505A)
Weight shipping	Weight per system package only (wo chassis, wo modules) M8050A-BU2 / -BU3: 12.3 kg M8050A-BU4 / -BU5: 24.6 kg (2 x M8050A-BU2)

Figure 36. M9505A 5-slot AXIe chassis with embedded system module and USB 2.0 or PCIe Gen2, x8 link to external controlling PC (included in the BU2, BU3, BU4, BU5 bundles).

Other Keysight AXIe chassis, not included in the M8050A bundles, can be also ordered separately and used with the M8050A modules. Please refer to their datasheets and requirements to ensure successful connectivity with your controlling PC.

Figure 37. Other AXIe chassis: M9502A 2-slot AXIe chassis (left), M9506A high-performance 5-slot AXIe chassis with PCIe Gen3 and Thunderbolt connectivity interfaces, 300W per slot, and GPS option.

Specification Definitions

Unless otherwise stated, all outputs must be terminated with **50 Ω (Ohm) to ground (GND)**.

Unless otherwise specified, all the **M8042A** specifications are valid at the output of the remote heads and at the end of the matched reference cable pair. The applicable reference cable is the **M8058A-801** when used with the M8058A or M8068A remote head, and the **M8059A-801** when used with the M8059A or M8069A remote head.

Unless otherwise specified, all **M8043A** specifications are valid when using the recommended matched cable pair **M8058A-801** (length 150 mm, 1.85 mm connectors).

Specification (spec.)

Warranted performance of a calibrated instrument that has been stored for a minimum of 2 hours within the operating temperature range of **0 °C to 40 °C** and after a **15-minute warm-up period**. Specifications are valid within **±10 °C** following auto-calibration. All specifications include measurement uncertainty and are established in compliance with **ISO 17025** methods. Performance values in this document are specifications only where explicitly identified as such.

Typical (typ.)

Characteristic performance that **80 % or more** of manufactured instruments are expected to meet. Typical values are **not warranted**, do not include measurement uncertainty, and are valid only at **room temperature (approximately 23 °C)**.

Nominal (nom.)

The mean or average characteristic performance, or a value defined by design, such as connector type, physical dimension, or operating speed. Nominal values are **not warranted** and are measured at **room temperature (approximately 23 °C)**.

Measured (meas.)

A parameter measured during development to indicate expected performance. Measured values are **not warranted** and are valid only at **room temperature (approximately 23 °C)**.

Accuracy

Represents the traceable accuracy of a specified parameter. Accuracy includes measurement error, time-base error, and calibration source uncertainty.

Related Keysight Literature

Description	Publication Number
Product Datasheets and Technical Overviews	
XE8-class M8050A High-Performance BERT 120 GBd – Configuration Guide	3122-1285.EN
XE8-class M8040A High-Performance BERT 64 GBd – Data Sheet	5992-1525EN
XE8-class M8020A High-Performance BERT 32 Gbps – Data Sheet	5991-3647EN
M8053A Interference Source 64 GHz – Data Sheet	3124-1184.EN
M8054A Interference Source 32 GHz – Data Sheet	5992-3917EN
M8049A ISI Channel Boards – Data Sheet	5992-3617EN
M8067A ISI Channel Boards – Data Sheet	3122-2261.EN
M9502A and M9505A 2- and 5-slot AXIe Chassis – Data Sheet	5990-6584EN
M9506A High-Performance 5-slot AXIe Chassis – Data Sheet	5992-3786EN
M9537A AXIe Embedded Controller – Data Sheet	5992-1530EN
M9538A AXIe Embedded Controller – Data Sheet	3125-1003.EN
M8047C PCIe Redriver for 32 GBd – Data Sheet	3124-1732.EN
N7718C Optical Reference Transmitter – Data Sheet	3124-1652EN
Infiniium UXR-Series Oscilloscopes – Data Sheet	5992-3132EN
N1000A DCA-X Sampling Oscilloscope Platform – Data Sheet	5992-3271EN
Test Automation Software Datasheets	
N5991DP2A DisplayPort 2.1 Receiver Test Automation Software – Data Sheet	3124-1689.EN
N5991U42A USB4 Version 2.0 Receiver Test Automation Software – Data Sheet	3125-1034.EN
N5992U32A USB 3.2 Receiver Test Automation Software – Data Sheet	3125-1425.EN
N5991P PCI Express Receiver Test Automation Platform – Data Sheet	5992-4365EN
M8091BSCB Receiver Test Automation Software for IEEE802.3bs/cd	3124-1256.EN
N4917BSCB 400/800G Optical Receiver Stress Test Automation Software – Data Sheet	5992-4040EN
M809212CA Receiver Test Automation Software for OIF-CEI 5.0 (112G) – Data Sheet	3123-1849.EN
M8091CKCA Receiver Test Automation Software for IEEE802.3ck – Data Sheet	3122-2122.EN
M8091DJCA Receiver Test Automation Software for IEEE 802.3dj – Data Sheet	3125-1419.EN
N4917DJCA 1.6T Optical Receiver Test Automation Software – Data Sheet	3124-1643.EN
Application Notes, White Papers, and Posters	
BERT Applications – White Paper	5992-3479EN
BER Measurement with Real-Time Oscilloscope in M8070B Software – Application Note	5992-2676EN
Advanced Modulation and Coding Challenges – White Paper	5992-3021EN
Total Jitter Measurement at Low Probability Levels – Application Note	5989-2933EN
How Signal Equalization Works for Different Systems – White Paper	5989-3777EN
Error Analysis of PAM4 Signals – Application Note	5992-3268EN
Your Path to 1.6T – Poster	3123-1060EN
Conformance Testing of 800G Ethernet Links for the Data Center – Application Note	3121-1220.EN
Equalizer (Tx/Rx) Optimization at 112 Gbps – Application Note	3124-1727.EN
Race to 448 Gbps – White Paper	7125-1060.EN

Confidently Covered by Keysight Services

Prevent delays caused by technical questions or unplanned system downtime with Keysight Services. Keysight Services support your test operations with expert technical assistance, instrument repair and calibration, software support, training, flexible acquisition program options, and more.

KeysightCare agreements provide dedicated, proactive support through a single point of contact for your instruments, software, and solutions. Covering a broad portfolio of Keysight hardware and application software, KeysightCare helps maximize uptime while delivering faster response times, quicker access to experts, and faster issue resolution.

Keysight Services Offering

Offering	Benefits
KeysightCare 	KeysightCare provides elevated support for Keysight instruments and software, with access to technical support experts that respond within a specified time and ensure committed repair and calibration turnaround times (TAT). KeysightCare offers multiple service agreement tiers, including KeysightCare Assured, Enhanced, and Application Software Support. See the KeysightCare data sheet for details.
KeysightCare Assured	KeysightCare Assured goes beyond basic warranty with repair services that include committed TAT and unlimited access to technical experts.
KeysightCare Enhanced	KeysightCare Enhanced includes all the benefits of KeysightCare Assured plus Keysight's accurate and reliable calibration services, accelerated, and committed TAT, and technical response.
Keysight Support Portal & Knowledge Center	All KeysightCare tiers include access to the Keysight Support Portal where you can manage support and service resources related to your assets such as service requests, and status, or browse the Knowledge Center.
Education Services	Build confidence and gain new skills to make accurate measurements, with flexible Education Services developed by Keysight experts. Including Start-up Assistance.
Alternative acquisition options	
KeysightAccess	Reduce budget challenges with a subscription service enabling you to get the instruments, software, and technical support you want for your test needs.

Recommended Services

Maximize your test system uptime by securing technical support, repair, and calibration services with committed response and turnaround times. **One-year KeysightCare Assured** is included with every new instrument purchase. Extend coverage by purchasing **multi-year KeysightCare upfront** to eliminate annual maintenance purchase cycles and administrative overhead, while ensuring secured service coverage for **2, 3, or 5 years**.

Service	Description
KeysightCare Enhanced *	**Includes technical and application support, warranty and calibration**
R-55B-001-1	KeysightCare Enhanced – Upgrade 1 year
R-55B-001-2	KeysightCare Enhanced – Extend to 2 years
R-55B-001-3	KeysightCare Enhanced – Extend to 3 years (Recommended)
R-55B-001-5	KeysightCare Enhanced – Extend to 5 years (Recommended)
KeysightCare Assured	**Includes technical and application support and warranty**
R-55A-001-2	KeysightCare Assured – Extend to 2 years
R-55A-001-3	KeysightCare Assured – Extend to 3 years
R-55A-001-5	KeysightCare Assured – Extend to 5 years
Start-Up Assistance	
PS-S10	Instrument fundamentals and operations starter
PS-S20	Optional, technology & measurement science standard learning

* Available in select countries. For details, please view the datasheet: KeysightCare Uptime, Precision, Expertise. At Your Service. R-55B-001-2/3/5 must be ordered with R-55B-001-1.

Solution Engineer Professional Services

Keysight Solution Engineer (SE) Professional Services provide expert, hands-on support to help you design, configure, and optimize complex test solutions with confidence. SE Professional Services can include system architecture consulting, application-specific test setup and validation, measurement methodology review, automation and software integration support, test optimization, on-site or remote troubleshooting, and tailored training for engineering teams.

By leveraging deep domain expertise across high-speed digital, SerDes, optical, and protocol-specific applications, Keysight SE Professional Services help shorten time-to-results, improve measurement accuracy, and maximize return on your test investment.

Service	Description
PS-XPS-100/200/300	Solution Engineer Professional Services (Familiarization, Consulting)
PS-XSUP-006/012/018/024/036	Professional Services for Solution Support (6/12/18/24/36 months)
PS-XINS-100/200/300	Solution Engineer Installation Services
PS-XSUP-AESN1	Solution Engineer Productivity Services and Support Days Delivered Over 12 Months (from order or if attached to a solution, with solution delivery)

Ask your local Keysight representative to include any of these or other available services as part of your next M8050A BERT system order to maximize performance, uptime, and long-term value.