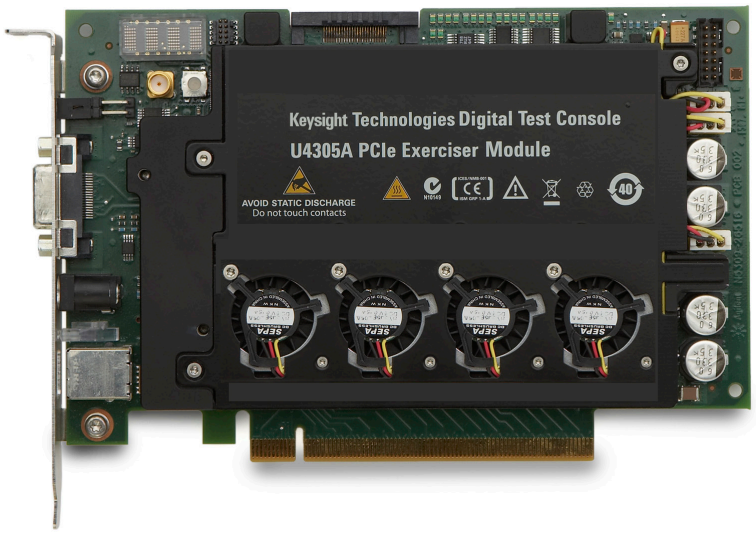
Keysight Technologies

U4305A Protocol Exerciser for PCI Express® 3.0

Data Sheet



A multi-personality test instrument for PCIe:

- NVMe conformance
- LTSSM analysis
- System verification
- Multi-root virtualization
- PCIe compliance testing

KEYSIGHT TECHNOLOGIES

One card: multiple PCIe test applications

PCIe Protocol Test Card

Test to the protocol standard of the PCI-SIG with our automated test package. Provides independent testing of PCIe add-in cards and BIOS systems with both PCIe 2.0 and 3.0 tests built in.

Error Injection on Intel® RAS Platforms

Intel® RAS validation framework now utilizes the Keysight U4305A PCIe 3.0 exerciser card to enable fault and error injection for testing of RAS features, allowing you to ensure the system performance, resiliency and reliability when faults occur.

Complete Exerciser Test Package

Verify LTSSM state transitions and timeouts; emulate PCIe root complex; emulate PCIe device; emulation of non IOV PCIe, MR-IOV, or SR-IOV; fully supported API to write custom test cases; NVMe device testing with Root Complex (RC) emulation.

Overview

- Supports Gen1 (2.5 GT/s), Gen2 (5.0 GT/s), and Gen3 (8.0 GT/s) speeds
- x1, x2, x4, x8, or x16 link widths
- Standard height, half-length card
- Perform thorough link PCIe® Link testing

The Keysight U4305A Exerciser can be configured to provide sub-protocol layer test and debug for legacy and next generation PCIe devices. The U4305A Exerciser for PCIe is an advanced traffic generator that can be used to send and respond to TLP, DLLP, and physical layer packets to stimulate PCIe devices and systems. The Exerciser operates in one of three modes, PCIe, MR-IOV, or SR-IOV. The capabilities of these modes can be enhanced with the purchase of additional software licenses. Specific DUT test case requirements can be written by means of the included API. U4305A is a standard height, half-length PC form factor card as described in the PCI Express specification, and fits into every system including blade servers.

The PCI Express test and debug capabilities of the U4305A is broken down into the sub-protocol layers of the specification as shown in Figure 1. By emulating a PCIe component (with or without MRIOV capabilities), the Keysight U4305A Exerciser acts as an ideal link partner by sending appropriate I/O traffic to stimulate the device under test. The device under test can be exercised under various conditions and scenarios without influencing the performance parameters of the device under test. The Keysight U4305A Exerciser can send a block of TLP requests of 32 or 64 bit Memory, I/O, Configuration, or Message types as stimulus to the device under test. It can also be used to send completion packets in response to DUT's requests.

The U4305A PCIe 3.0 Exerciser provides the following:

- Supports Gen1 (2.5 GT/s), Gen2 (5.0 GT/s), and Gen3 (8.0 GT/s) speeds
- Supports LTSSM functions for up to x16 link widths
- Supports simultaneous use of LTSSM and Protocol Exerciser functions
- Provides SR-IOV capabilities at Gen2 speeds
- Provides emulation of non IOV PCIe components, MR-IOV capable component, or SR-IOV capable components
- Emulation of MR-IOV capable components with five virtual hierarchies (with a separate completion queue for each hierarchy)
- Protocol Exerciser GUI provides a graphical control of the U4305A Exerciser card
- API program control can be done through TCL, Python, C++, or C#
- NVMe Emulation of root complex or end point provides test and verification tools for device controller initialization and queue management

Functions

As an endpoint

When emulating an endpoint, the Keysight U4305A Gen3 exerciser card is plugged into a PCIe slot on the motherboard, as a normal PCIe device. In this scenario, the exerciser card can be used to perform load and stress testing of the system under test.

As a root complex

When emulating a root complex, the Keysight U4305A Gen3 exerciser card communicates with the device under test through the Keysight N5316A backplane board. In this configuration, the exerciser communicates to the DUT through the bottom connectors. The DUT receives its power from the backplane.

Figure 2 shows example setups of a Protocol Exerciser card emulating an endpoint and a root complex.

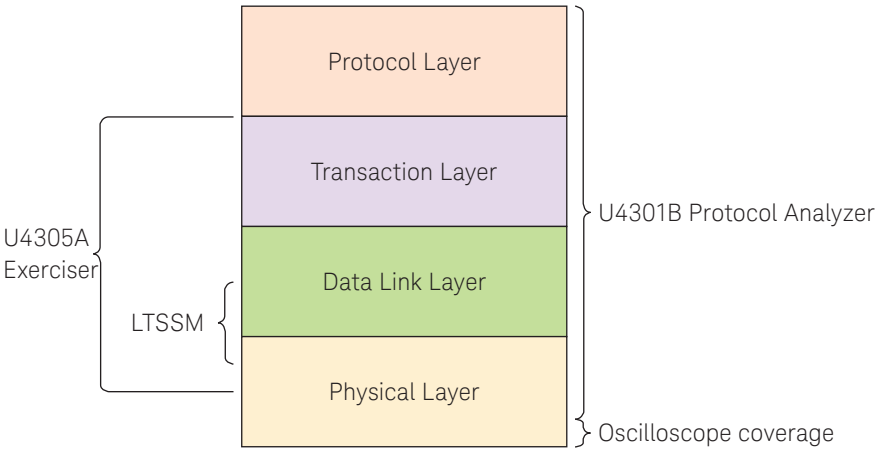


Figure 1. Application coverage of the Keysight U4305A PCIe 3.0 Exerciser module

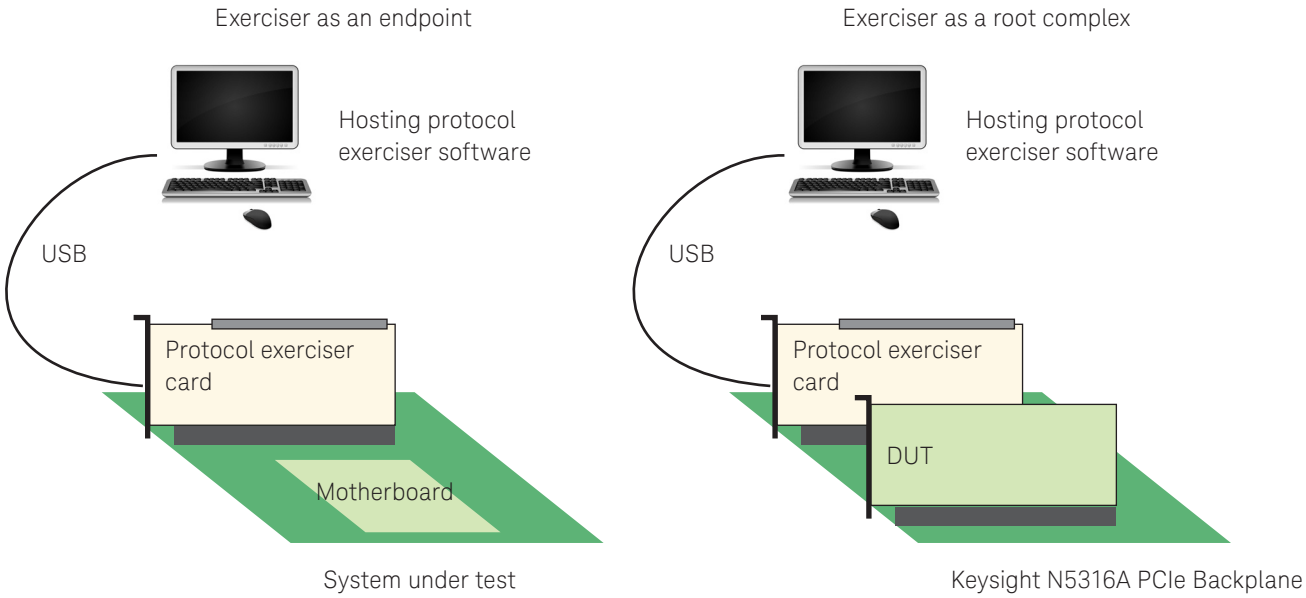


Figure 2. U4305A PCIe exerciser as endpoint and root complex applications

Functions (continued)

As an LTSSM tester

The Link Training and Status State Machine (LTSSM) is the sub-block that drives and controls the link initialization and training process for a PCIe device to enable the normal data exchange between PCIe nodes on the link. LTSSM operates at the physical layer and exchanges physical layer packets (Ordered sets such as TS1 and TS2) to initialize, train, and manage the link. LLTSSM features are provided when option LT3 and EX3 is purchased.

The Keysight U4305A Exerciser provides positive and negative test cases to exercise critical functions of either the end node (adaptor card) or root complex (motherboard or blade). These test cases can force either DUT target devices into various LTSSM states, verify the state transitions, and timeout implementations, and report the test case results as either Passed or Failed.

LTSSM Physical Layer test features

- Supports 1.0 specifications through software selection
- Supports six way speed change from any of the three speeds to any of the three speeds
- When programmed as an Upstream Component (USC), supports going to Gen3 speed with all phases of equalization (0 through 3), only phase 1, or without equalization
- When programmed as a Downstream Component (DSC), it follows USC in equalization process
- Supports automatic or manual enabling/disabling of the lane reversal feature
- Supports independent lane polarity inversion setting for all the lanes
- Supports physical link widths x1, x2, x4, x8, and x16. Link width is fixed and is specified when ordering.
- Supports option to enable/disable scramble modes for Gen1 and Gen2 speeds
- Supports all possible SKIP ordered sets (OS) at transmitter for all three speeds
- Can replace STP/END of a transmitted packet by programmable character at Gen1 and Gen2 speeds. Can corrupt FCRC of STP Token at Gen3 speed.
- Supports programmable Transceiver Settings covering a wide range of transmitted signal amplitude and emphasis levels
- Supports programmable Equalization settings sent in Transition Ordered Sets (TS OS) to request the DUT to transmit at various signal amplitude and emphasis levels

Data Link Layer test features

- Receive a packet as having an LCRC error and NAK in the packet to stimulate DUT response mechanism. Can repeat this for N (N is programmable) for a programmable sequence number causing DUT to replay multiple times and link retraining.
- Can offset Sequence number of transmitted packet for sequence number testing of the DUT
- Can send TLPs with LCRC and/or disparity errors
- Programmable replay timer value

Transaction Layer test features

- Can generate 32 bit or 64 bit memory transactions, Configuration Cycles, I/O Cycles, and message requests
- Generate correct or incorrect ECRC and check the same at the receiver
- Generate malformed TLP by making field inconsistent with actual payload length
- Generate poisoned TLP and nullified TLP
- Delay or discard erroneous completion notification to force completion notification
- Supports Data Compare to check integrity of the payload

Functions (continued)

Exerciser protocol checker

The U4305A PCIe Gen3 Exerciser provides an internal protocol check that reports various protocol errors that the DUT may have made and has been detected at the Exerciser's receiver. An external trigger can be generated on these events to enable trace tools to capture the details of the error condition.

Exerciser as a NON-IOV PCIe device

The Exerciser behaves as NON-IOV End Point (EP) or Root Complex (RC) when the protocol is set to PCIe. In this mode the U4305A Exerciser has three hardware channels and each channel is associated with a specific function (F0, F1, and F2). The traffic in each channel can be programmed independently either through the GUI or through the PCI port.

Two additional functions can be obtained with the purchase of the Option 024 software license.

Exerciser as a SR-IOV capable device

The exerciser behaves as a SR-IOV capable End Point (EP) or Root Complex (RC) when the protocol is set to SR-IOV. In this mode it is compliant with SR-IOV specification Rev. 1.1 (September 8, 2009).

In this configuration the exerciser supports the following:

- One Non-IOV function
- Two Physical Functions (PF)
- Two virtual channels (VC0 and VC(x))
- Two virtual functions (VF1 and VF2) per PF

Multi-root testing

If you want to test an MRIOV-capable PCIe switch, then the protocol exerciser needs to emulate a PCIe device with MRIOV capabilities. The MRIOV license enables the exerciser to emulate an MR- (multi-root) enabled PCIe device. As an MRIOV-capable device, the exerciser supports up to five virtual hierarchies at a time.

The Keysight PCIe protocol exerciser can perform the link negotiation, initialization and training, data link layer functions, and handle incoming requests and completions as per the:

- PCI Express 3.0 base specification for testing a non-IOV PCIe component.
- MRIOV specifications revision 1.0 for testing an MRIOV capable PCIe component.
- SRIOV specifications revision 1.1 for testing an SRIOV capable PCIe component.

	Exerciser license –EX3				Exerciser + Five Function (EX3 + 024)		
Primary option	–	–	**SRIOV (016)**	**MRIOV (025)**	–	**SRIOV (026)**	**MRIOV (025)**
IOV options	-FFP	—	-026	-025	—	-026	-025
Functions	3	3	3	3	5	5	5
Virtual functions			4	4		8	8
Hardware channels	3	3	7	7	5	13	13
Virtual channels	2	2	2	1	2	2	1
Completion queues	2	2	2	3	2	2	5
Virtual link				1			1
Virtual hierarchies				3			5

The Keysight U4305A can be optioned to support multiple functions, virtual functions, and virtual hierarchies.

U4305A-021 Protocol Test Card 3.0

Description

Option 021 protocol test card is a Keysight Technologies, Inc. third-generation PCIe 3.0 link and transaction compliance test tool. Designed to the requirements of the PCI-SIG®, the industry organization chartered to develop and manage the PCI Express standard, the PTC3 will provide the Independent Hardware Vendor (IHV) and Independent BIOS Vendor (IBV) with link transaction test results designed to maximize interoperability and conform to current PCIe 3.0 industry protocol specification.

The PCI Express 3.0 link and transaction layer tests require the use of one Protocol Test Card (PTC). The PCI-SIG has approved the use of the Keysight U4305A protocol test card for PCIe 3.0 compliance testing. It is considered a pass if a product passes all tests on this system at a compliance workshop. Please see the PCISIG.com website for more details on these test procedures.

The PCI-SIG has developed test procedures for PCI Express Link Protocol Testing and PCI Express Transaction Protocol Testing to test add-in card compliance to the specification requirements. It also supports the PCI Express Platform BIOS test to exercise the platform BIOS to make sure it properly detects and initializes PCI Express devices.

Key Features and Specifications

- PCIe 3.0 link and transaction compliance testing
- PCI-SIG-approved testing for PCIe Gen3
- Includes PCIe 2.0 and PCIe 3.0 protocol test cases
- Supports PCIe 2.5 Gb/s, 5 Gb/s and 8 Gb/s speeds
- Requires only x1 lane width U4305A hardware
- PTC3 software can be used on x4, x8, and x16 lane width U4305A
- Requires N5316A test backplane to test add-in cards

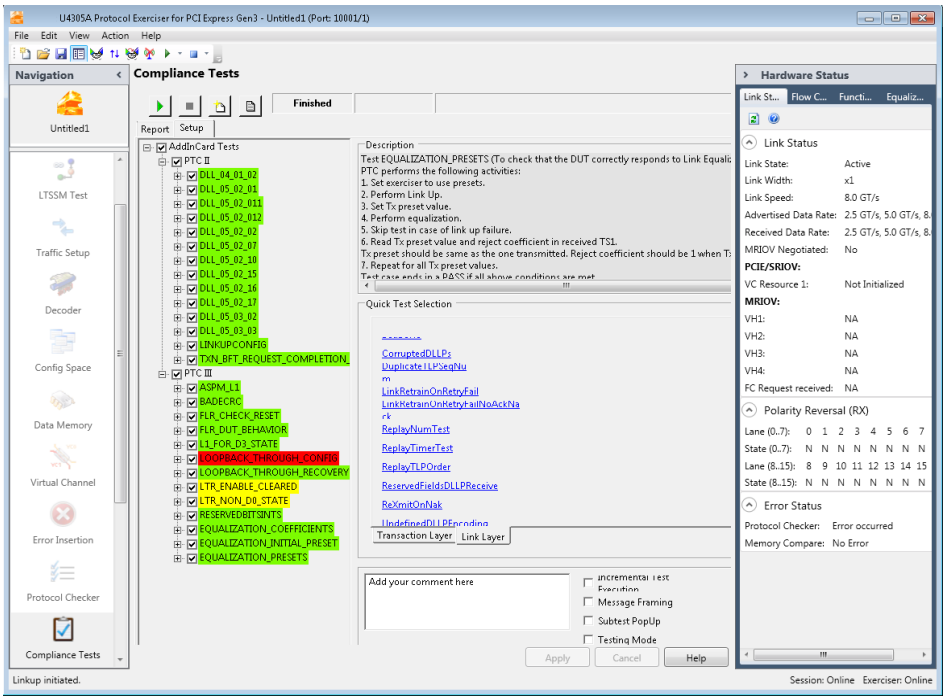


Figure 3. PCIe link and transaction tests as defined by the PCI-SIG provide easy-to-understand pass/fail results.

U4305A-FFP PCIe RAS Test Software License

Description

Intel® RAS (reliability, availability and serviceability) validation framework now utilizes the Keysight U4305A PCIe 3.0 exerciser card to enable fault and error injection for testing of RAS features, allowing you to ensure the system performance, resiliency, and reliability when faults occur.

Solution Structure

Intel® PCI Express RAS Validation Tool Kit

- Keysight U4305A PCIe 3.0 exerciser card
- Keysight PCIe RAS test software license 3.0 (or Keysight PCIe 3.0 exerciser software license)
- Intel® PCI Express hardware error injection GUI software (available from Intel® CDI)
- PCI Express injection tool overview, order guide, user guide (available from Intel® CDI)

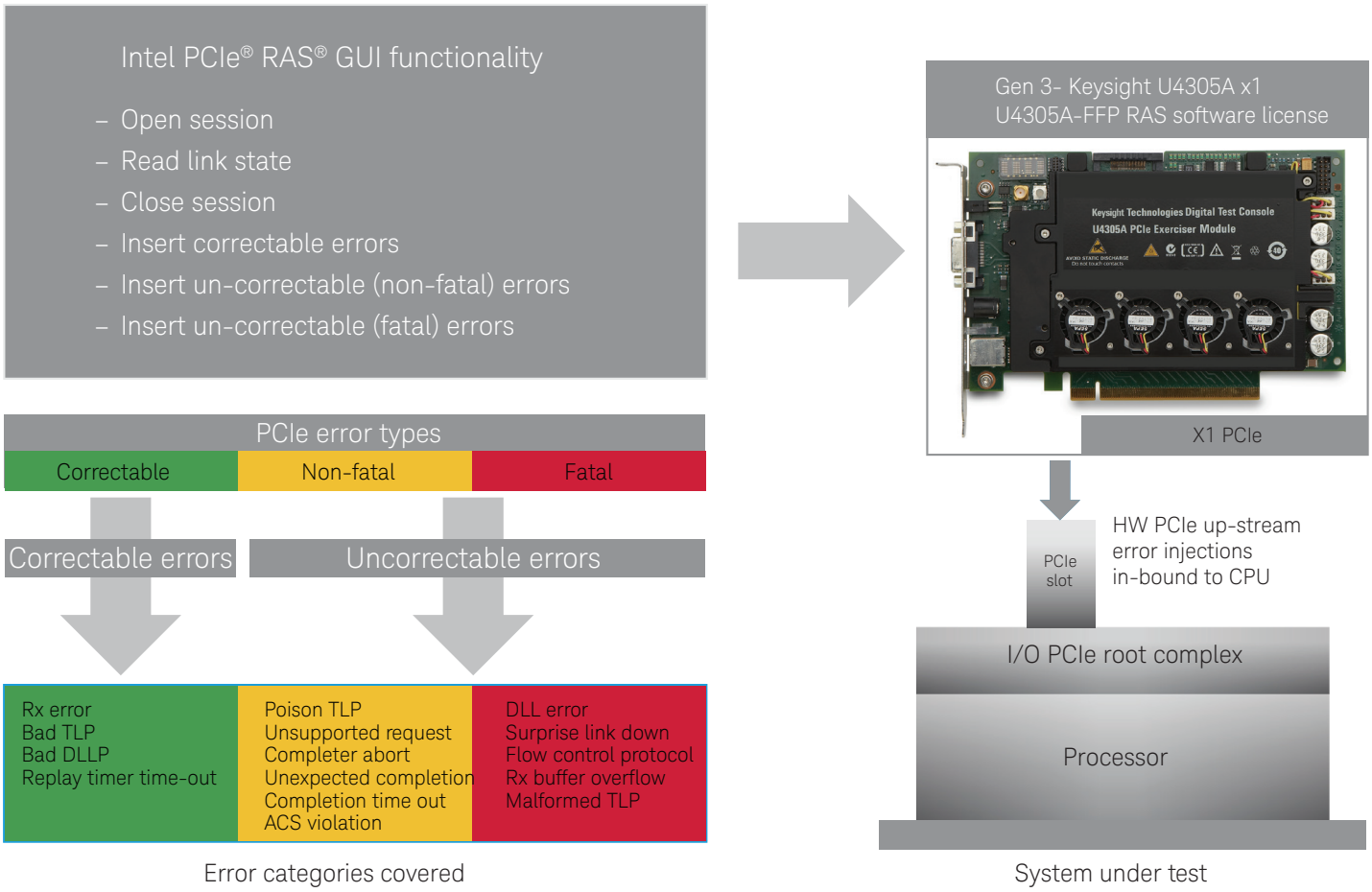


Figure 4. Using the RAS test scripts from Intel, testing fault operations provides validation of the RAS error framework.

U4305A-1FP NVMe RC Emulation

Description

As an NVMe root complex, the exerciser submits various requests (NVMe commands) to an NVMe DUT for completion. These commands include admin commands submitted to the admin queue as well as the I/O commands submitted to the I/O submission queue(s). By sending NVMe command requests to the DUT, you can check how the NVMe controller responds to and completes these requests. You can also verify how the NVMe controller handles admin requests such as queue management or controller initialization. Create multiple submission and completion queues and then use the easy-to-use drag and drop interface to create and send NVMe commands

- View and configure NVMe controller registers of DUT.
- Configure the admin submission and completion queue attributes.
- Initialize and configure the interrupt mechanism.
- Initialize, view, and edit the MSI- X table of the DUT.
- Create up to 64 I/O submission and 64 completion queues.
- Add NVMe commands to submission queues and increase the doorbell accordingly. The commands are available as predefined templates.
- View the commands and their subsequent completions in the completion queues.
- Create PRP lists and PRP entries that can be used in the submitted NVMe commands for data transfer.
- Create SGL entries and SGL lists for validating support of Scatter Gather operations.

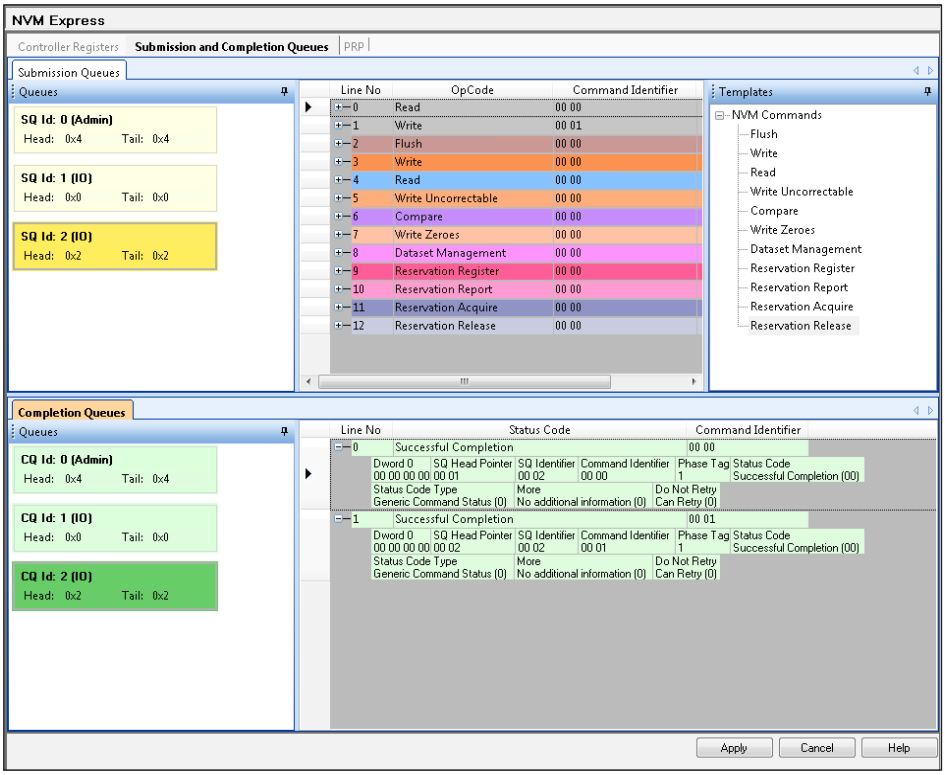


Figure 5. Create up to 64 submission and 64 completion queues, and easily execute queue management commands.

NVMe Conformance Testing

Included with U4301A-1FP and U4301A-2FP options

Standardized testing not only improves the adherence to the specification and increases device interoperability, but it also decreases test time by providing tests that give developers insight into device operation. Keysight is proud to implement the NVMe conformance tests as defined by the University of New Hampshire (UNH) Interoperability Lab (IOL). These tests provide pass/fail/warning results with detailed diagnostic information to improve NVMe validation.

The conformance test implemented 38 tests for validating NVMe and admin commands, features, and process operations

Included in the NVMe test package is a complete programming interface to allow the user to extend the automated test procedures. All of the NVMe conformance tests are implemented using the TCL scripting environment, and scripts are open to user modification. The scripting environment includes a TCL language editor with autocomplete features.

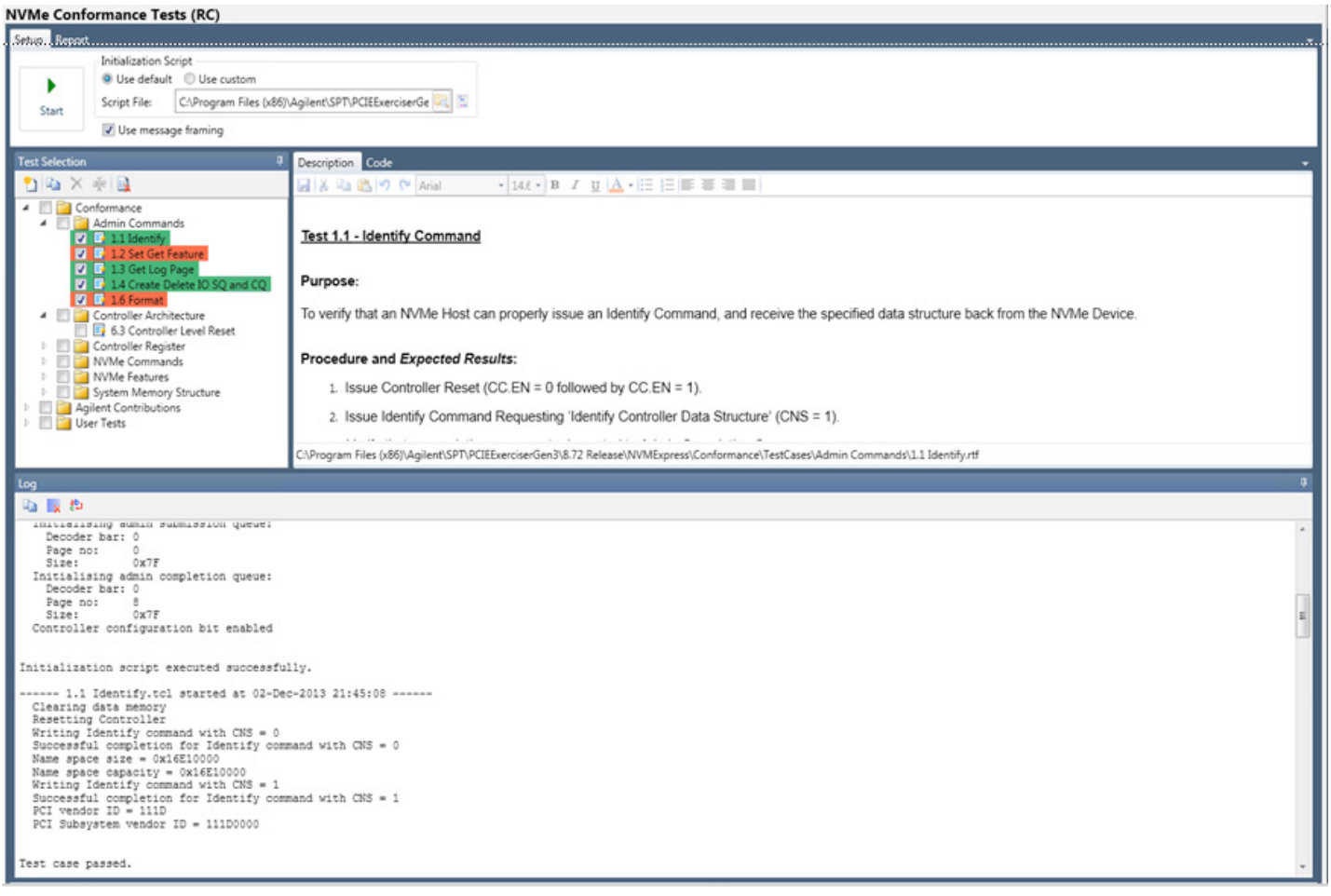


Figure 6. The NVMe conformance test suite 1.1 testing is implemented in an easy-to-use validation framework.

Emulate an NVMe Drive

Using the U4305A as an NVMe device allows the user to verify the proper operation of the storage devices. The user gains easy access and control of all of the device configuration space registers and all NVMe controller operations for fast and easy scenario testing.

- Exerciser allows the RC device to configure its controller registers as an NVMe endpoint and to start NVMe traffic on the exerciser.
- The supports MSI and MSI-X interrupt mechanisms so the RC device can use these mechanisms. The exerciser can respond to interrupts sent via MSI or MSI-X and fetch commands from the submission queues, execute them and write back completions in the completion queues.
- The exerciser allows you to set up the values in the controller registers and also set values for data structures such as identify structures and log pages. It will also let you set the values for device features to be used with the Get/Set features command.
- The exerciser shows up as two drives in the SUT.

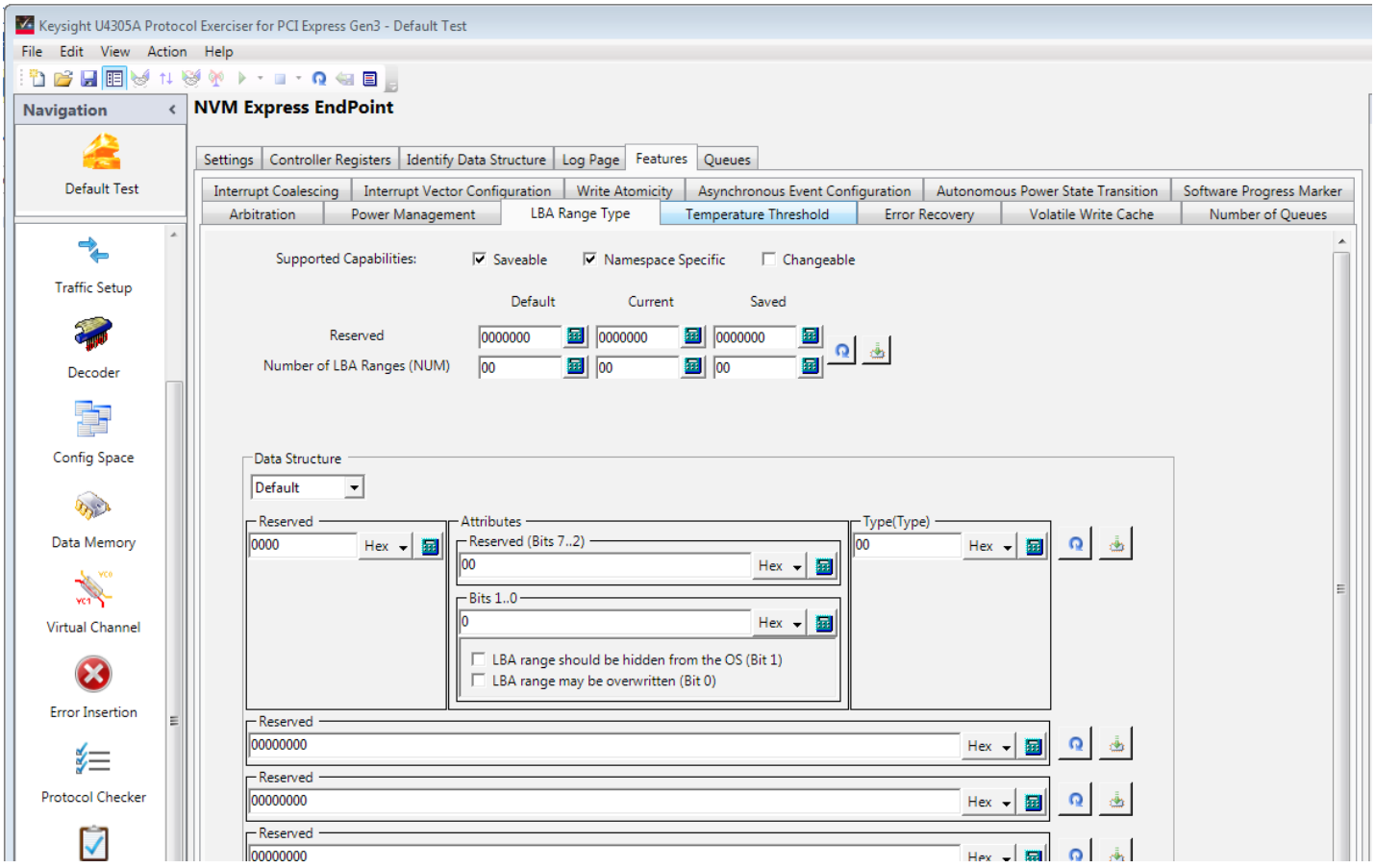


Figure 7. U4305A exerciser can perform all of the functions of an NVMe endpoint with easily modifiable operational parameters.

Test Automation

The U4305A PCIe exerciser supports a rich programming interface that allows automation of all of the exerciser capabilities. Programming can be done via TCL, which is part of the controller PC software package. Experienced users may directly use the API through its COM interface within other programming languages as well. (Examples are included for TCL, Python, C++, and C#.)

API programs can control the exerciser to do complete PCIe test automation. The program can also share the control with the GUI, acting like a subroutine to execute a specific task.

In order to simplify programing, the U4305A includes an API program logging console. To use this tool, the user simply launches the API console, chooses and preferred programming language, and then uses the exerciser GUI interface to perform a test. Then save the program and add any loops, test conditions, or other program operations of interest.

Note that the following API calls are NOT logged: Calls initiated through PTC, LTSSM, or NVMe conformance test suite.

You can view the API logs in the following formats:

- TCL
- C#
- C++
- Python
- Plain text

N5316A Passive Backplane

General	Provides power and clock to DUT
	Test fixture for add-in card testing with exerciser
Power	Separate power on/off for fast reset in tests
	Power reset
	AUX (stand by) power for add-in card available if required
	Per bus power switch
Link width	All link widths are supported
Clocks	Clock generation with/without SSC
	Input for external clock
	Clock output (e.g. for oscilloscope measurements)
	Supports different mid-bus probes N4241A/2A/3A
	Reset/power button
Connectors	Bus 1 – One pair of x16 PCIe connectors – Two x8 mid-bus probe retention modules with bidirectional footprint supporting N4242A (x16), N4241A (x1, x4, x8), N4243A (dual x4)
	Bus 2 – One x16 PCIe connector with loop back
	Bus 3 – One pair of x16 PCIe connectors – Two x8 mid-bus probe retention modules with unidirectional footprint supporting two N4241A (x1, x4, x8, x16)

Figure 7.

PC Requirements

Two computers are required for the operation of the PCI express exerciser, a controller hosting the measurement application software, and a client hosting the device under test (SUT). The controller PC can connect up to a maximum of four Exerciser cards by means of USB ports.

Multiple clients can remotely connect to a single U4305A Exerciser session on the controller PC. Figure 3 shows an Exerciser session scenario in which Session A and Session B have been created on the controller PC with two U4305A Exerciser cards. Two clients are accessing Session A and one client is accessing Session B.

Controller and Client PC Requirements

- USB 2.0 interface for each Exerciser card
- Pentium processor 1 GHz or equivalent
- Windows XP (with Service Pack 2) or Windows 7 (Enterprise or Professional 32-bit or 64-bit) operating system
- At least 256 MB RAM. For better performance, Keysight recommends the installation of at least 512 MB RAM.
- At least 500 MB free disk space on the C drive

Additionally, the client computer must have Microsoft .NET Framework 2.0 installed and it is provided on the installation CD.

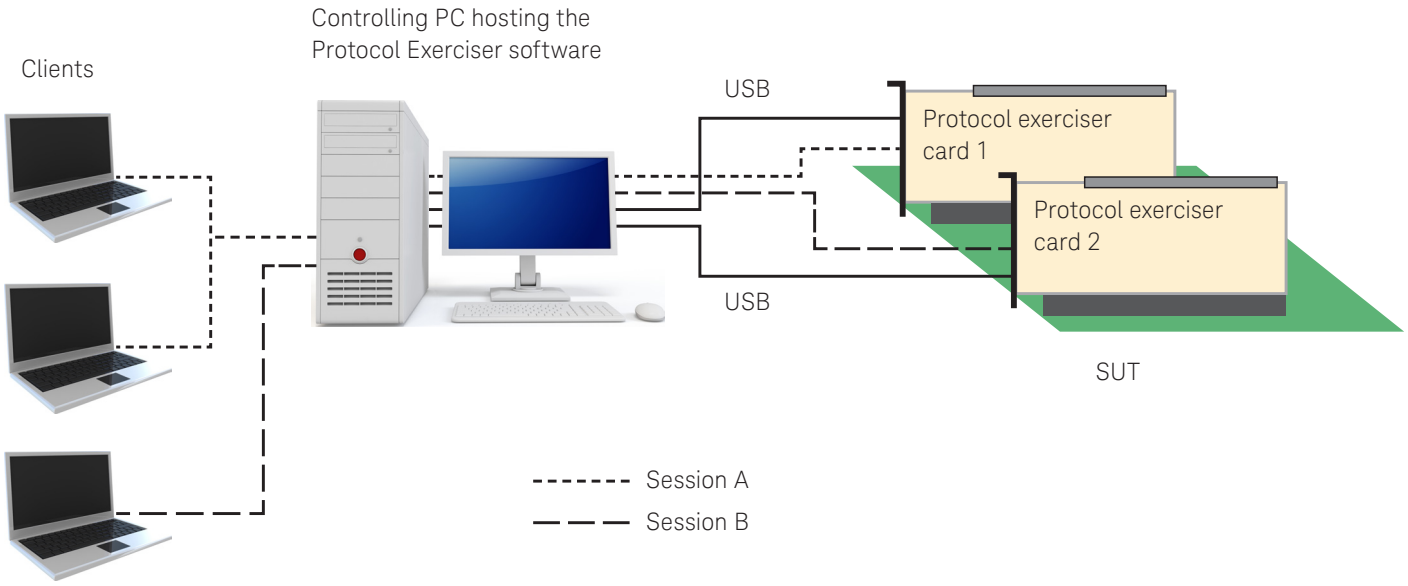


Figure 8.

Specifications and Characteristics

Physical characteristics	
Size	Standard height half-length PCIe module 106.7 mm (4.2 inches) high and 167.65 mm (6.6 inches) long
Weight	408 gr (0.9 lb) Shipping weight: 2.36 Kg (5.2 lb)
Connectors	Power input, USB 2.0B, and two SMA(f) connectors for trigger in and out. Edge connector width is determined by the product configuration purchased. Note: The edge connector is not upgradable after purchase and Keysight does not recommend or support the use of lane adaptors as they have a negative impact on the unit's performance at high speeds.

Power requirements	
Input	15 Vdc, 10 A maximum
Power dissipation	70 W maximum
Keysight part number 0950-5159 external power supply supplied with the Exerciser	
Input	100 to 240 V at 3.5 A maximum, 50 to 60 Hz

LTSSM supported states

The Keysight U4305A supports seven of the 11 LTSSM states. The supported states are:

- Detect
- Quiet
- Configuration
- L0
- Recovery
- L0s
- L1

U4305A trigger specifications	
Trigger output	
Source impedance	50 ohms
Amplitude	2.4 V open circuited, 1.2 V into 50 ohms
Pulse width	120 ns
Trigger input	
Maximum input	2.0 V
Input impedance	Approximately 4 k ohms

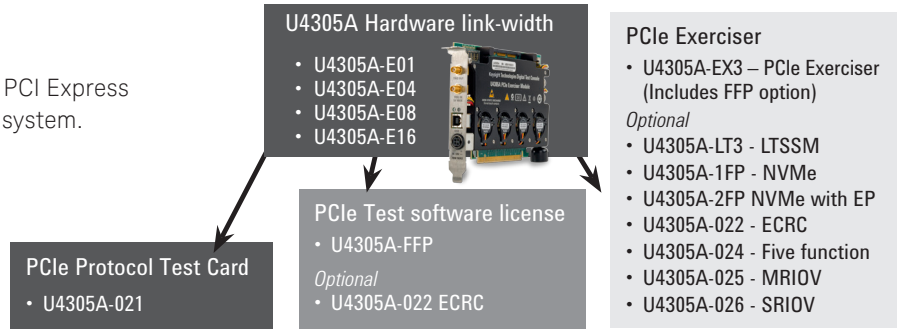
Environmental specifications	
This instrument is intended for indoor use in an installation category II, pollution degree 2 environment.	
Temperature	Operating: 0 to +45 °C Storage: –40 to +70 °C
Humidity	15% to 95% operating, non-condensing
Altitude	2000 m (6,500 feet) maximum
Safety	IEC 61010-1:2001 / EN 61010-1:2001 Canada: CSA C22.2 No. 61010-1:2004 USA: UL 61010-1: 2004

Ordering Information

Use the following steps to configure your U4305A PCI Express module for 8 Gbps to ensure you have a complete system.

Configuration

1. Select exerciser with required link width
2. Select desired functionality
3. Then select additional software license(s)



1. Select desired link width option (x1, x4, x8, or x16).

Link width is a fixed hardware configuration that is not upgradable after purchase. Ensure your link width selection supports your future measurement needs. Keysight does not recommend or support the use of lane width adaptors, as they greatly reduce the ability to reliably test systems operating at Gen2 or greater speeds.

Link width *(required, select one)*	
U4305A-E01	Exerciser board x1 for PCIe 8 Gbps
U4305A-E04	Exerciser board x4 for PCIe 8 Gbps
U4305A-E08	Exerciser board x8 for PCIe 8 Gbps
U4305A-E16	Exerciser board x16 for PCIe 8 Gbps

2. Select desired functionality.

At least one of the following functions must be ordered to make the U4305A operational. The U4305A can be configured to support any combination or all of following functions.

Functionality *(required, select at least one)*	
U4305A-021	Protocol test card (PTC)
U4305A-FFP	PCIe RAS test software, fixed perpetual license
U4305A-EX3	Exerciser software license for PCIe 8 Gbps

3. Select available software options and accessories.

Depending on the selected functionality, you can add software options to expand the product's capabilities.

Additional options for the PCIe RAS test software (-FFP) functionality	
U4305A-022	Transaction layer end-to-end cyclic redundancy check (ECRC) software license
Additional options for the PCIe exerciser (-EX3) functionality	
U4305A-LT3	LTSSM software license
U4305A-1FP	NVMe host (root complex) exerciser and NVMe conformance testing
U4305A-2FP	NVMe host exerciser, NVMe conformance testing, and NVMe deivce emulation (includes option 1FP)
U4305A-022	Transaction layer end-to-end cyclic redundancy check (ECRC) software license
U4305A-024	Software license to enable five functions for use with MRIOV, SRIOV and PCIe
U4305A-025	Multi-root I/O virtualization software license
U4305A-026	Single-root I/O virtualization software license

U4305U Upgrade options	
U4305U-LT3	LTSSM software license
U4305U-1FP	NVMe host (root complex) exerciser and NVMe conformance testing
U4305U-2EP	Upgrade option 1FP to 2FP (add NVMe device emulation)
U4305U-2FP	NVMe host exerciser, NVMe conformance testing, and NVMe deivce emulation (includes option 1FP)
U4305U-FFP	PCIe RAS test software, fixed perpetual license
U4305U-FX3	Upgrade RAS test to exerciser for PCIe 8 Gbps, fixed perpetual license
U4305U-EX3	Exerciser software license for PCIe 8 Gbps
U4305U-021	Protocol test card 3.0 software license
U4305U-022	Transaction layer end-to-end cyclic redundancy check (ECRC) software license
U4305U-024	Software license to enable five functions for use with MRIOV, SRIOV and PCIe
U4305U-025	Multi-root I/O virtualization software license
U4305U-026	Single-root I/O virtualization software license

Ordering accessories

N5316A	Test backplane for PCIe3/PCIe2

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