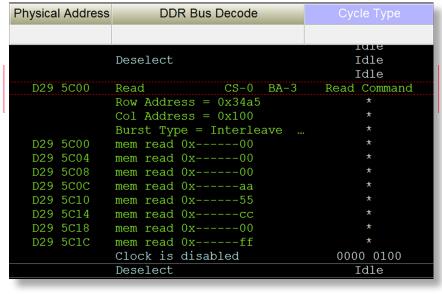
Keysight Technologies

B4623B Bus Decoder for LPDDR, LPDDR2, LPDDR3, or LPDDR4 Debug and Validation

Data Sheet



B4623B bus decode shown in listing window-LPDDR2 example.



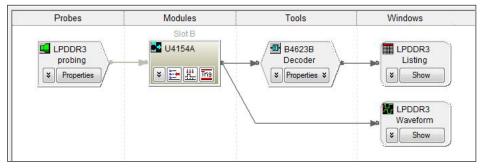
Introduction

Accelerate your time to insight using the B4623B bus decoder for LPDDR, LPDDR2, LPDDR3, or LPDDR4 debug and validation. The B4623B provides complete protocol decode of memory transactions using a Keysight logic analyzer as the analysis execution engine. The B4623B protocol-decode software translates acquired signals into easily understood bus transactions showing associated data bursts, for all LPDDR/2/3/4 data rates. Valid Read and Write commands are decoded to include Row and Column Addresses and the complete data burst associated with the command. The B4623B bus decode software anticipates key system attribute inputs (Burst length, CAS Latency and CAS Write Latency, Chip Selects) from default LPDDR/2/3/4 probing configurations and/or DDR Setup Assistant tool to accelerate decode of LPDDR/2/3/4 bus signals.

Key features and benefits:

- Decodes LPDDR, LPDDR2, LPDDR3, or LPDDR4 acquired traces on Keysight logic analyzer or off-line
- Displays commands, protocol transaction type, physical/row/column/bank addresses, and data in the listing viewer
- Data bursts are associated and displayed with appropriate Read and Write transactions
- Data is displayed at any level of detail from protocol to binary
- Anticipates key system attribute inputs from default probing configurations and/or DDR Setup Assistant tool
- Allows user input to customize decoder properties

After installing the logic analyzer software and the B4623B software and loading the default configuration for your LPDDR/2/3/4 memory, the B4623B icon will show up in the Keysight Technologies, Inc. logic analyzer overview window between the logic analyzer module icon and the listing icon.



LPDDR3 example showing B4623B icon in Keysight logic analyzer overview window, between logic analyzer module and listing.

The properties button on the B4623B icon allows the selection of memory variables. Typically, preferences are filled out for the user in default configurations for specific LPDDR/2/3/4 probes and by the DDR Setup Assistant software tool*, as it helps walk the user through state mode setups.

* DDR Setup Assistant and Eyefinder software is available free of charge. DDR Setup Assistant provides a series of semi-automated steps to simplify state mode measurements for DDR2/3/4 and LPDDR/2/3/4 with U4154B or U4154A logic analyzer modules. The DDR Setup Assistant and Eyefinder software also provides a DDR Eyefinder tool specifically for the 16962A module using the read and write data valid windows for accurate sampling of data.

Chip Selects			Memory Configuration
Chip Select 0	CKE0	•	Memory Type LPDDR3 ▼
Chip Select 1	CKE1	-	Memory Width 16 ▼
Chip Select 2	CKE0	7	Row Bits 15 ▼
Chip Select 3	CKEO	-	
Chip Select 4	CKEO	-	Column Bits 10 ▼
Chip Select 5	CKE0	-	CAS Latency 6.0
Chip Select 6	CKEO	7	CAS Write Latency 5.0
Chip Select 7	CKE0	-	
Chip Select 8	CKEO	7	
Chip Select 9	CKEO	-	Burst Length 8 ▼
Chip Select 10	CKEO	-	DM Enable
Chip Select 11	CKEO	7	
Chip Select 12	CKEO	7	Physical Address Construction
Chip Select 13	CKE0	-	BA Row Address Column Address
Chip Select 14	CKEO	7	Row Address BA Column Address
Chip Select 15	CKEO	+	User supplied .NET assembly
			C:\Program Files\Agilent Technolo Browse
al Address Summar	v		
38373635343332		928 27	262524 2322212019181716 1514131211109 8 7 6 5 4 3 2 1

B4623B properties window, LPDDR3 example.

The B4623B bus decoder for LPDDR/2/3/4 debug and validation operates with multiple Logic Analyzers from Keysight Technologies. Logic analyzer selection criteria includes: logic analyzer specifications and characteristics, maximum DDR technology data rate, and minimum data valid windows of the data eyes at the logic analyzer probe point.

Keysight's 4.0GT/s U4154B or U4154A logic analysis modules are recommended for all LPDDR, LPDDR2, LPDDR3, or LPDDR4 configurations.

Logic analyzer recommendations:

Keysight logic analysis module recommendations for LPDDR/2/3/4 technologies	LPDDR	LPDDR2	LPDDR3	LPDDR4
U4154A* /B	Yes	Yes	Yes	Yes
16962A	Yes	Yes	No	No
16950B	Yes, up to 667 Mb/s	No	No	No
16951B	Yes, up to 667 Mb/s	No	No	No
16910A/11A with option 500	No	No	No	No
16800A series with option 500	No	No	No	No

^{*} U4154A is limited to merging two modules

Refer to www.keysight.com/find/logic for a comparison view of Keysight logic analyzer modules.

Refer to your logic analyzer module data sheet or specific LPDDR/2/3/4, probing solution for logic analyzer module configurations.

Default configurations for B4623B bus decoder for LPDDR/2/3/4 debug and validation are loaded for recommended E5406A Soft Touch Pro footprints, when the B4623B SW is installed.

For custom embedded applications, where changes are made to default configurations, refer to on-line help in the logic analyzer software application for details on the B4623B bus decoder label requirements. For new embedded application configurations, Keysight recommends using the DDR Configurator Creator tool to create a configuration for your unique embedded system. DDR Configurator Creator tool is provided at no cost with version 5.80 and higher software.

Users of the B4623A LPDDR, LPDDR2 bus decoder can upgrade to the B4623B bus decoder for LPDDR/2/3/4 debug and validation by ordering the B4621U.

B4623U upgrade from B4623A bus decoder for LPDDR, LPDDR2 to B4623B bus decoder for LPDDR/2/3/4 requires a prior license for B4623A.

Related literature:

Publication title	Pub number
U4154B 4 Gb/s State Mode Logic Analyzer Module Data Sheet	5992-0108EN
U4154A Logic Analyzer Module Data Sheet	5990-7513EN
Keysight Technologies 16900 Series Logic Analysis System Color Brochure	5989-0420EN
Keysight W3630A Series DDR3 DRAM BGA Data Sheet	5990-3179EN
B4622B DDR2/3/4 LPDDR/2/3/4 Protocol Compliance and Analysis Tool Data Sheet	5990-3300EN

For software downloads refer to: www.keysight.com/find/la-sw-download

Required/recommende	ed software		
Logic and protocol anal	yzer software (required)		
B4623B (required)	Bus decoder for LPDDR/2/3/4 debug and validation		
DDR Setup Assistant ar	nd DDR Eyefinder (recommended)		
Related software			
B4622B	Protocol compliance and analysis toolset for DDR/2/3/4 and LPDDR/2/3/4		
B4621B	Bus decoder for DDR2, DDR3, or DDR4 debug and validation		
Related products			
U4154B	Logic analyzer module		
U4154A	Logic analyzer module		
16962A	Logic analyzer module		
E5406A	Pro Series soft touch connectorless probe - single-ended, for 90-pin cable		

For additional LPDDR/2/3 probing options, contact your local Keysight representative ${\bf www.keysight.com/find/contactus}$

For additional analysis software, refer to www.keysight.com/find/logic-sw-apps

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