Errata

Title & Document Type: **3760A / 3761A 150Mb/s Error Rate Measuring System Operating Manual**

Manual Part Number: **03760-95002**

Revision Date: **June 1973**

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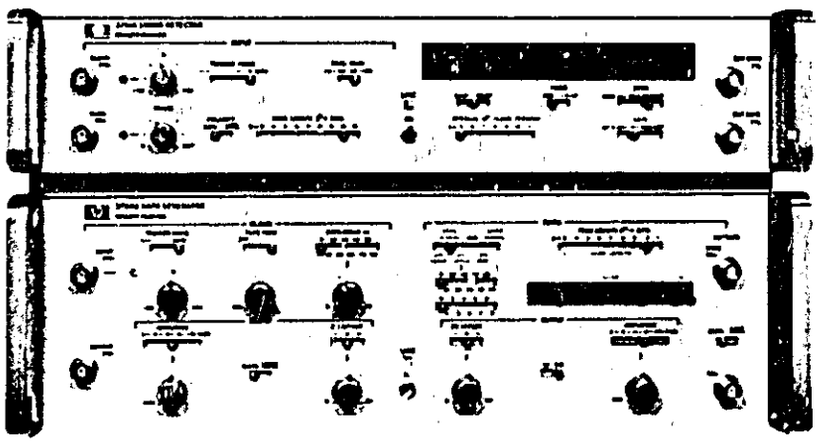
OPERATING MANUAL

150 Mb/s ERROR RATE MEASURING SYSTEM

3760A/61A



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HP 3760A/61A

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CERTIFICATION

The Hewlett-Packard Company certifies that this instrument was thoroughly tested and inspected and found to meet its published specifications when it was shipped from the factory. The Hewlett-Packard Company further certifies that its calibration measurements are traceable to the U.S. National Bureau of Standards to the extent allowed by the Bureau's calibration facility.

WARRANTY AND ASSISTANCE

All Hewlett-Packard products are warranted against defects in materials and workmanship. This warranty applies for one year from the date of delivery, or, in the case of certain major components listed in the operating manual, for the specified period. We will repair or replace products which prove to be defective during the warranty period provided they are returned to Hewlett-Packard. No other warranty is expressed or implied. We are not liable for consequential damages.

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OPERATING MANUAL

MODEL 3760A/61A
150 Mb/s ERROR RATE MEASURING SYSTEM

SERIAL PREFIX

This manual applies to Model 3760A Data Generators with serial prefix numbers higher than 1237U and Model 3761A Error Detectors with serial prefix numbers higher than 1247U.

03760-95002

Printed: JUNE 1973

FOREWORD

The *hp* 3760A/61A Error Rate Measuring System comprises the 3760A Data Generator and 3761A Error Detector. A complete set of manuals for this system is listed below:

3760A/61A System Operating Manual

3760A Data Generator Service Manual

3761A Error Detector Service Manual

This manual contains the following sections:

Section I — General Information and Preparation for Use
Information which applies to both the Data Generator and Error Detector. It covers initial inspection, packaging and supply connection.

Section II — Operating the 3760A Data Generator
3760A Specifications, details of front panel controls connectors and indicators and operational notes.

Section III — A replica of Section II with 3761A details and additional information on setting up procedures and rear panel connectors.

Section IV — Fault Isolation
Isolating a fault to one instrument.

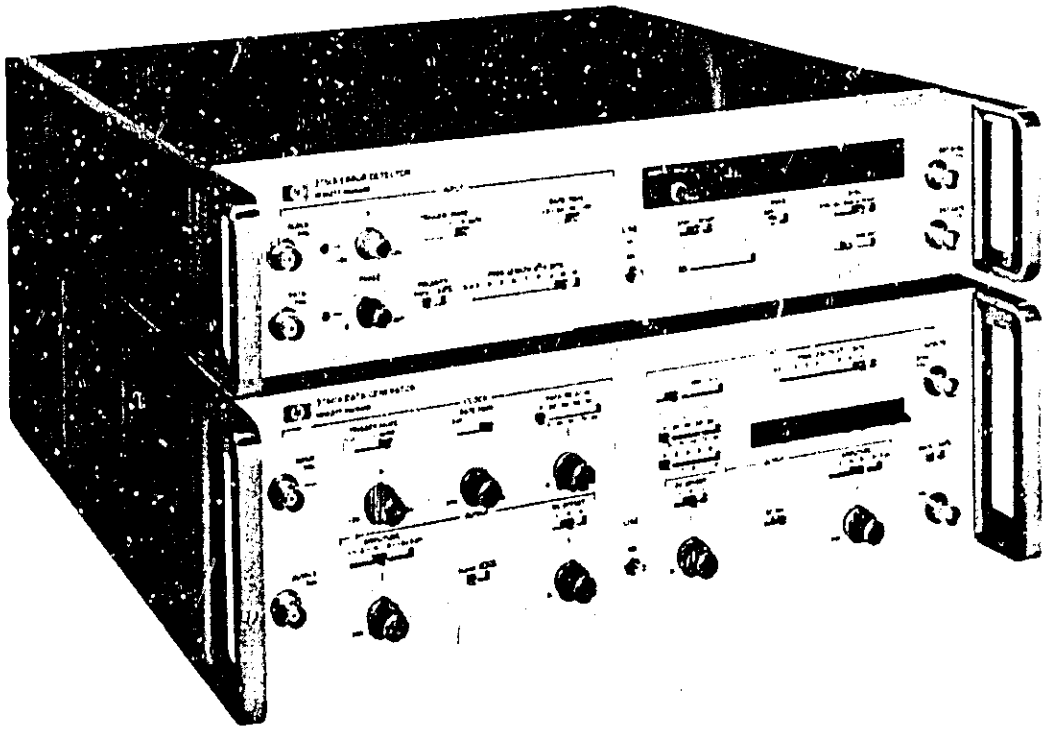
LIST OF CONTENTS

SECTION I GENERAL INFORMATION AND PREPARATION FOR USE

SECTION II OPERATING THE 3760A DATA GENERATOR

SECTION III OPERATING THE 3761A ERROR DETECTOR

SECTION IV FAULT ISOLATION



3760A/61A Error Rate Measuring System

SECTION I
GENERAL INFORMATION and PREPARATION FOR USE

1-1 GENERAL INFORMATION

1-2 INTRODUCTION

This section contains the general information relating to both the 3760A Data Generator and 3761A Error Detector. General information on individual instruments, eg, options available, accessories supplied and fuse ratings are given at the beginning of Section II for the Data Generator and the beginning of Section III for the Error Detector.

1-3 INSTRUMENT IDENTIFICATION

An identification plate is fitted to the rear panel of each instrument. The number on this plate consists of a four digit serial prefix, a reference letter, and a five digit serial number. These details should be quoted in any correspondence with Hewlett-Packard relating to the instrument and are particularly important when ordering spare parts or components.

1-4 TEMPERATURE RANGE

The instruments are designed to operate over an ambient temperature range of 0^{o} to 50^{o}C (32^{o} to 122^{o}F) and to be stored at -40^{o} to 65^{o}C (-40^{o} to 149^{o}F).

1-5 SERVICE

A technique for fault isolation between the Data Generator and Error Detector will be found in Section IV of this manual, separate manuals being provided for the service of the individual instruments. If it is necessary to return an instrument to one of the *hp* Service Offices, listed at the back of this manual, a card should be firmly attached to the instrument giving details of the fault condition or type of service required and the return address.

1-6 INITIAL MECHANICAL INSPECTION

Each instrument is carefully examined both mechanically and electrically prior to shipment. The instruments should be examined as soon as possible after receipt for external damage which may have occurred during shipment such as broken controls or connectors and dents or scratches on the panel surfaces. If any damage is evident refer to Paragraph 1-8 for recommended claim procedure and Paragraph 1-9 for repackaging information.

1-7 INITIAL ELECTRICAL INSPECTION

The Performance Tests in the individual instrument service manuals provide a method of confirming the specification and may be useful as incoming inspection checks. In the event of the instrument not performing within the specifications refer to the claim procedure Paragraph 1-8 and repackaging information Paragraph 1-9.

1-8 CLAIMS FOR SHIPPING DAMAGE

If the instrument is physically damaged or fails to meet specifications on receipt, notify the carrier and the nearest Hewlett-Packard Sales and Service Office (listed at the back of this manual). The Sales and Service Office will arrange for repair or replacement without waiting for settlement of a claim with the carrier.

1-9 REPACKAGING FOR SHIPMENT

To protect electronic equipment during storage or shipment always use the best packaging methods available. Hewlett-Packard field offices can provide packing materials used for original factory packaging at short notice. Two suitable alternative packaging methods are given below:

a. RUBBERISED HAIR. Cover painted surfaces of instrument with protective wrapping paper. Pack instrument securely in strong corrugated container (350lb/sq. in bursting test) with 2-inch rubberised hair pads placed along all surfaces of the instrument. Insert fillers between pads and container to ensure a snug fit.

b. EXCELSIOR. Cover painted surfaces of instrument with protective wrapping paper. Pack instrument in a strong corrugated container (350lb/sq. in bursting test) with a layer of excelsior about 6-inches thick packed firmly against all surfaces of the instrument.

1-10 PREPARATION FOR USE

1-11 POWER REQUIREMENTS

Both the Data Generator and Error Detector may be operated from a 90 to 125V ac (nominal 115V) or a 200 to 255V ac (nominal 230V) supply of 40 to 400Hz single phase.

1-12 SELECTING 115 or 230V OPERATION

Slide the shutter, on the rear panel power input connector, over the connection pins and expose the fuse compartment. Remove the line fuse and set the line voltage selection switch to the required range. Select the correct fuse using Table 1-1 and insert in the fuse holder. Slide the shutter over the fuse compartment to expose the connection pins.

Table 1-1 Line fuse ratings

	3760A DATA GENERATOR	3761A ERROR DETECTOR
115V line fuse	3A slow-blow *hp* 2110-0381	2A slow-blow *hp* 2110-0303
230V line fuse	1.5A slow-blow *hp* 2110-0304	1A slow-blow *hp* 2110-0007

1-13 SUPPLY CONNECTION

A 3-core power cable is supplied with each instrument using the colour coding given in Table 1-2. It should be ensured that the correct line voltage has been selected before connecting the instrument to the supply. If connection is made via a two pin socket the GREEN/YELLOW CORE OF THE POWER CABLE SHOULD BE CONNECTED TO GROUND for the protection of the operator.

Table 1-2 Power Cable Colour Code

	Line	Neutral	Ground
Europe	Brown	Blue	Green/Yellow
USA	Black	White	Green/Yellow

1-14 COOLING

Forced air cooling is used in the 3760A and 3761A and the following clearances should be allowed for ventilation.

3 to 4 inches at the rear for air intake.

2 to 3 inches at each side for air exhaust.

The clearances provided by the plastic feet in bench mounting and by the filler strip in rack mounting permit adequate ventilation for the top and bottom surfaces. The operating temperature should be maintained within the range 0^{o} to 50^{o}C. Storage temperature limits are -40^{o}C and $+75^{o}$C.

1-15 AIR FILTER

Each instrument has an air intake filter which is fixed to the rear panel with four screws. This filter should be removed and cleaned at intervals of approximately one month. A compressed air line is recommended for cleaning the air filter.

1-16 BENCH OPERATION

Both instruments have plastic feet and foldaway tilt stands for convenience of use in bench operation. The feet provide both air circulation clearance and a self aligning facility when stacked with other *hp* full rack width instruments.

1-17 RACK MOUNTING

The rack mounting kit contains all of the hardware required for mounting the instruments in standard 19-inch racks. Installation instructions are given in the kit.

OPERATING PROCEDURES

3760A Data Generator Specifications

MODES OF OPERATION

PRBS NORMAL	Generates a repetitive $2^N - 1$ bit, maximal length, Pseudo Random Binary Sequence where N = 3 to 10 and 15.
PRBS ADD ZEROS	Addition of a block of 1 to 99 zeros into PRBS NORMAL, occurring after the sync pulse.
PRBS ADD ERROR	Introduction of two errors per 4000 sequences by changing two consecutive bits to their logic complements.
1010	Generates a preset repetitive word, content 1010.
WORD NORMAL	Generates a continuous 3 to 10-bit word with selectable content.
WORD ADD ZEROS	Addition of a block of 1 to 99 zeros into WORD NORMAL, occurring between words

CLOCK INPUT

Rate	1.5 to 150MHz.
Impedance	50Ω ±5% dc coupled (75Ω optional).
Trigger:	
Manual	Level range: -3 to +3V. Slope +ve or -ve.
Auto	Input mark:space ratio range 10:1 to 1:10.
Sensitivity	Better than 500mV pk-pk.
Amplitude	5V pk-pk maximum. Limits ±5V.
Pulse Width	3ns minimum at 50% pulse amplitude.

CLOCK OUTPUT

Outputs	CLOCK or $\overline{\text{CLOCK}}$, from external or optional internal clock.
Impedance	Source impedance 50Ω ±5% (75Ω optional).
Amplitude	Continuously variable in 5 ranges from 0.1 to 3.2V symmetrical about offset level.
Rise/Fall time	<1.4ns into 50Ω. <1.6ns into 75Ω (75Ω impedance option).
DC Offset	Zero: <2% of pulse amplitude. Variable: Continuous 0 ±3V.

OPTIONS

Option 001	75Ω CLOCK and DATA input/output impedances.
Option 002	Internal, variable frequency clock. Rate: 1.5 to 150MHz. Jitter: <0.5% of period +0.05ns pk-pk.
Option 003	Options 001 and 002 combined.

DATA OUTPUT

Outputs	DATA or $\overline{\text{DATA}}$.
Format	NRZ. RZ (up to 130Mb/s).
Impedance	Source impedance 50Ω ±5% (75Ω Optional).
Amplitude	Continuously variable in 5 ranges from 0.1 to 3.2V into 50Ω symmetrical about offset level.
Rise/Fall time	<1.4ns into 50Ω. <1.6ns into 75Ω (75Ω impedance option).
Overshoot	<10% of pulse amplitude.
DC Offset	Zero: <2% of pulse amplitude. Variable: Continuous 0 to ±3V.
DELAY	Data (and sync) delayed with respect to clock continuously in 10 ranges from 0 to 100ns.

SYNC OUTPUT

Rate	Once per PRBS or WORD cycle.
Duration:	
PRBS and WORD Normal	1 CLOCK period.
Add Zeros	Length of zero block plus one clock period.
Position:	
PRBS Normal	Front panel selectable.
WORD Normal	Precedes word.
Add Zeros	Precedes zero block by one clock period.
Impedance	Source impedance 50Ω ±5%.
Amplitude	+1V nominal

GENERAL

Power 90 to 125 or 200 to 250V. 40 to 400Hz, consumption 90W.	Weight 30lbs (13.6kg)	Dimensions 16¾in wide, 5½in high, 18¾in deep (425mm x 140mm x 467mm).

SECTION II
OPERATING THE 3760A DATA GENERATOR

2-1 INTRODUCTION

The Hewlett-Packard Model 3760A Data Generator produces both digital words and Pseudo Random Binary Sequences, PRBS, at rates from 1.5Mb/s up to 150Mb/s.

The clock frequency, in the range 1.5 to 150MHz can be derived from an internal clock generator (optional) or the unit can be manually or automatically triggered from an external clock. A clock output, variable in amplitude from 0.1 to 3.2V pk-pk with a rise time of better than 1.4ns, is also provided.

The pseudo-random binary sequence, PRBS, is variable in length from $2^3 - 1$ to $2^{10} - 1$ bits, with an additional long sequence of $2^{15} - 1$ bits. A sync pulse occurs once per sequence and can be used to initiate a block of 1 to 99 zeros. This block is inserted into the data stream to facilitate the clock extraction tests used in some PCM systems. As the 3760A Data Generator is often used in conjunction with the 3761A Error Detector, deliberate errors can be inserted to check the accuracy of the 3760A/61A system.

The length of the binary word is variable from 3 to 10 bits and its content is selected on the front panel. A sync pulse occurs once per sequence and again it can be used to initiate a block of zeros which is inserted between words. Alternatively, the pre-programmed maximum change sequence, 1010 can be selected.

The data output which can be PRBS, WORD or the fixed maximum change sequence, 1010, is available in normal or complemented form. As with the clock, this output is calibrated from 0.1 to 3.2V pk-pk in amplitude and 0 to ±3V dc in offset with rise times of better than 1.4ns. Either RZ or NRZ formats may be selected and the data output can be delayed by up to 100ns with respect to the clock.

2-2 OPTIONS

In the standard instrument all input and output impedances are 50Ω and the clock drive is from external input only. OPTION 001 has input and output impedances of 75Ω with the exception of the sync output which remains at 50Ω. With OPTION 002 the Data Generator has an internal clock generator with frequency variable from 1.5 to 150MHz and retains the external input facility. Both of the above options are available on the same instrument as OPTION 003 if required.

2-3 ACCESSORIES

The instrument is provided with a 3-core power cable, an extender board located in a spare position in the clock module, a 3 amp fuse: stock number 2110-0381 for 115V operation, a spare indicator lamp, stock number 2140-0374 clipped to the rear of the front panel lamp assembly, and a rack mounting kit.

2-4 FUSE RATINGS AND LOCATION

Table 2-1 provides a list of all fuses in the instrument and Figure 2-1 shows their location. All fuses are protected by overvoltage and overcurrent limiting in the power supply.

Table 2-1 Fuse Ratings

Fuse		Rating	*hp* Stock Number
F1	Main Supply 230V	1.5A slow-blow	2110-0304
	Main Supply 115V	3A slow-blow	2110-0381
F2	+15V	4A slow-blow	2110-0365
F3	- 5V	10A slow-blow	2110-0051
	- 2V		
F4	-15V	4A slow-blow	2110-0365

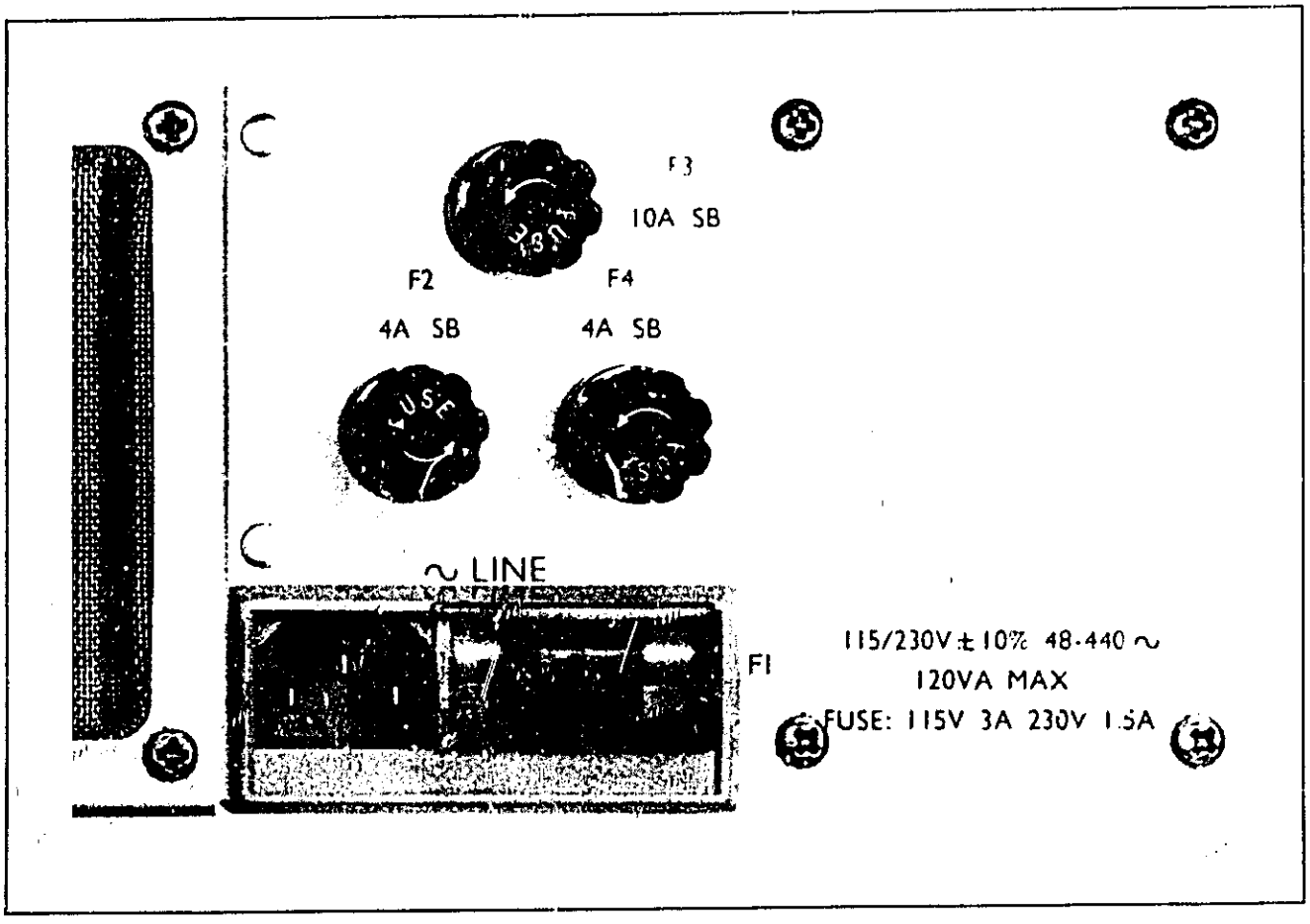


Figure 2-1 Fuse location on Rear Panel

2-5 THE FRONT PANEL

The front panel may be divided into functional areas as shown in Figure 2-2. The description of the controls connectors and indicators, given on Pages 2-4 to 2-7, is divided into the same functional areas.

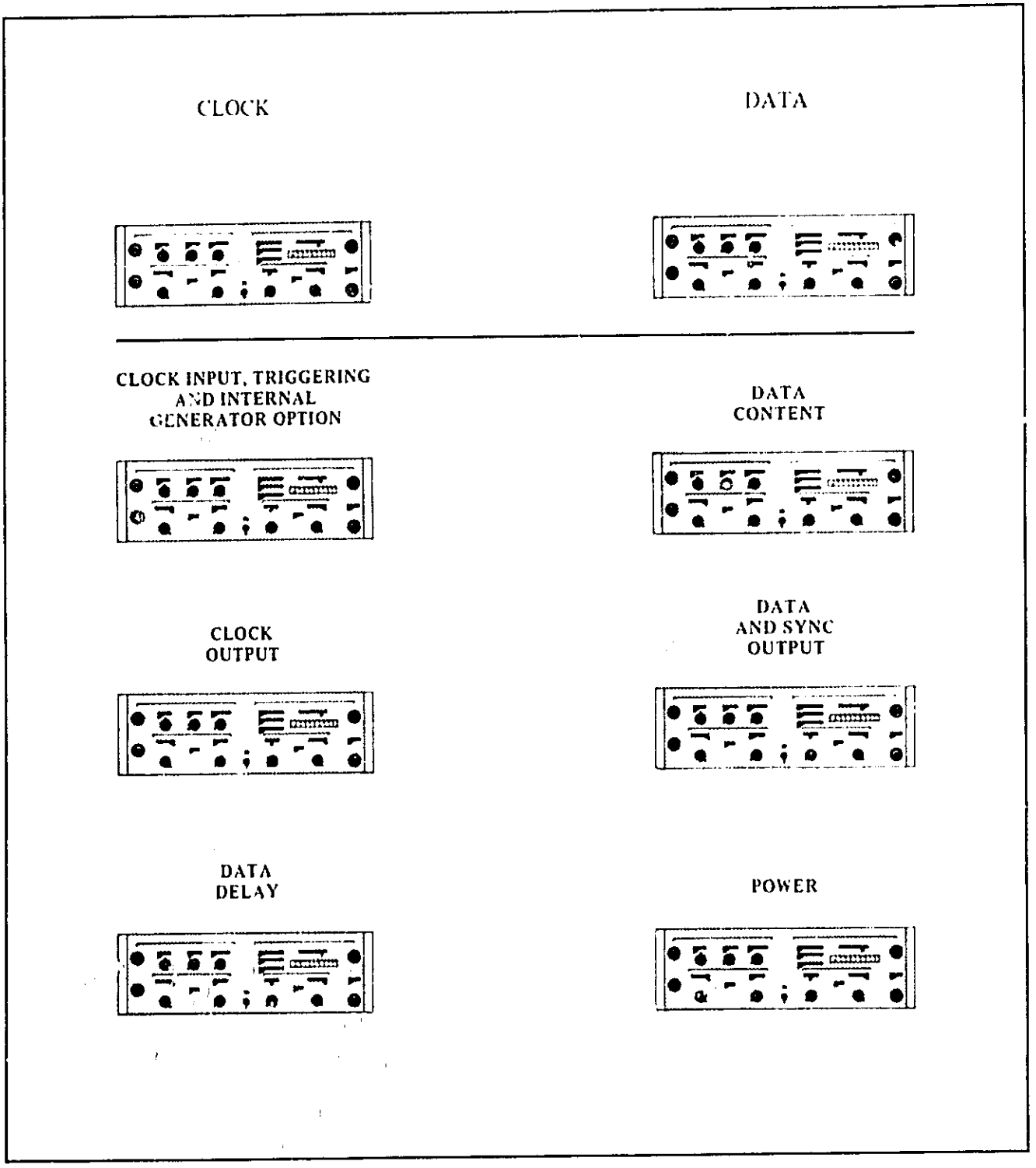
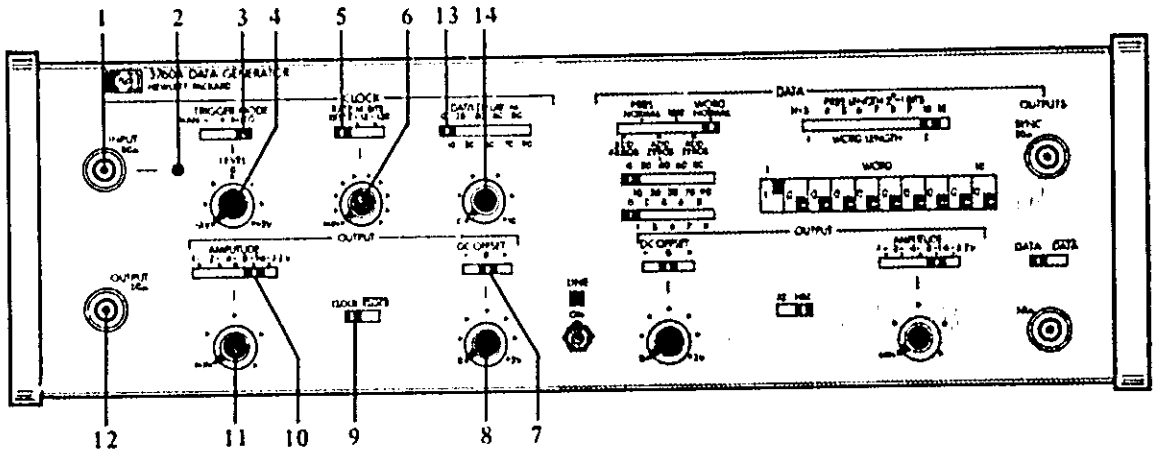


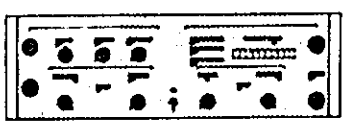
Figure 2-2 Front Panel Functional Areas

2-6 Controls Connectors and Indicators

2-7 CLOCK SECTION



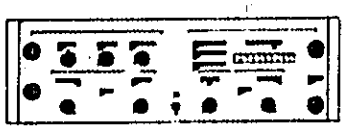
CLOCK INPUT, TRIGGERING AND INTERNAL GENERATOR OPTION



1. CLOCK INPUT. 50Ω External input frequency controls data rate. Input levels: minimum 500mV pk-pk, maximum ± 5V.
2. TRIGGER INDICATOR LAMP. Data Generator is triggered when lamp is ON.
3. TRIGGER MODE SWITCH. Selects MANUAL +ve or -ve slope triggering or AUTO triggering.
4. TRIGGER LEVEL VERNIER. Sets MANUAL trigger level between +3 and -3V.
5. CLOCK RATE SWITCH, OPTION 002 ONLY. Selects external source or internal generator ranges 1.5 to 15, 15 to 150MHz.
6. CLOCK FREQUENCY VERNIER, OPTION 002 ONLY. Sets frequency over range selected with 5.

Figure 2-3 Clock Controls

CLOCK
OUTPUT



7. CLOCK OUTPUT DC OFFSET SWITCH. Selects (+) positive offset range 0 to 3V, (-) negative offset range 0 to -3V or (0) zero offset.

8. CLOCK OUTPUT DC OFFSET VERNIER. Sets offset 0 to 3V either positive or negative as selected with 7.

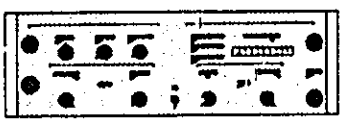
9. CLOCK/$\overline{\text{CLOCK}}$ SWITCH selects the clock signal or its complement at clock output 12.

10. CLOCK OUTPUT AMPLITUDE SWITCH. Selects amplitude range of CLOCK or $\overline{\text{CLOCK}}$ output ranges available 0.1 – 0.2, 0.2 – 0.4, 0.4 – 0.8, 0.8 – 1.6 and 1.6 – 3.2V.

11. CLOCK OUTPUT AMPLITUDE VERNIER. Sets amplitude over range selected with 10.

12. CLOCK OUTPUT 50Ω. Provides an output from external clock input signal or from internal clock generator OPTION 002. The complement of the clock signal is also provided (see switch 9).

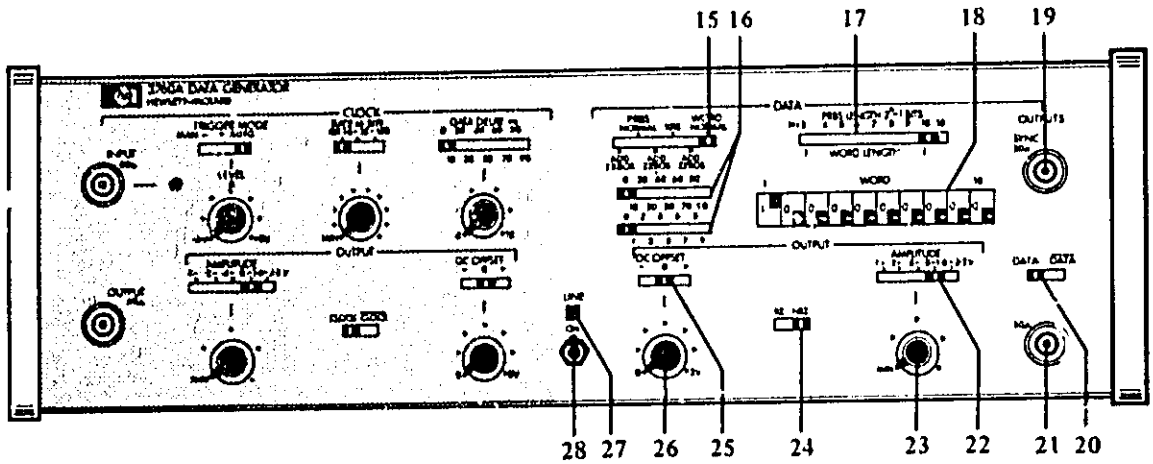
DATA
DELAY



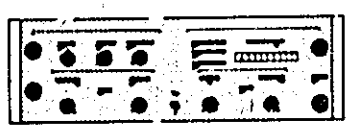
13. DATA DELAY SWITCH. Selects coarse delay in 10ns steps from 0 to 90ns on clock input to the data section. Delays DATA, $\overline{\text{DATA}}$ and SYNC outputs but not CLOCK output.

14. DATA DELAY VERNIER. Sets fine delay, continuously variable 0 to 10ns additional to delay selected with 13.

2-8 DATA SECTION



DATA CONTENT



15. **MODE SWITCH.** Selects data output mode: PRBS or WORD NORMAL, ZERO ADD, maximum change sequence 1010 or PRBS with one ERROR in 2000 sequence.

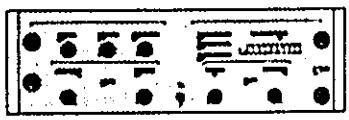
16. **ADD ZEROS SWITCHES.** For setting the number of zeros added (0 to 100) in PRBS and WORD ZERO ADD modes.

17. **REGISTER LENGTH SWITCH.** Sets the register length n for word length n bits (3 to 10 only) or PRBS length $2^n - 1$ bits.

18. **WORD BIT SELECT SWITCHES.** Illuminated positions available for WORD selection. Switch settings determine position of SYNC and ADDED ZEROS in PRBS.

Figure 2-4 Data Controls

DATA
AND SYNC
OUTPUT



19. SYNC OUTPUT 50Ω. Provides one pulse per WORD or PRBS. Amplitude 1V, duration 1 clock period in NORMAL and PRBS ERROR modes, 1 clock period longer than added zeros in ZERO ADD modes.

20. DATA/$\overline{\text{DATA}}$ switch selects the data signal DATA or its complement $\overline{\text{DATA}}$ at output 21. In DATA level of data 1 more positive than data 0. In $\overline{\text{DATA}}$ level of data 0 more positive than level of data 1.

21. DATA OUTPUT 50Ω provides an output of the data selected with MODE switch 15. Either normal or complemented data may be selected with switch 20.

22. DATA OUTPUT AMPLITUDE SWITCH selects amplitude range of both DATA and $\overline{\text{DATA}}$ outputs, ranges available 0.1 – 0.2, 0.2 – 0.4, 0.4 – 0.8, 0.8 – 1.6 and 1.6 – 3.2V.

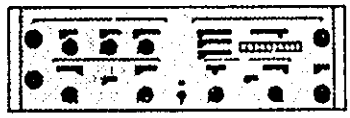
23. DATA OUTPUT AMPLITUDE VERNIER. Sets amplitude over range selected with 22.

24. FORMAT SWITCH selects format of DATA and $\overline{\text{DATA}}$ outputs either RZ (return to zero) or NRZ (non return to zero).

25. DATA OUTPUT DC OFFSET SWITCH selects (+) positive offset range 0 to 3V, (-) negative offset range 0 to -3V or (0) zero offset.

26. DATA OUTPUT DC OFFSET VERNIER. Sets offset 0 to 3V either positive or negative as selected with 25.

POWER



27. LINE ON/OFF INDICATOR LAMP. Indicates state of switch 28.

28. LINE ON/OFF SWITCH. Connects supply to power supply transformer primary.

2-9 OPERATIONAL NOTES

The 3760A DATA GENERATOR operational notes are divided into four groups which are presented in the following order.

CLOCK	Clock input and triggering. Clock output.
DATA GENERATION	Word generation. PRBS generation.
DATA MODIFICATION	Zero addition. Error addition. Data format. Data delay.
OUTPUT CONTROL	Output amplitude and dc offset. Complementary outputs.
THE SYNC PULSE	

2-10 CLOCK INPUT AND TRIGGERING

The Data Generator has a 50Ω external clock input which accepts any waveshape in the 1.5 to 150MHz range with an amplitude of at least 0.5V pk-pk. Either AUTO triggering, or MANUAL triggering on +ve or -ve slope may be selected with the TRIGGER MODE switch, the manual triggering level being set between +3 and -3V with the TRIGGER VERNIER. A front panel lamp indicates that the Data Generator is being triggered when it is 'ON'.

With the TRIGGER switch in the AUTO position the triggering level is the mean dc level of the clock input. In order to retain this level between the maximum and minimum thresholds the clock input mark:space ratio should be limited to the range 10:1 to 1:10. The mark:space ratio is maintained through the data delay circuitry and is reproduced at the data output when using RZ format. The clock mark should be at least 3ns wide particularly if it is intended to use the zero add facility.

The MANUAL TRIGGER VERNIER may be set to operate at any level between +3 and -3V, enabling the width of the RZ data output mark to be chosen by selecting the triggering level of a sine wave clock input as shown in Figure 2-5. Note that the minimum input triggering pulse width is 3ns.

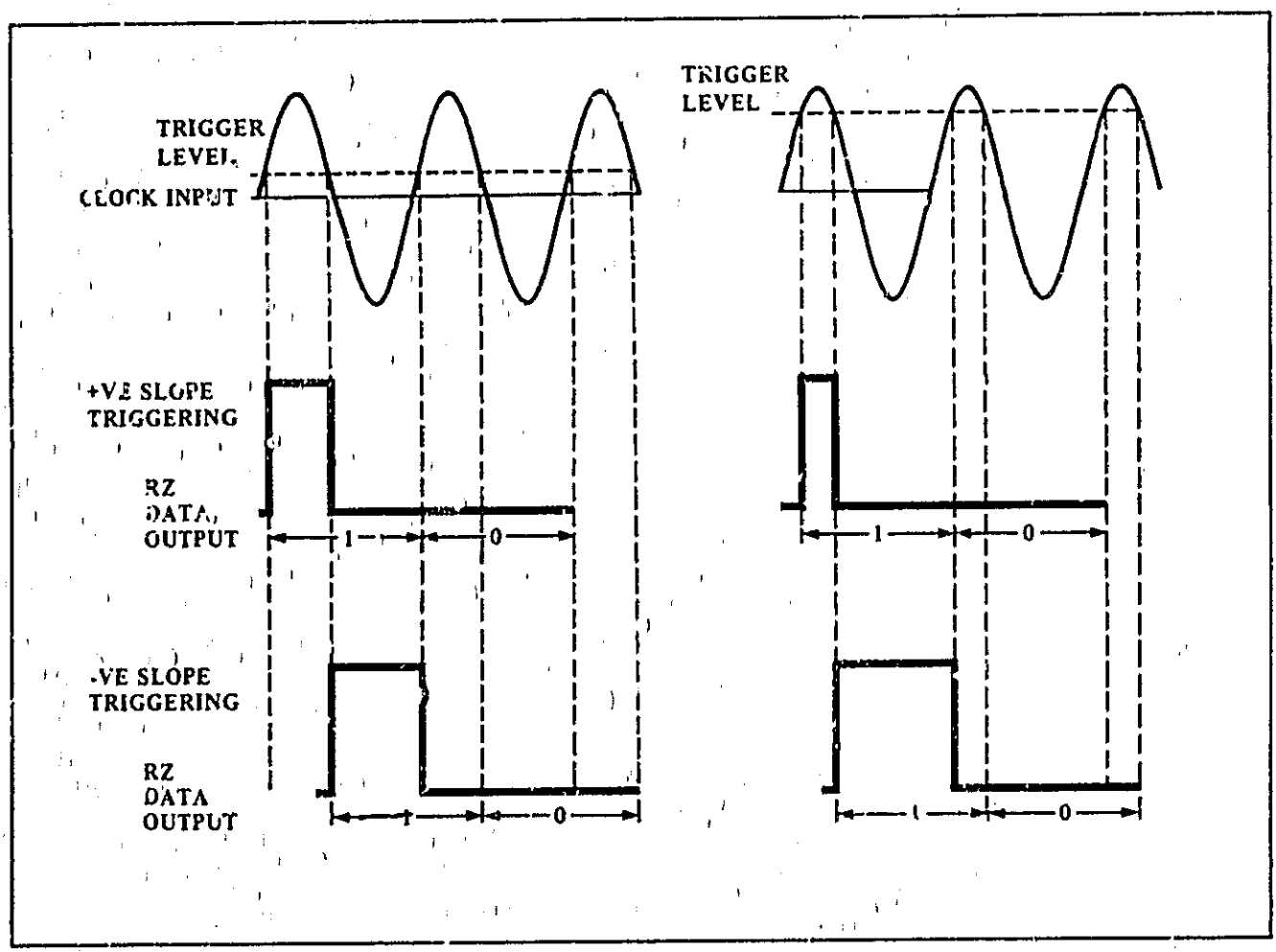


Figure 2-5 Clock Input Triggering/RZ Data Output

2-11 CLOCK OUTPUT

The clock output may either be the external clock input modified by the clock triggering or the output of the optional internal clock generator as shown in Figure 2-6. The output is variable in amplitude and offset with independent, non interacting, controls and may be inverted with the CLOCK/$\overline{\text{CLOCK}}$ switch.

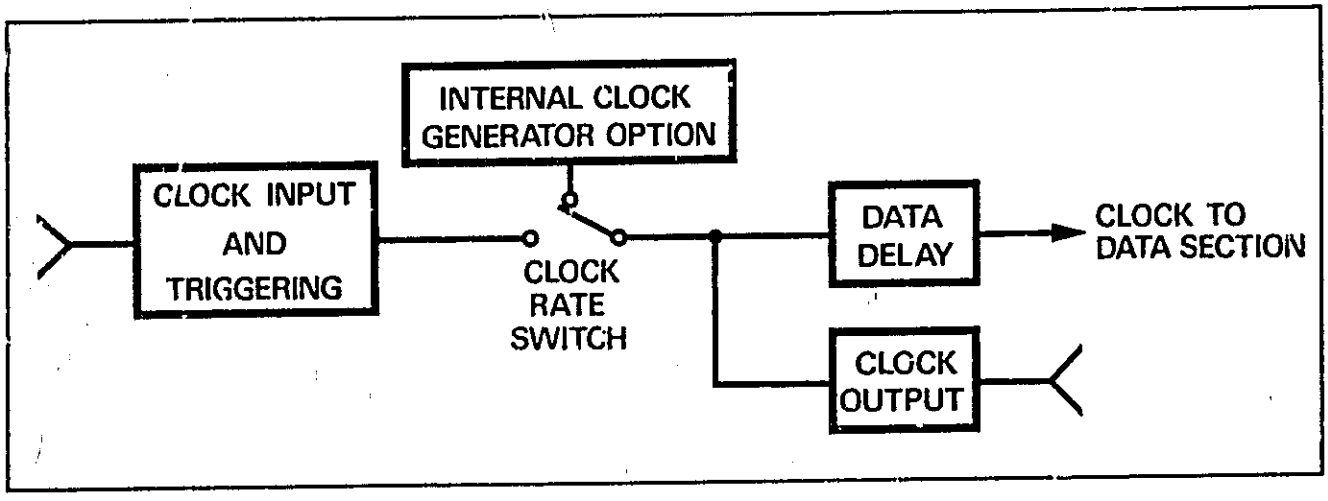


Figure 2-6 Clock Output

Details of offset, amplitude and complementary outputs are given in the Output Control notes on Pages 2-16 and 2-17 as they apply to both clock and data outputs. The mark:space ratio of the clock output is determined by the clock input triggering as shown in Figure 2-7, the clock mark being used to control the RZ data mark as shown in Figure 2-5.

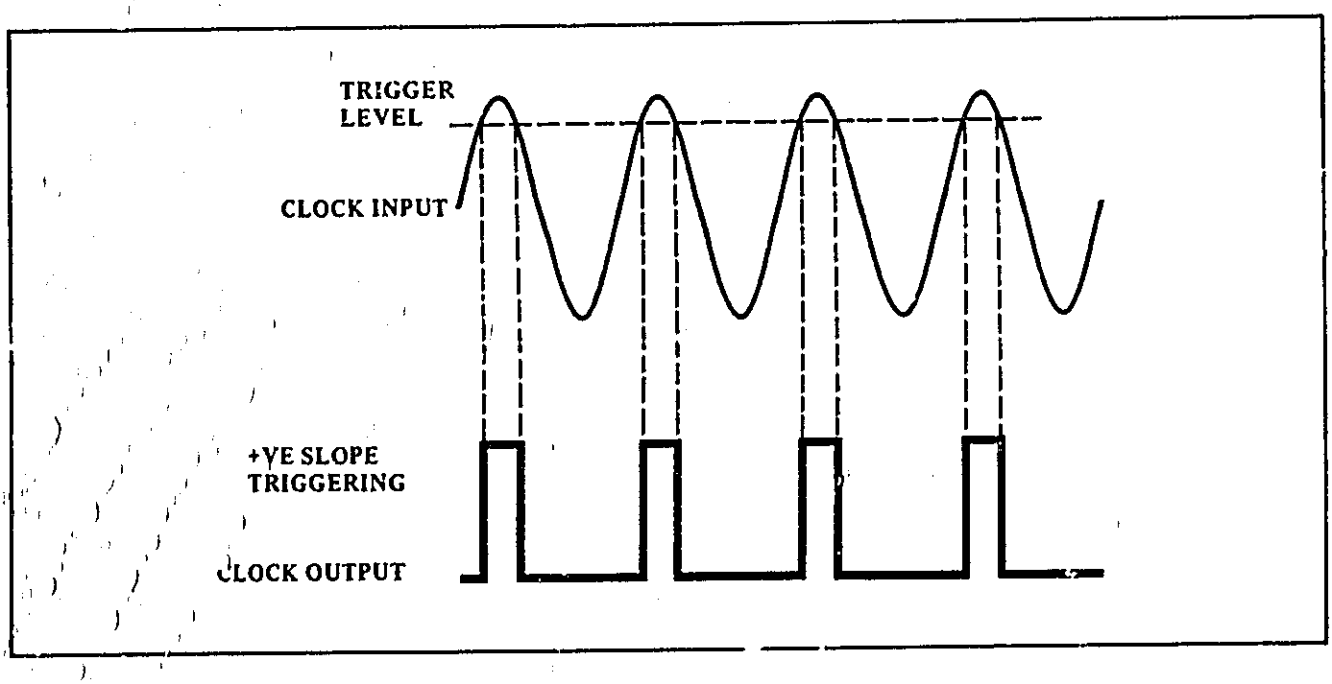


Figure 2-7 Clock Input Triggering/Clock Output

2-12 WORD GENERATION

With the MODE switch in the WORD NORMAL position the length of the word is selected with the REGISTER LENGTH switch and the content with the WORD BIT SELECT switches. When the word length, n bits from 3 to 10, is selected the available positions on the WORD BIT SELECT switches are illuminated to show the bits in use. The selectable bits become available from the left hand end of the WORD BIT SELECT switches as the word length is increased. the extreme left hand switch representing the first output bit. The setting of the WORD BIT SELECT switches is therefore identical to an oscilloscope trace of the data output.The output is a continuous repetition of the selected word with RZ or NRZ format being selected with the FORMAT switch. It should be noted that the n = 15 position of the REGISTER LENGTH switch is not used in the word mode and if selected will produce a 10 bit word. Words which are multiples of shorter words, eg, 110110110 produce a sync pulse for each of the shorter words, and no data or sync is produced for words consisting of all 1's or all 0's. Although these words are not normally used they may be inadvertantly selected when reducing the register length.

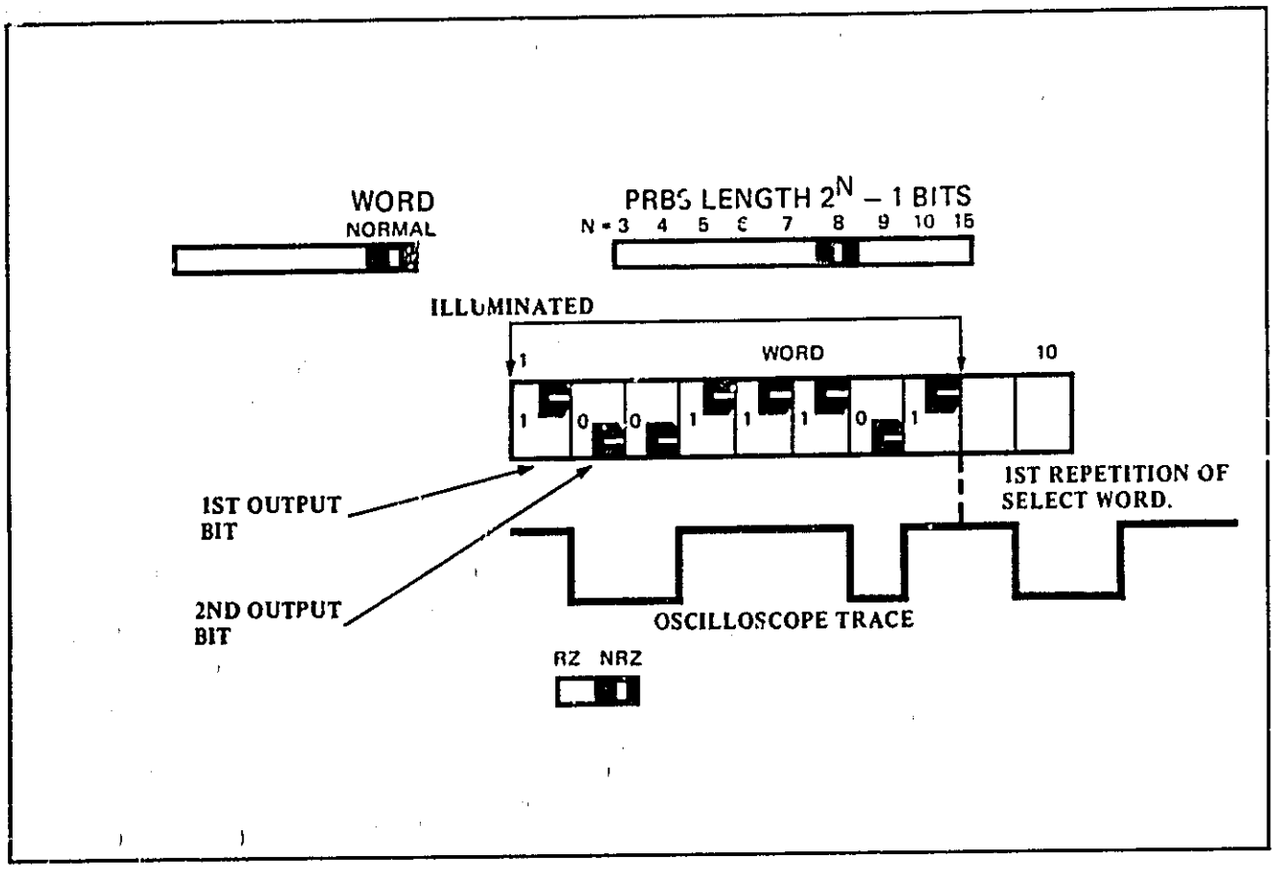


Figure 2-8 Word Generation

OUTPUTS AVAILABLE IN WORD MODE
CLOCK or $\overline{\text{CLOCK}}$, DATA or $\overline{\text{DATA}}$, SYNC PULSE ONCE PER WORD.
FORMAT RZ or NRZ.

2-13 PRBS GENERATION

With the MODE switch in the PRBS NORMAL position the length of the PRBS, $2^n - 1$ bits, is selected with the REGISTER LENGTH switch. This switch is calibrated in values of n from 3 to 10 with an additional value of n = 15. The characteristic equations of the maximal length sequences produced by the feed forward shift register are given in Table 2-2.

Table 2-2 PRBS characteristic equations

Register Length	Characteristic Equation	Sequence Length ($2^n - 1$)
3	$D^3 + D^2 + 1 = 0$	7
4	$D^4 + D^3 + 1 = 0$	15
5	$D^5 + D^2 + 1 = 0$	31
6	$D^6 + D + 1 = 0$	63
7	$D^7 + D + 1 = 0$	127
8	$D^8 + D^4 + D^3 + D^2 + 1 = 0$	255
9	$D^9 + D^4 + 1 = 0$	511
10	$D^{10} + D^3 + 1 = 0$	1,023
15	$D^{15} + D + 1 = 0$	32,767

The following example shows the derivation of the output 7 bit sequence with the n = 3 setting of the REGISTER LENGTH switch. The shift register stages and modulo two adder are switched into the configuration shown in Figure 2-9.

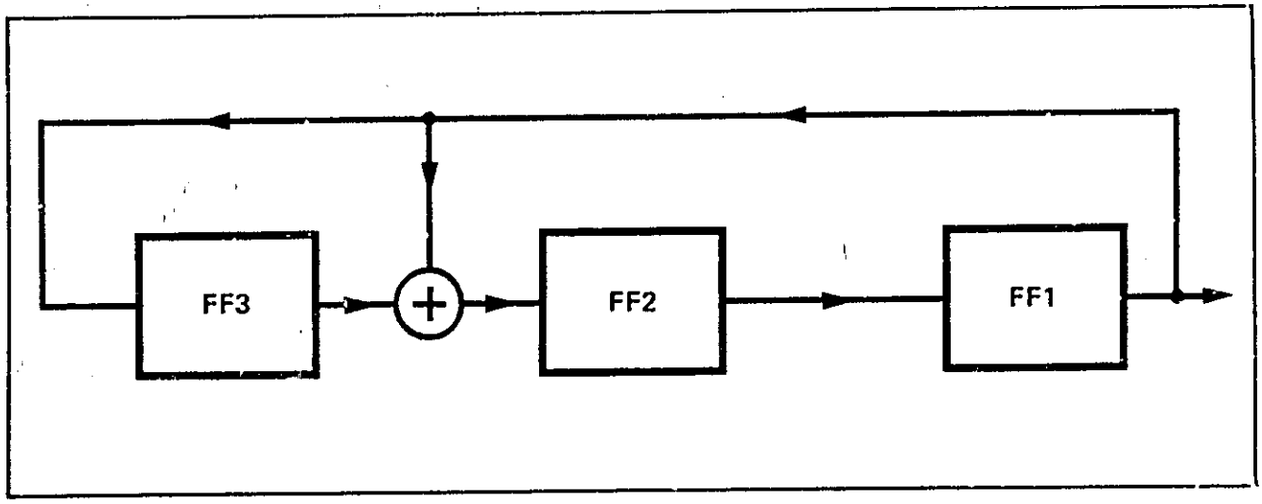


Figure 2-9 The Shift Register shown for n = 3

At each clock pulse the state of FF1 is clocked into FF3, the modulo two addition of the FF1 and FF3 stages is clocked into FF2, and the state of FF2 is clocked into the FF1 stage. If the register is assumed to start in the 100 state then Figure 2-10 shows the successive register states following each clock pulse, the last column or FF1 state indicating the output sequence.

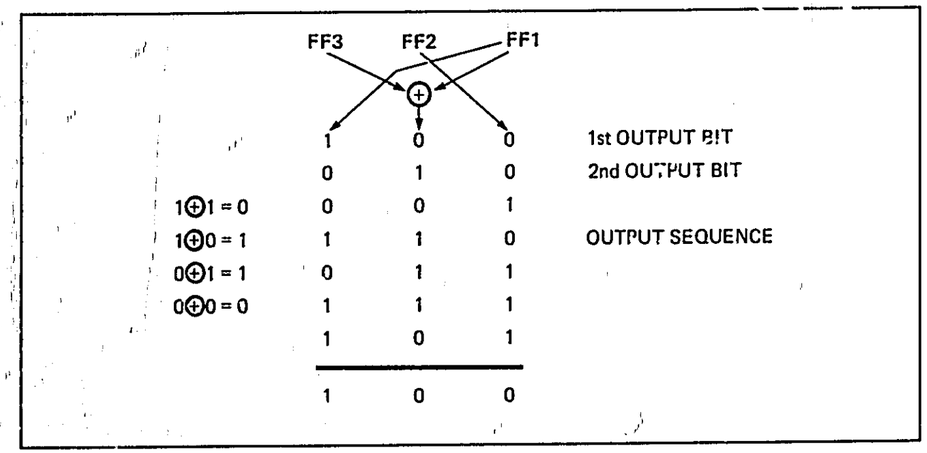


Figure 2-10 States of Shift Register Stages

The output is a continuous repetition of the selected PRBS, RZ or NRZ format being selected with the FORMAT switch. Sync pulses are generated with reference to the WORD BIT SELECT switches, sync pulse notes Page 2-18, and no sync pulses are produced when all of the WORD BIT SELECT switches in use are 0's.

2-14 ZERO ADDITION

A block of 1 to 99 zeros can be added into a WORD or PRBS by selecting the WORD ZERO ADD or PRBS ZERO ADD positions of the MODE switch. The zero block is initiated by, and occurs immediately after, the sync pulse. The position of the zero block in the sequence is therefore controlled by the WORD BIT SELECT switches which determine the position of the sync pulse as shown in the sync pulse notes on Page 2-18. In the WORD ZERO ADD mode the zero block occurs between words and in the PRBS ZERO ADD mode the zero block occurs at the point in sequence determined with the WORD BIT SELECT switches.

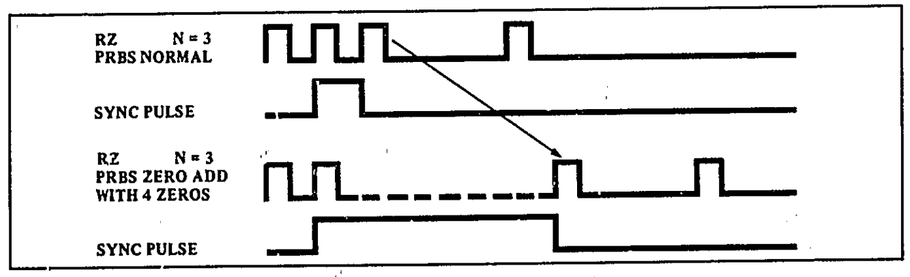


Figure 2-11 Zero addition

2-15 ERROR ADDITION

Selection of PRBS ERROR ADD with the MODE switch deliberately introduces errors by changing two consecutive bits in every 4000 sequences to their logic complements. The actual bits changed are determined by the position of the sync pulse which may be selected with the WORD BIT SELECT switches as shown in the sync pulse notes on Page 2-18. The Error Rate, which will depend on the register length selected, may be used to confirm the correct operation of the 3761A Error Detector. The error rates produced in the error add mode are listed with the sequence lengths in Table 2-3, for all positions of the REGISTER LENGTH switch.

Table 2-3 Error Rates in the PRBS Error Add Mode

REGISTER LENGTH	SEQUENCE LENGTH BITS	ERROR RATE
3	7	7.1×10^{-5}
4	15	3.3×10^{-5}
5	31	1.6×10^{-5}
6	63	7.9×10^{-6}
7	127	3.9×10^{-6}
8	255	1.9×10^{-6}
9	511	9.7×10^{-7}
10	1,023	4.8×10^{-7}
15	32,767	1.5×10^{-8}

2-16 DATA FORMAT

A choice of two data output formats is provided with the FORMAT switch. With the NRZ format a data 1 has the same duration as one clock cycle and with the RZ format a data 1 has the same duration as the 'triggered on' part of the clock input. Figure 2-12 demonstrates the difference between the two formats. The trigger level may affect the RZ data width depending on the clock input waveshape.

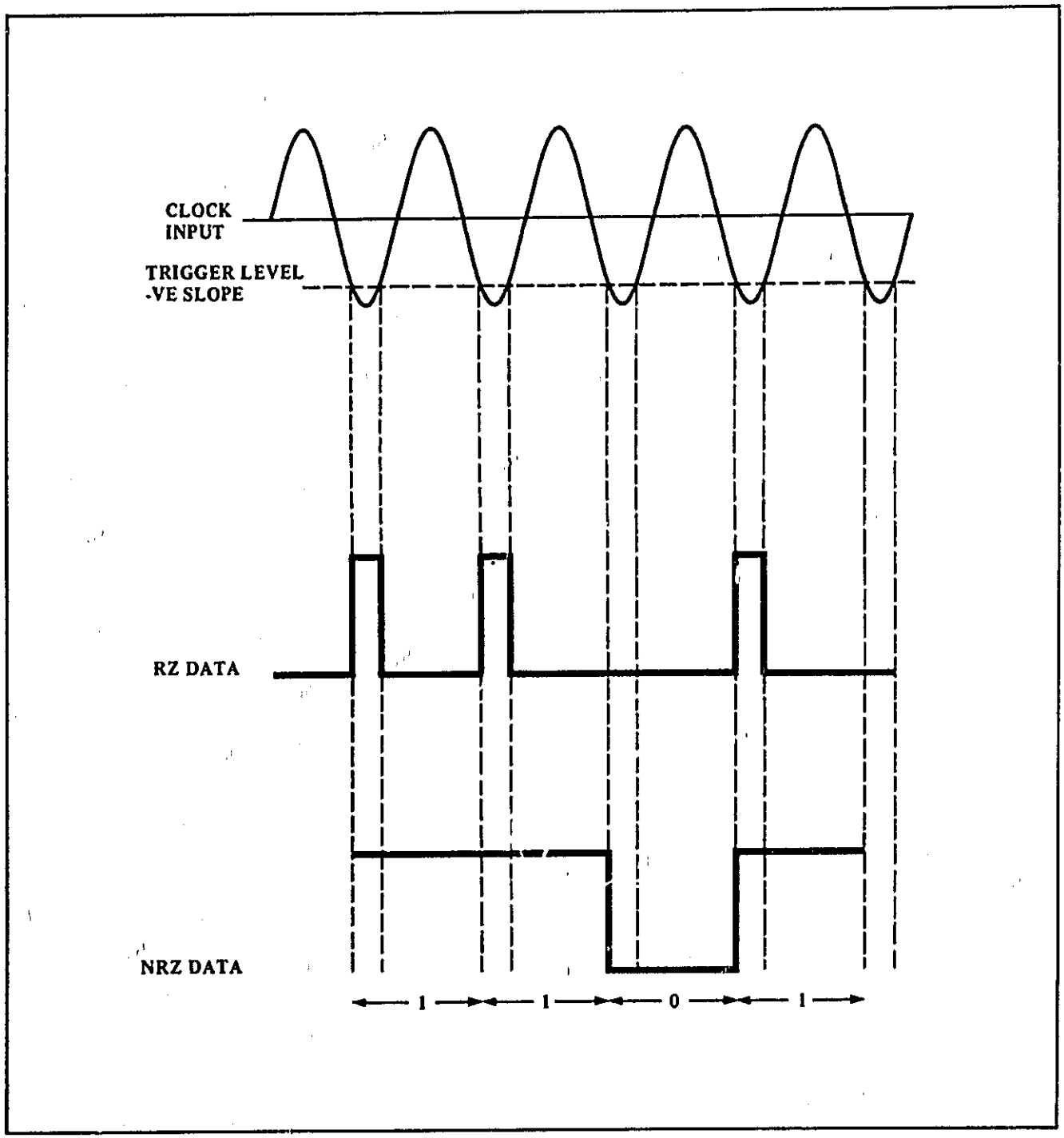


Figure 2-12 RZ and NRZ Formats

2-17 DATA DELAY

The clock input to the data generation circuits may be delayed with the DATA DELAY switch and vernier, the data and sync outputs being subjected to the same delay with respect to the clock output. The DATA DELAY switch is calibrated from 0 to 90ns in 10ns steps and a continuously variable 0 to 10ns delay is provided with the vernier. This facility allows clock and data edges to be aligned in cases where they have been subjected to different delays.

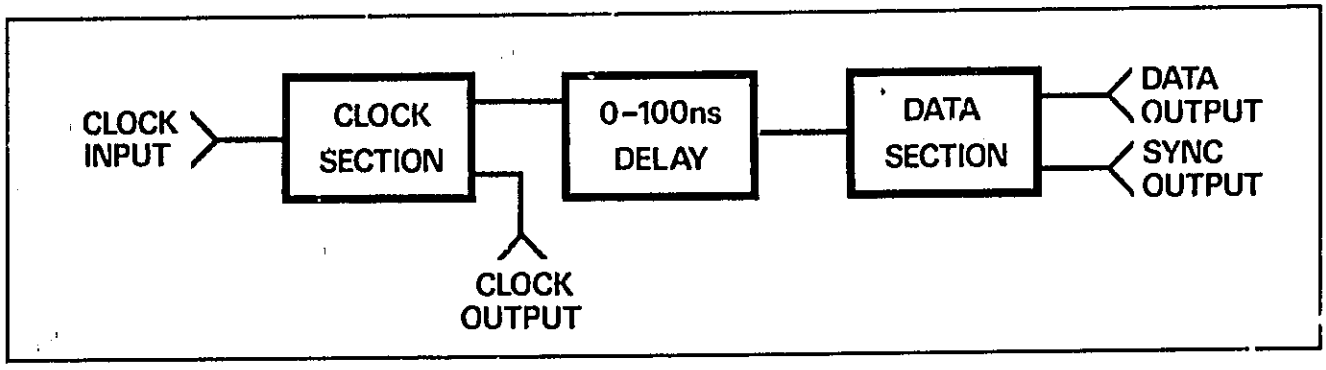


Figure 2-13 Data Delay

2-18 OUTPUT AMPLITUDE AND DC OFFSET

The following information applies to the amplitude and dc offset control of both clock and data outputs. The output amplitude switches which have 5 ranges from 0.1 to 3.2V are calibrated in pk-pk volts and a vernier provides continuous variation over each range. The DC offset switches govern the polarity of the offsets and the associated verniers provide continuous variation of the mean output levels from 0 to 3V. The amplitude and offset controls are not interacting.

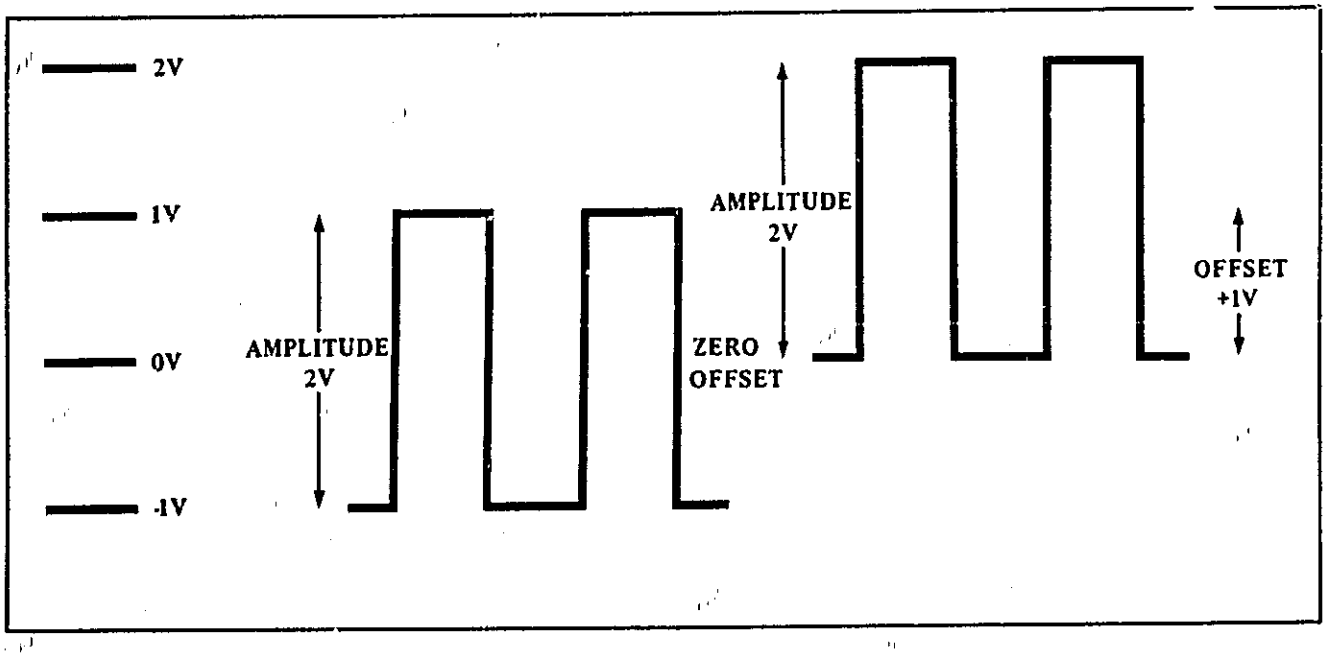


Figure 2-14 Output Amplitude and Offset

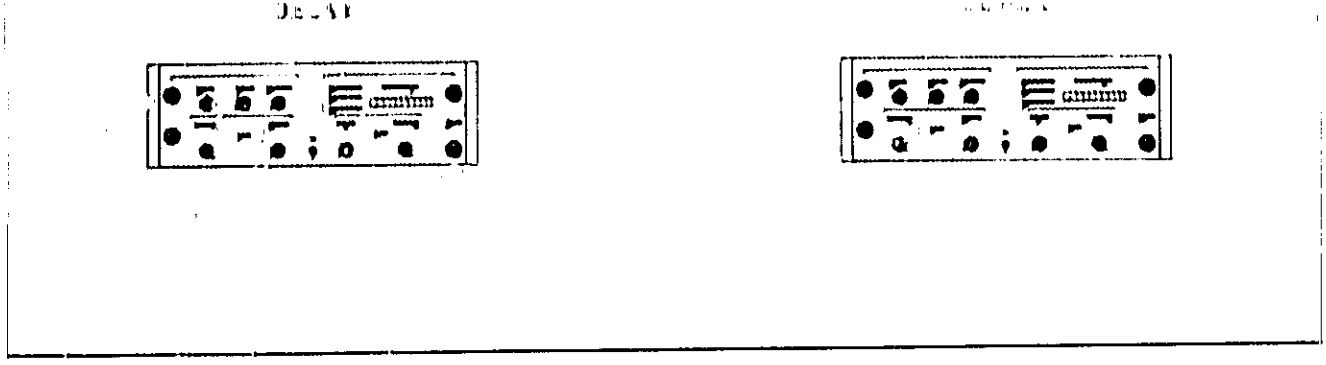


Figure 2-2 Front Panel Functional Areas

2-19 COMPLEMENTARY OUTPUTS

The logic output is complemented when using the $\overline{\text{CLOCK}}$ and $\overline{\text{DATA}}$ outputs. Both $\overline{\text{CLOCK}}$ and $\overline{\text{DATA}}$ may be selected, with individual front panel switches as alternatives to CLOCK and DATA. The amplitude and offset of the complemented outputs remain the same as those for CLOCK and DATA as shown in Figure 2-15.

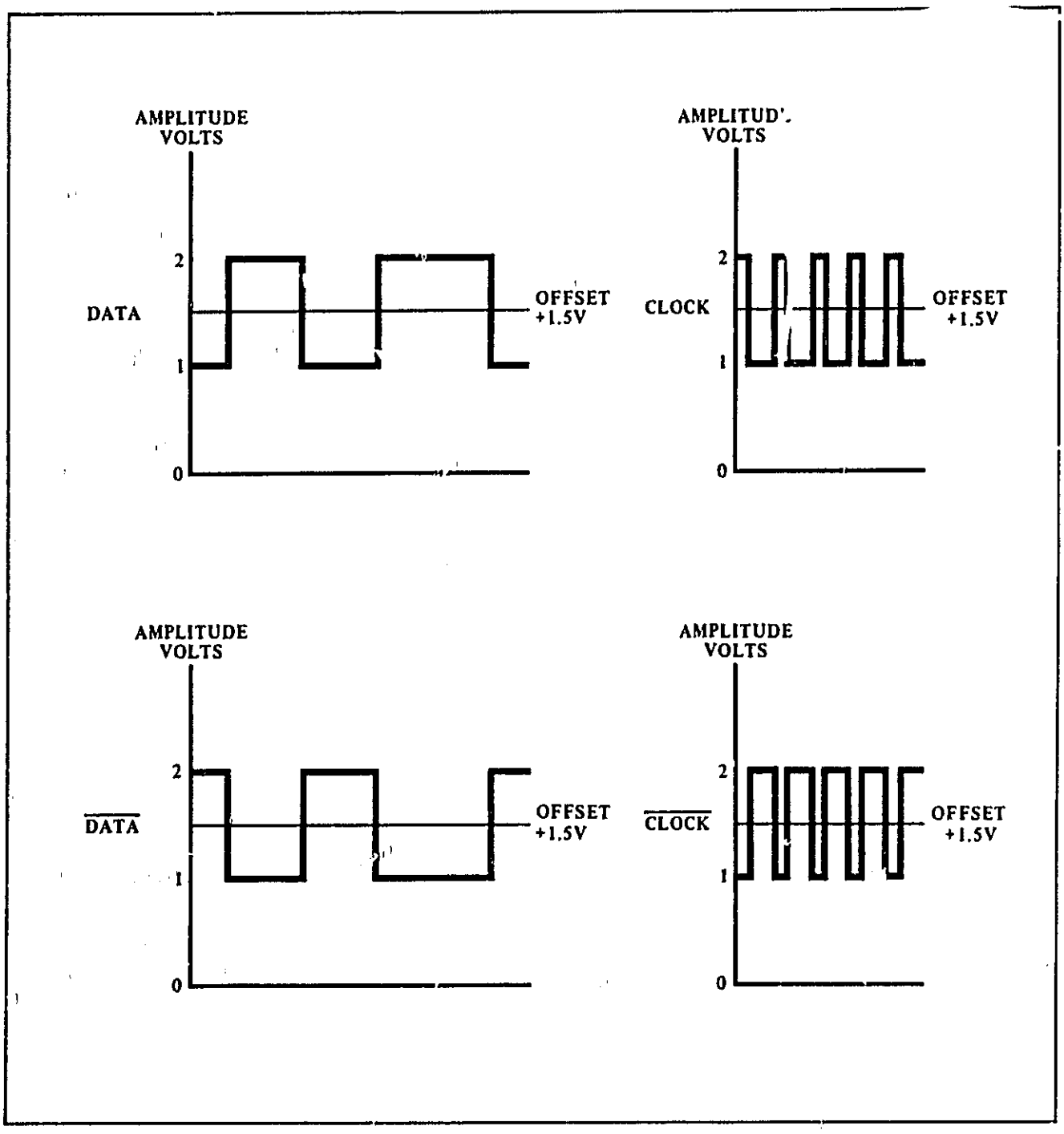


Figure 2-15 Complementary Outputs

2-20 THE SYNC PULSE

A 1V sync pulse is generated during each PRBS or WORD cycle when the shift register stages are in the states indicated by the WORD BIT SELECT switches. In the WORD NORMAL mode a sync pulse of one clock period duration is generated coincident with the last bit of the repetitive word, and the falling edge provides a convenient oscilloscope trigger for observation of the complete word. When the PRBS or WORD, ZERO ADD modes are selected the sync pulse is stretched to the length of the zero block plus one clock period. As the rising edge of the sync pulse initiates the zero block, it occurs one clock period before the first zero and the rising and falling edges may therefore be used as triggers for the examination of the zero block period or the part of the sequence immediately after as shown in Figures 2-16 and 2-17. The effect of delays both within the instrument and in the external cabling may affect the timing of the sync pulse relative to the data.

In the PRBS NORMAL mode with n = 3 to 10 the sync pulse can be generated at any desired point in the sequence by selection of the appropriate configuration of the WORD BIT SELECT switches. This enables the whole of a long PRBS to be examined by sampling successive parts of the sequence (eg, 16 bits) on an oscilloscope triggered with the sync pulse, and advancing the sync pulse for each sample using the WORD BIT SELECT switches.

In order to set the WORD BIT SELECT switches for generation of the Sync pulse at a particular point in the sequence it is necessary to reconstruct the shift register state table for that part of the sequence using the characteristic equations given on Page 2-12. The sync pulse precedes by one bit coincidence between the states of the shift register stages and the states selected with the front panel WORD BIT SELECT switches. This is demonstrated by Figures 2-10 and 2-17. In PRBS modes no sync pulses are produced with a $2^n - 1$ PRBS if the first n WORD BIT SELECT switches are at 0. In the WORD mode, words which are multiples of shorter words, eg 110110110 produce a sync pulse for each of the shorter words. No data or sync is produced for words containing all 1's or all 0's and no sync pulses are produced with the maximum change word 1010.

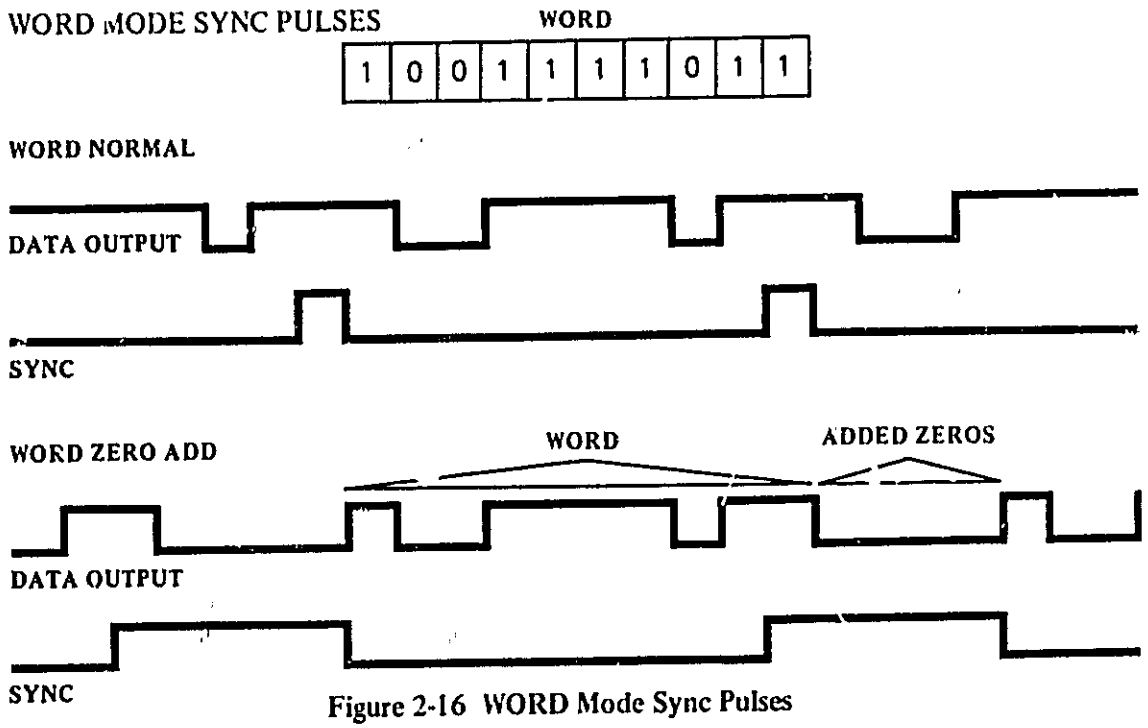


Figure 2-16 WORD Mode Sync Pulses

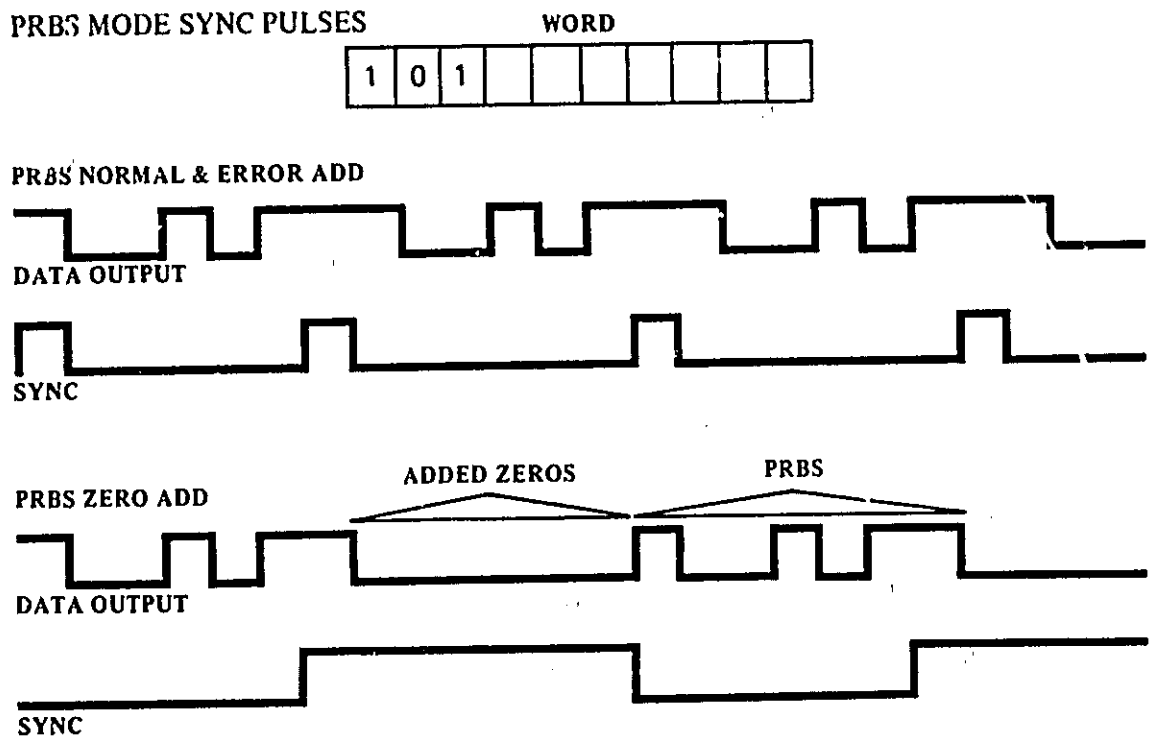


Figure 2-17 PRBS Mode Sync Pulses

NOTE: THE SEQUENCE SHOWN IS THE ONE DERIVED IN PRBS GENERATION PAGE 2-13

3761A Error Detector Specifications

MEASUREMENTS

Bit Error Rate, BER

Range	9.9×10^{-1} to 0.1×10^{-9}, automatically scaled.
Gating	Automatic, at least 100 errors before computation.

Total Error Count, COUNT

Range	0 to 9999.
Gating:	
Internal	Repetitive or single shot
Interval	10^n clock periods where integer n = 5 to 11.
External	Logic level TTL.
Manual	Front panel switch.
Sequences	Maximal length PRBS
Lengths	$2^N - 1$ where N = 3 to 10 and 15.

CLOCK INPUT

Rate	1.5 to 150MHz.
Impedance	50Ω ±5% dc coupled (75Ω optional).
Trigger:	
Slope	+ve or -ve.
Manual	Level range -3 to +3V.
Auto	Input mark:space ratio range 10:1 to 1:10.
Sensitivity	Better than 500mV pk-pk.
Amplitude	5V pk-pk max. Limits ±5V.
Pulse Width	3ns minimum at 50% pulse amplitude.

DATA INPUT

Input	DATA or $\overline{\text{DATA}}$, selectable.
Rate	1.5 to 150Mb/s.
Impedance	50Ω ±5% dc coupled (75Ω optional).
Trigger Level	Automatic. Input mark:space ratio range 10:1 to 1:10.
Sensitivity	Better than 500mV pk-pk.
DC Offset	±3V maximum.
Amplitude	5V pk-pk max. Limits ±5V.
Pulse Width	5ns minimum at 50% pulse amplitude.

PHASING

Control	Clock phase variable relative to data.
Indication	Lamp off when clock and data edges coincide.

Range:

1.5 to 50Mb/s	50 to 150Mb/s
0 to 180°.	0 to 12ns.

SYNCHRONISATION

Modes:	Auto, Manual, External
	External and Manual initiate single shot Auto sync.
Auto	Automatically searches for synchronism if more than 20,000 errors in 100,000 bits.
External	Resynchronisation commanded by TTL input.
Manual	Resynchronisation commanded from front panel

DISPLAY

BER	Two digits plus exponent a.b x 10^{-x}.
COUNT	Four digits.
Flags	Sync loss, overflow and gating.

OUTPUTS

Printer	8421 BCD.
BER and COUNT	Current display on command.
Flags:	
Sync loss	0 printed in column 1.
Overflow	Output inhibited.
Print command	Pulse at display change.
Error output	
Rate	One pulse per error.
Amplitude	+1V into 50Ω nominal.

ACCURACY

BER	Computation based on at least 100 errors.
COUNT	Internal gating, ±1 error.

OPTIONS

Option 001	75Ω CLOCK and DATA input impedances.
Option 002	Printer interface cable.

GENERAL

Power	90 to 125 or 200 to 250V 40 to 400Hz, consumption 70W	Weight	23lbs. 10.4kg.	Dimensions	16¾in wide, 3¾in high, 18¾in deep (425mm x 95mm x 467mm).

SECTION III
OPERATING THE 3761A ERROR DETECTOR

3-1 INTRODUCTION

The 3761A Error Detector has a built-in counter with two modes of operation: Bit Error Rate, BER, and Total Error Count, COUNT. In BER mode the measurement is displayed in the form a.b x 10^{-X}. In COUNT mode the errors accumulated in a chosen interval are displayed as a four digit number with leading zeros blanked.

The Error Detector has been specifically designed for operation with the pseudo random sequences produced by the 3760A Data Generator. It requires both clock and data inputs, and performs error detection using bit-by-bit comparison with an internally generated, closed loop, reference sequence. This technique ensures detection of every error, random or systematic, and avoids the problems associated with open loop reference sequence generation.

The BER measurement is computed from more than 100 errors, and has a range of 9.9 x 10^{-1} to 0.1 x 10^{-9}. The total error count, COUNT, which has a range of 0 to 9999, is provided with both internal and external gating. The internal gating period can be selected within the range 10^5 to 10^{11} clock decades and can be single shot or repetitive in operation. A TTL compatible external gate input is provided, and manual gating is controlled with a front panel stop/start switch. In both BER and COUNT modes the display is continually updated at a rate which may be set by the operator.

The 3761A Error Detector clock input (impedance 50Ω, optionally 75Ω), accepts regular waveshapes in the frequency range 1.5 to 150MHz. It has a sensitivity of better than 500mV pk-pk and can be triggered manually or automatically on the +ve or -ve slope of the input waveform. The range of the manual trigger control is +3 to -3V and indication of correct trigger is given by a front panel lamp. The auto trigger will accept mark:space ratios in the range 10:1 to 1:10 subject to a 3ns minimum pulse width.

A front panel variable phase control is used to ensure that coincidence between clock and data edges is avoided. At frequencies up to 50MHz the control range is 0 to 180° and from 50 to 150MHz it is 0 to 12ns. A lamp indicates when a correct phase relationship between the clock and data has been attained.

Synchronisation of the 3761A Error Detector to the incoming data can be accomplished automatically, manually, or externally. In the automatic mode, correct synchronism is ensured by continually monitoring the average error rate over a period long enough to remove the effect of error bursts. In the manual synchronisation mode the Error Detector searches for synchronism on command from a front panel switch, and in the external mode by command from an external TTL signal.

A BCD output of the current display is available from a rear panel socket. This output is in 8421 format and includes the sync loss and overflow flag indications. An output of one pulse per error is also available at the rear panel for further analysis.

3-2 OPTIONS

OPTION 001 is provided with 75Ω clock and data input impedances and OPTION 002 is provided with an interface cable suitable for use with *hp* 5050B and 5055A printers. Both options are available on the same instrument if required.

3-3 ACCESSORIES

The instrument is provided with a three core power cable, two extender boards clipped behind the modules, a 2A fuse, stock number 2110-0303 for 115V operation, and a rack mounting kit.

3-4 FUSE RATINGS AND LOCATION

Table 3-1 provides a list of all fuses in the instrument and Figure 3-1 shows their location.

Table 3-1 Fuse Ratings

Fuse		Rating	*hp* Stock Number
F1	Main Supply 230V Main Supply 115V	1A slow-blow 2A slow-blow	2110-0007 2110-0303
F2	-5.2V	5A	2110-0010
F3	+5V	3A	2110-0003
F4	-15V	1.5A	2110-0043
F5	+15V	2A	2110-0062

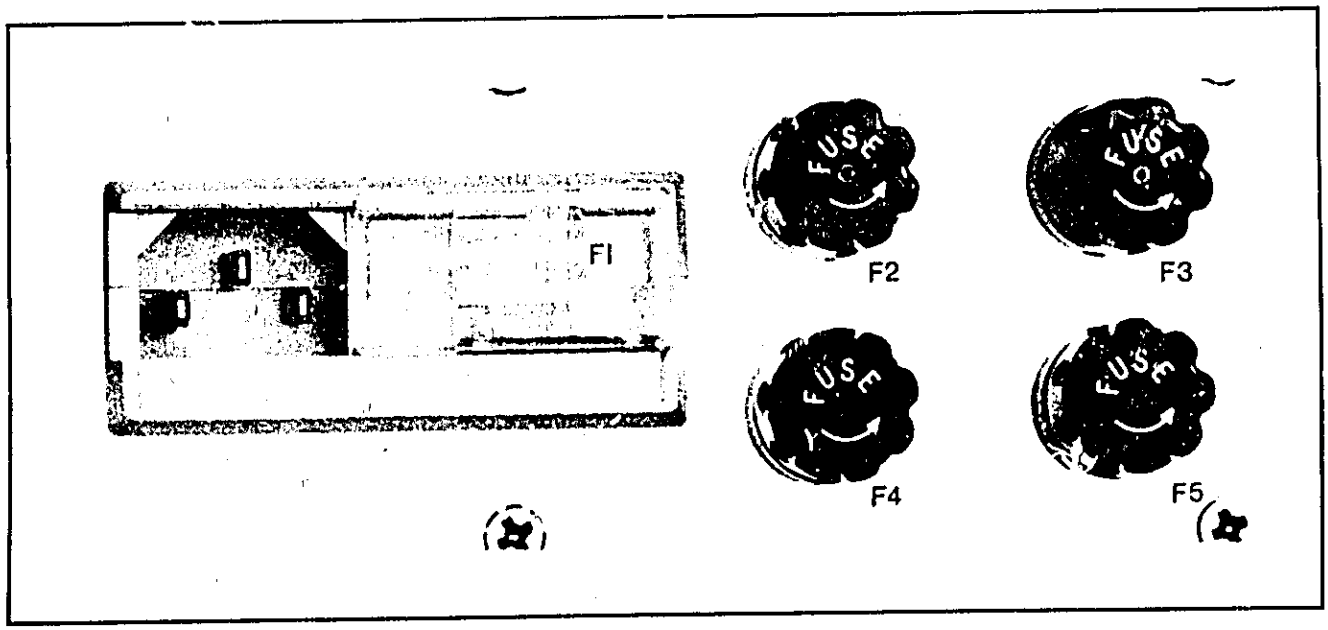


Figure 3-1 Fuse location on Rear Panel

3-5 THE FRONT PANEL

The front panel may be divided into functional areas as shown in Figure 3-2. The description of the controls, connectors and indicators, given on pages 3-4 to 3-7, is divided into the same functional areas.

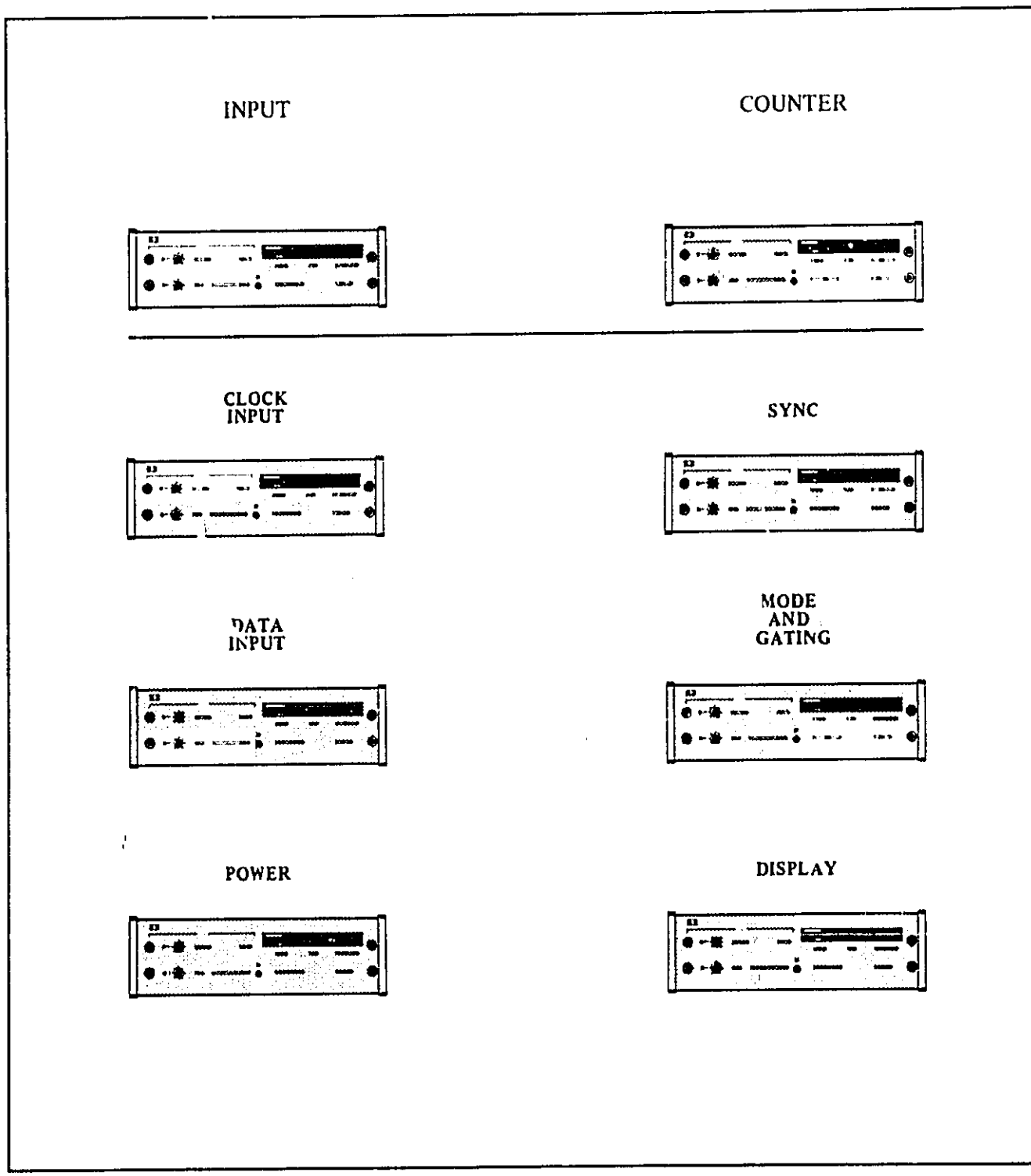
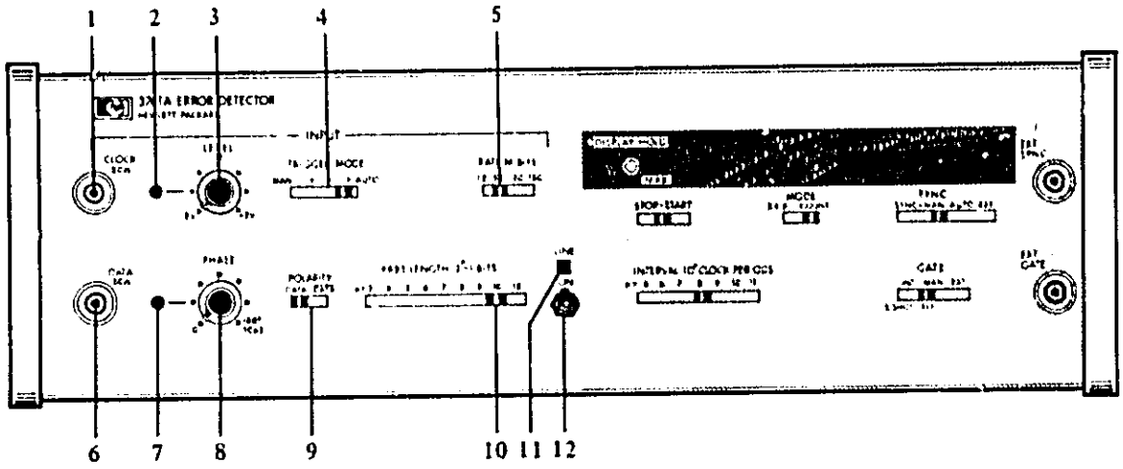
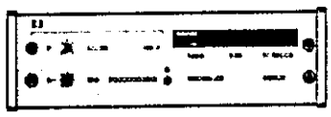


Figure 3-2 Front Panel Functional Areas

3-6 Controls, Connectors and Indicators
3-7 INPUT CONTROLS



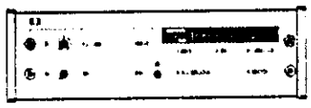
CLOCK INPUT



1. CLOCK INPUT 50Ω requires input synchronous with data. Input levels, minimum 500mV pk-pk, maximum ±5V.
2. TRIGGER INDICATOR LAMP. The Error Detector clock circuits are triggered when the lamp is ON.
3. TRIGGER LEVEL VERNIER sets MANUAL trigger level between +3 and -3V.
4. TRIGGER MODE switch selects AUTO or MANUAL clock trigger and +ve or -ve slope.
5. RATE SWITCH selects input frequency range for PHASE control. 0 to 180° PHASE range for 1.5 to 50MHz and 0 to 12ns range for 50 to 150MHz.

Figure 3-3 Input Controls

DATA
INPUT



6. DATA INPUT 50Ω accepts sequences from 3760A Data Generator. Input levels, minimum 500mV pk-pk, ±5V maximum.

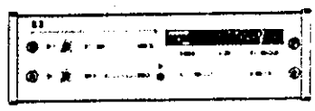
7. PHASE INDICATOR LAMP. Lamp ON when clock and data edges not coincident.

8. PHASE CONTROL VERNIER sets the relative phase of clock and data. The range is 0 to 180° for 1.5 to 50MHz and 0 to 12ns for 50 to 150MHz. The frequency range is selected with the RATE switch 5.

9. POLARITY SWITCH selects DATA or $\overline{\text{DATA}}$ to allow for data inversion in the item or system under test.

10. PRBS LENGTH SWITCH selects the register length of the internal reference sequence generator. The setting of this switch must be identical to the setting of the 3760A Data Generator register length switch.

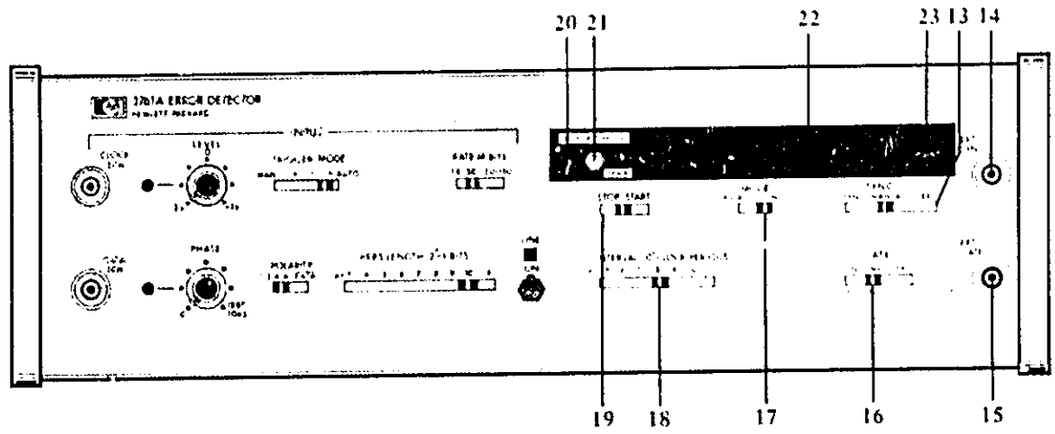
POWER



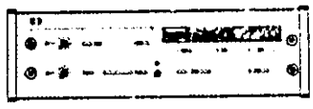
11. LINE INDICATOR LAMP indicates state of switch 12.

12. LINE ON/OFF SWITCH connects supply to power supply transformer primary.

3-8 COUNTER CONTROLS



SYNC

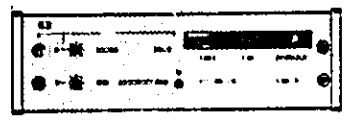


13. **SYNC SWITCH** selects synchronisation mode, automatic, manual or external. In MAN and EXT the instrument searches for synchronism only with a manual or TTL logic command. Manual control by selecting SYNC position or external control with input 14.

14. **EXT SYNC INPUT** accepts TTL pulses when EXT is selected with SYNC switch 13. A negative going edge causes a search for synchronisation to take place.

Figure 3-4 Counter Controls

MODE
AND
GATING



15. EXT GATE INPUT. The gate is held open while the TTL input is held positive.

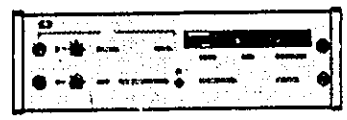
16. GATE SWITCH. In the MAN or EXT positions the error count is controlled by a manual or TTL logic command. Manual control switch 19 or external input 15. In the INTERNAL SINGLE SHOT and REPETITIVE positions the gating interval is selected with the INTERVAL switch 18.

17. MODE SWITCH selects operating mode, BER or gated COUNT.

18. INTERVAL SWITCH selects gating interval from 10^5 to 10^{11} clock periods.

19. STOP/START SWITCH controls the counter when GATE switch 16 is in the MAN or SINGLE SHOT positions

DISPLAY



20. STROBED LAMP indicating display refreshment times, controlled by 21.

21. DISPLAY HOLD CONTROL varies the refreshment rate of the display from 200 milliseconds to 3 seconds approximately.

22. LED DISPLAY. Four digits in COUNT mode. Two digits and exponent of 10 (a.b x 10^{-X}) automatically scaled in BER mode.

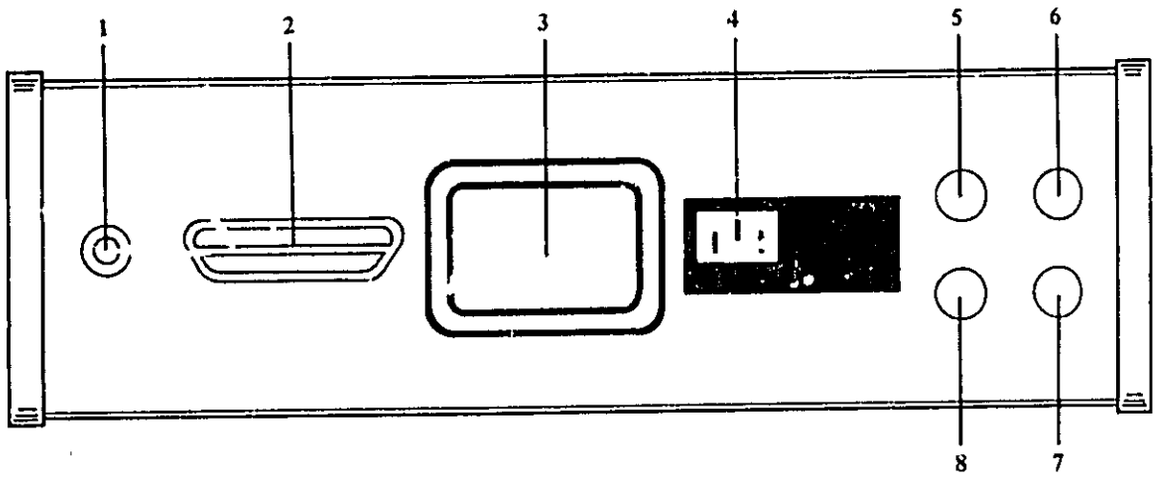
23. FLAG SIGNALS are displayed as follows:

GATING when the error counter is accumulating errors.

SYNC LOSS during a search for synchronism. The flag is retained until the next measurement is displayed.

OVERFLOW when the error count or display overflow. The flag is retained until the next measurement is displayed.

3-9 The Rear Panel



1. ERROR OUTPUT provides one pulse per error in both BER and COUNT modes. The pulse width is the same as the clock input pulse and its amplitude is +1V into 50Ω.
2. BCD OUTPUT is a printer output of the current display and flag information in 8421 BCD format. The measurement result is available for the duration of the print command pulse.
3. AIR FILTER. Information on the instrument forced air cooling and air filter is given on Page 1-3.
4. POWER INPUT CONNECTOR containing supply fuse F1. Details of power requirements, fuses, and the selection of 115 or 230V operation are given on Page 1-2.
5. F2, 5A fuse for -5.2V supply.
6. F3, 3A fuse for +5 supply.
7. F5, 2A fuse for +15V supply.
8. F4, 1.5A fuse for -15V supply.

Figure 3-5 Rear Panel Controls

3-10 SETTING-UP PROCEDURE

Before any measurements are made the sequence length, data polarity and clock/data phasing must be correctly set; other control settings depending on the measurements to be made. The normal setting up procedure is listed below and is required for all measurements.

1. Set the sequence length switches on the Data Generator and Error Detector to the same length.

2. Connect the clock and data signals to their respective inputs.

3. Select manual or auto triggering, +ve or -ve slope as required for clock. If operating with manual triggering set the trigger level control until lamp is ON.

4. Set the data polarity for normal or inverted data.

5. Set the RATE switch to the range which includes the incoming bit rate and adjust the PHASE control for correct phasing of the clock and data channels. The phasing is correct when the phase indicator lamp is ON although in RZ operation at high frequencies the phasing may be correct without this indication. In this case adjust for minimum error rate.

6. Set the SYNC MODE switch to the form of resynchronisation required.

NOTE: Incorrect settings will produce a sync loss display flag, or an incorrect display.

3-11 OPERATIONAL NOTES

The 3761A Error Detector operational notes are divided into four groups which are presented in the following order.

PHASING AND SYNCHRONISATION	Clock/data phasing. Synchronisation.
MEASUREMENTS	The BER mode. The count mode.
DISPLAY	Refreshment rate. Flag signals.
OUTPUTS	BCD output. Error output.

3-12 CLOCK/DATA PHASING

The PHASE control is provided so that coincidence between clock and data pulse edges may be avoided, a condition necessary for correct sampling of the data pulse with the clock pulse edge. Either a delay or phase change may be introduced depending on the input bit rate, the PHASE control ranges being selected with the RATE switch. For bit rates of 1.5 to 50Mb/s the range is 0 to 180° and for bit rates of 50 to 150Mb/s it is 0 to 12ns.

The phase lamp indicates coincidence between clock and data edges when it is out. When using NRZ format, or RZ format at bit rates up to 100Mb/s, correct phasing is indicated when the lamp is on, the best sampling point being at the mid position between two coincidence points. In RZ format at bit rates above 100Mb/s the best sampling point may be determined by adjusting the PHASE control for minimum error rate.

Incorrect adjustment of the PHASE control may result in loss of synchronisation which will be indicated by the SYNC LOSS flag. An incorrect display may result from incorrect PHASE adjustment.

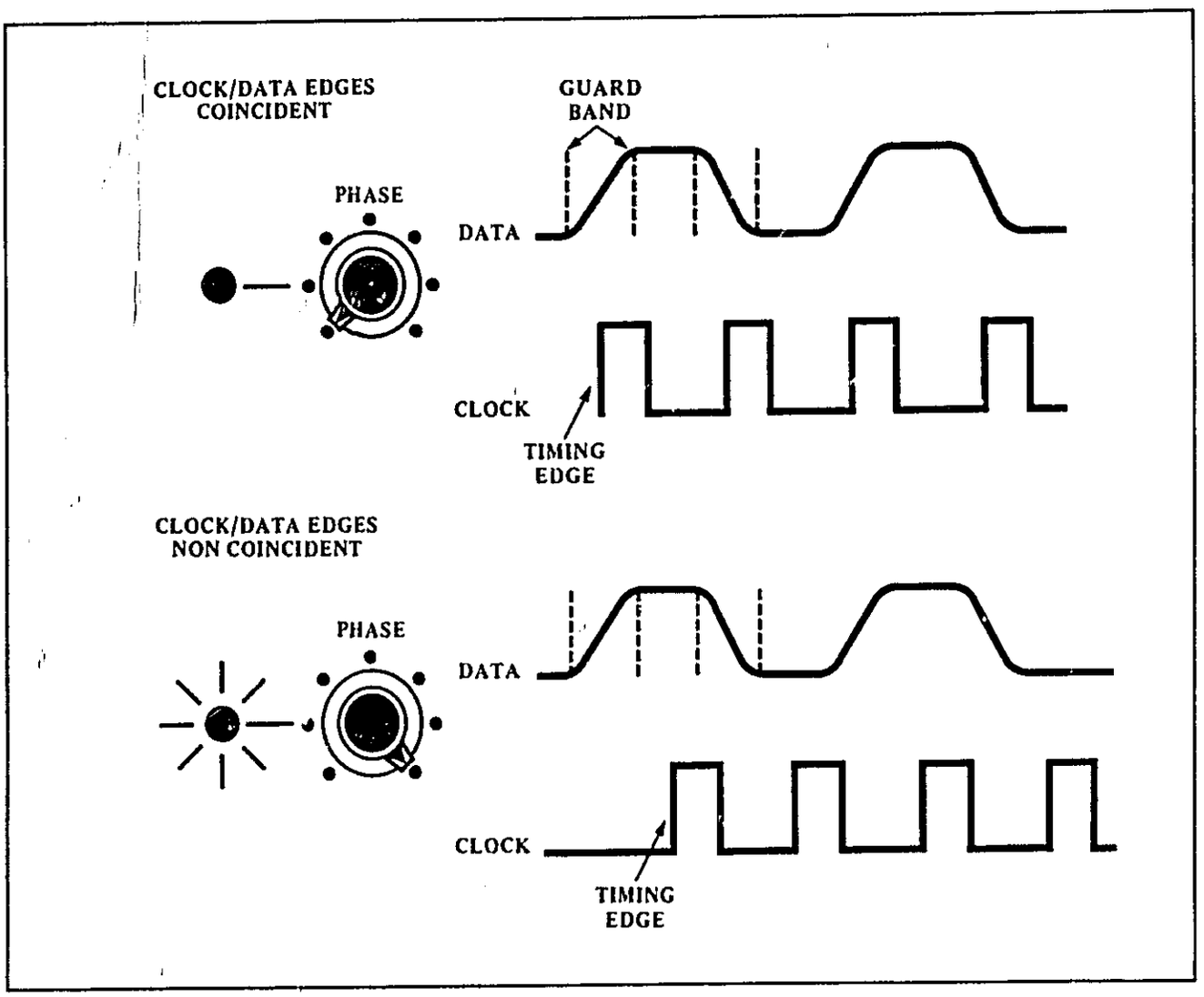


Figure 3-6 Clock/Data Phasing

3-13 SYNCHRONISATION

The reference sequence produced by the Error Detector has to be synchronised to the incoming sequence before comparison can take place. This Synchronisation is achieved by using part of the incoming sequence to set the stages of the reference sequence generator to the correct states.

Three modes of synchronisation are available for selection with the SYNC switch: automatic (AUTO), manual (MAN), and external (EXT).

In the AUTO mode the synchronism of the reference sequence is continually checked over periods of 100,000 clock bits and the detection of 20,000 errors constitutes loss of synchronism. If synchronism has been lost a search is automatically initiated and continues until it is found again.

In the MANUAL and EXTERNAL modes a search for synchronism will only be initiated by an external command. In the case of manual this takes the form of a spring loaded control, the SYNC switch position, and in external the command is the -ve going edge of a TTL logic pulse. These two modes allow the initiation of the search for synchronism to be completely under the control of the operator if the criterion used in the AUTO mode is unsuitable.

During any search for synchronism the display is automatically blanked and SYNC LOSS is flagged.

3-14 THE BER MODE

With the MODE switch set to BER follow the setting up procedure on Page 3-9. The method of measurement in the BER mode is to accumulate 100 errors, continue counting until the next clock decade is reached, and then to display the two most significant digits of the error count with an exponent derived from the clock counter as shown in Figure 3-7.

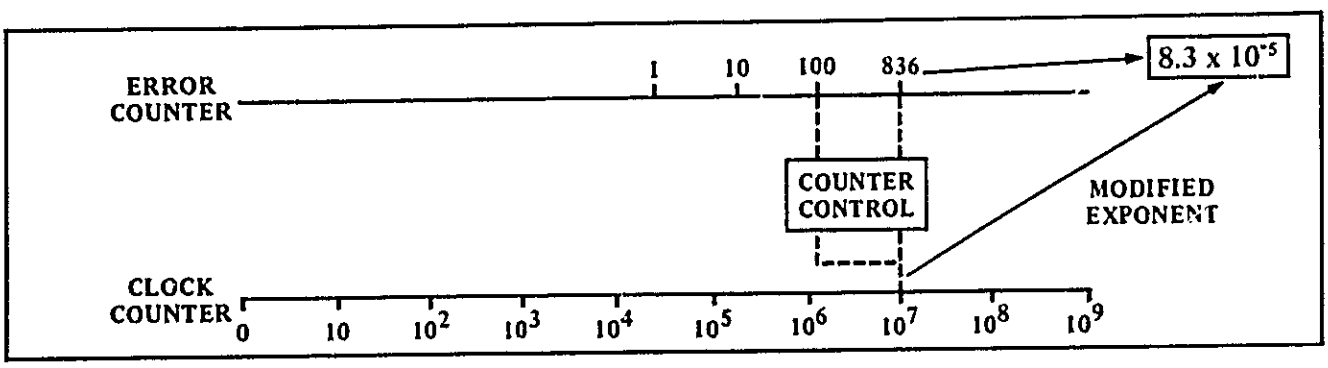


Figure 3-7 BER Measurement

If sync loss is continuously flagged check the following:

Error Detector phase and data polarity are correctly set.
Data Generator and Error Detector sequence lengths are the same.
Time has been allowed for a measurement to be completed after a search for synchronism, if the gating flag is on.

The Gating flag indicates that synchronism has been achieved and that the counter is in operation. This is particularly useful at low error rates when a significant time might elapse before the first 100 errors are accumulated.

At very low error rates operation of the measuring system may be confirmed by inserting a deliberate error once per 2000 sequences. The error rates are given in Table 2-3, Page 2-14.

In the BER mode the display rate is controlled with the DISPLAY HOLD control and an indication of the refreshment rate is given by the strobe lamp on the display. Operation of this lamp is described in the flag signal section on Page 3-15.

3-15 SYNC MODES AVAILABLE WITH BER OPERATION

Manual, Auto, External.

Synchronisation mode details are given on Page 3-12.

3-16 OUTPUTS AVAILABLE IN BER MODE

LED display of BER, BCD output of current display. One Pulse per error.

3-17 THE COUNT MODE

With the MODE switch set to COUNT follow the Setting-up Procedure on Page 3-9. Four gating methods are provided and details of each method are given below:

EXTernal — The gating interval is the duration of a TTL high level at the EXT GATE INPUT. The counter starts with the rising edge and stops with the falling edge.

MANual — Counter operation with manual gating is controlled with the STOP/START switch. The counter stops when the STOP switch contacts are made, and starts when the START switch contacts are broken.

INTernal — The gating interval in both single shot and repetitive is 10^n clock periods where values of integer n between 5 and 11 may be selected with the INTERVAL SWITCH.

In SINGLE SHOT the counter is started with the START/STOP switch, and in REPETITIVE successive starts are automatic.

When setting up the gating interval at low error rates it may be useful to measure the error rate in the BER mode. The gating period can then be selected to provide good resolution, ie to give a high counter reading without overflowing.

With internal repetitive gating the display rate is controlled with the DISPLAY HOLD control and an indication of the refreshment rate is given by the stobe lamp on the display. Operation of this lamp is described in the Flag signal section on Page 3-15.

3-18 SYNC MODES AVAILABLE WITH COUNT OPERATION

Manual, Auto, External

Synchronisation mode details are given on Page 3-12.

3-19 OUTPUTS AVAILABLE IN COUNT MODE

LED display of COUNT, BCD output of current display. One pulse per error.

3-20 REFRESHMENT RATE

At high error rates the measurements may be completed faster than they can be read from the display. In order to reduce the rate of change of the display, refreshment rate, a hold control is provided which holds the measurement and delays the display change for periods of 200ms to 3s approximately. A strobed lamp is provided, on the left hand side of the display, to indicate the times at which the display may be refreshed. The display changes at the first refreshment time after the completion of a measurement as shown in Figure 3-8. When the display can be refreshed faster than measurements can be made, the strobed lamp will indicate possible refreshment times.

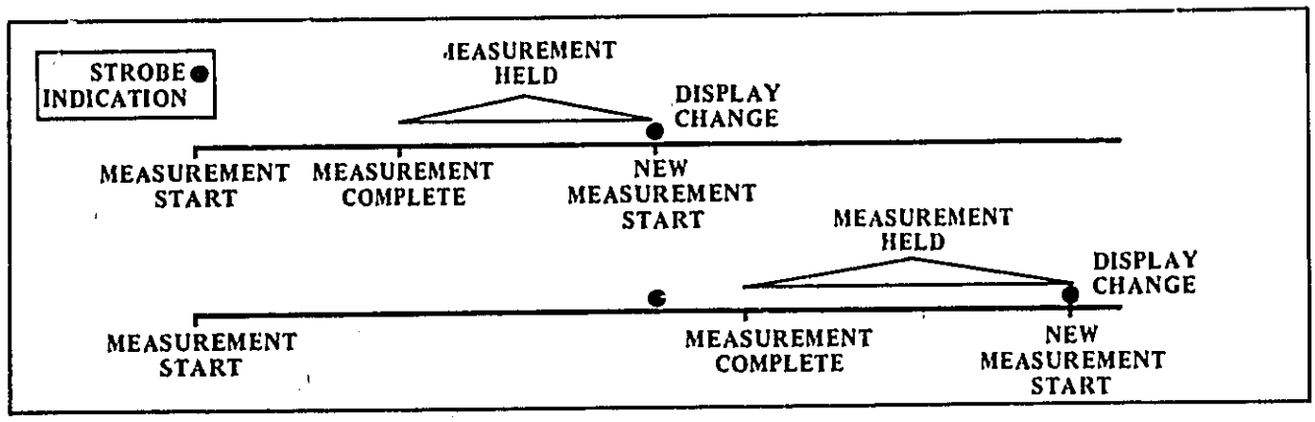


Figure 3-8 Display Refreshment

3-21 FLAG SIGNALS

The three flag signals, GATING, SYNC LOSS, and OVERFLOW, provided on the display, apply to both BER and COUNT modes of operation. The conditions indicated by these flag signals are listed below:

GATING indicates that an error count is taking place.

SYNC LOSS indicates that a search for synchronism is taking place or took place before the current measurement.

OVERFLOW indicates display overflow in COUNT and error counter overflow in BER. The flag will continue to be indicated until a fresh computation has been made.

The display of the current BER or COUNT is blanked during SYNC LOSS and OVERFLOW conditions. Two typical displays are shown in Figure 3-9.

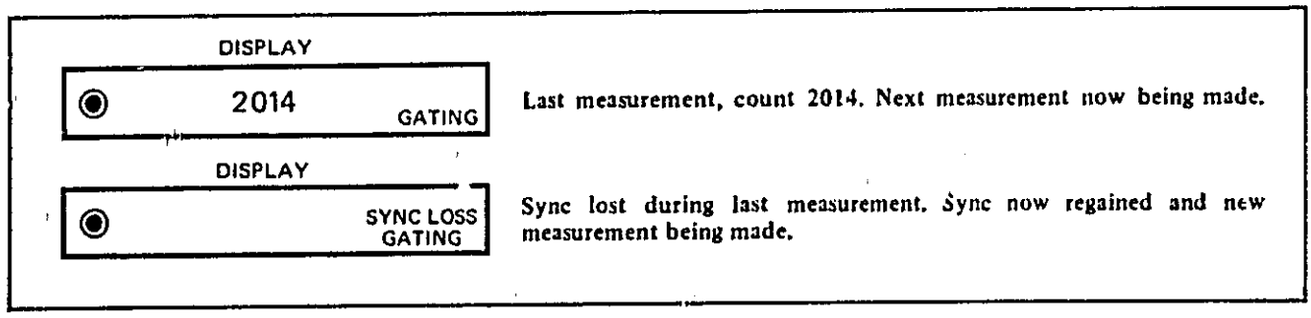


Figure 3-9 Typical Flag Displays

3-22 BCD OUTPUT

An output of the current display, BER or COUNT is provided in 8421 BCD form at a socket on the Error Detector rear panel. This output has been designed for use with Hewlett-Packard Models 5050B and 5055A printers, a suitable connecting cable being supplied with the Error Detector Option 002. This cable is also available separately, *hp* stock number 562-16C. The BER print out occupies columns 1 to 4 and the count columns 3 to 6, column 1 being the right hand column of the print out. Sync loss is indicated by a 0 in column 10 and overflow inhibits the output. The print command is a +ve going TTL pulse initiating paper feed and current display print out. Typical examples of print out are given in Figure 3-10, and Table 3-2 shows the function of the output pins and the printer lines that they control. The measurement result is available at the BCD output socket for the duration of the print command pulse.

DISPLAY		PRINT OUT
BER	3.8×10^{-5}	******38*5
COUNT	2581	****2581**
SYNC LOSS		0*********
OVERFLOW		**********

Figure 3-10 Printer Format

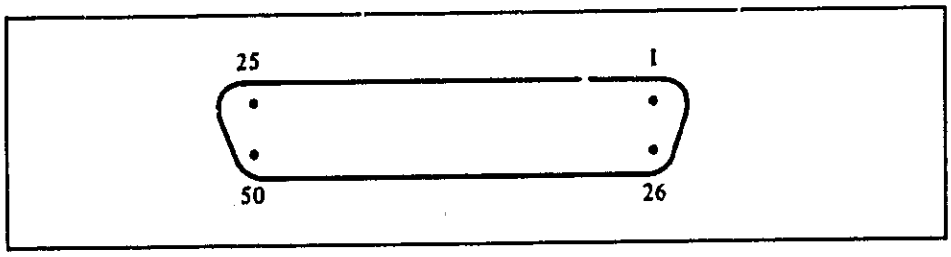


Figure 3-11 Output Socket Pin Numbering

3-23 ERROR OUTPUT

An output is provided once per error in both BER and COUNT modes at the rear panel error output socket. The output pulse is the same width as the clock mark and its amplitude is +1V into 50Ω.

Table 3-2 BCD Output

PRINTER COLUMN	BCD WEIGHTING	FUNCTION	OUTPUT PIN
1	8	BER Exponent	27
1	4	"	26
1	2	"	2
1	1	"	1
2		+5V	3, 4, 28, 29
3	8	Least significant digit	31
3	4	"	30
3	2	"	6
3	1	"	5
4	8	2nd digit	33
4	4	"	32
4	2	"	8
4	1	"	7
5	8	3rd digit	35
5	4	"	34
5	2	"	10
5	1	"	9
6	8	Most significant digit	37
6	4	"	36
6	2	"	12
6	1	"	11
7		+5V	13, 14, 38, 39
8		"	15, 16, 40, 41
9		"	17, 18, 42, 43
10		+5V when in sync	19, 20, 44, 45
10		0V Sync Loss	
		Print command	23
		Ground	50

ERFORMANCE CHECK

FUSE OR POWER SUPPLY FAILURE INDICATION

The following tables show the symptoms of fuse or power supply failure and may be used to determine which fuse is faulty. The instruments should be connected as shown in Figure 4-1.

KEY
- X off or not present
- / on and operational
- // permanently on
- 0 Refreshment indicator lamp operates when changing MODES or when GATE selector is moved from S. SHOT to REP in the COUNT mode.

3760A

	F4 -15V	F2 +15V	F3 -5.2V
TRIGGER indicator	X	X	//
WORD indicators	X	/	/
FAN	/	/	X

3761A

	F5 +15V	F4 -15V	F2 -5.2V	F3 +5V
LEVEL and PHASE indicators	X	X	//	/
GATING flag	X	X	//	X
REFRESHMENT indicator	X	0	/	X
X10^{-} indicator	X	X	X	/
FAN	/	X	/	/

SECTION IV
FAULT ISOLATION

4-1 INTRODUCTION

If a fault occurs in the 3760A/61A Error Rate Measuring System the following procedure is recommended for isolation of the fault to one instrument. The technique described below may be used to determine if a fault exists by generating sequences, deliberately introducing errors, and measuring the error rate produced.

Faults may then be isolated by performance testing the Data Generator to discover if the correct input is available for the Error Detector. The individual instrument service manuals provide troubleshooting information for further fault isolation.

4-2 OPERATIONAL TEST

Connect the Data Generator directly to the Error Detector as shown in Figure 4-1. Set the Data Generator MODE to ERROR ADD, sequence length 3, and the Error Detector MODE to BER, sequence length 3. Confirm that the Error Detector control settings are correct using the setting up procedure on Page 3-9. Increase the Data Generator and Error Detector sequence lengths together and check the displayed error rate, given on Page 2-14. If the error rates are correct return the sequence lengths to 3 and set the Error Detector MODE to COUNT using internal repetitive gating with a suitable interval.

If a fault is observed in only one of the Error Detector modes then the Error Detector is faulty. If a fault condition occurs in both modes, and the clock inputs are correct, the Data Generator Error Add performance test may be used for fault isolation. This test is given on Pages 4-2 and 4-3.

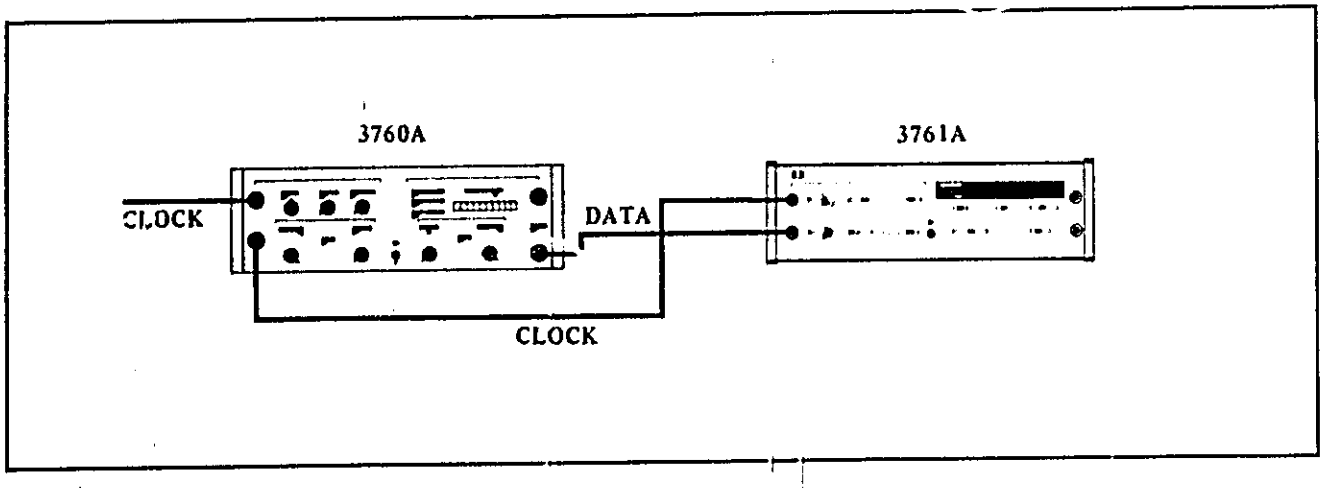
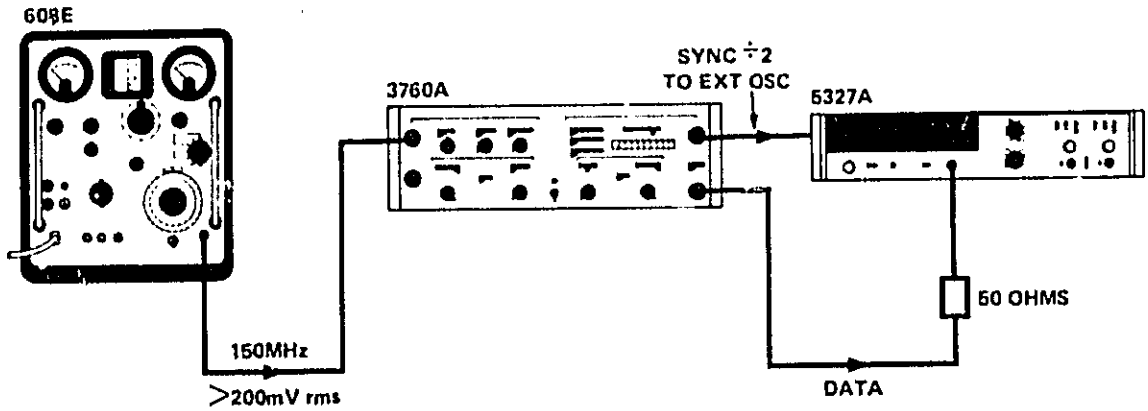


Figure 4-1 Operational Test



DATA MODE	WORD CONTENT	COUNTER READING
PRBS NORMAL	101	80000.00 ±.01
PRBS – ERROR ADD	101	80010.00 ±.01
PRBS – ERROR ADD	011	79990.00 ±.01

Figure 4-2 Error Add Performance Test

4-3 DATA GENERATOR ERROR ADD PERFORMANCE TEST

SPECIFICATION: Introduction of two errors per 4000 sequences by changing two consecutive bits to their logic complements.

1. Set the 3760A DATA MODE to PRBS NORMAL n = 3, DATA FORMAT to RZ, WORD to 101 and the internal Sync Mode switch mounted on assembly A37 to ÷2.

2. Connect a 608E VHF Signal Generator set to 150MHz at >200mV rms to the 3760A CLOCK INPUT.

3. Connect the 3760A DATA OUTPUT terminated in 50Ω to INPUT C on a 5327A Timer/Counter. Connect the 3760A SYNC OUTPUT to the Counter EXT OSCILLATOR (rear panel). Set the counter controls as follows:

   INPUT C .. .. ÷10
   FUNCTION .. .. FREQ C
   MULTIPLIER .. .. 10^7
   OSC (rear panel) .. .. EXT

4. The counter reading should be 80000.00 ±1.

5. Change the DATA MODE switch to PRBS ERROR and check that the Counter reading is now 80010.00±1.

6. With the DATA MODE still at PRBS ERROR change the WORD CONTENT to 011. The Counter reading should now be 79990.00 ±1.

MANUAL CHANGES

HP MANUAL CHANGES

MAKE ALL CORRECTIONS IN YOUR MANUAL ACCORDING TO ERRATA.

Check the following table for your instrument serial prefix and make any indicated changes to the manual:

MANUAL TITLE: 3760A/61A Op. Man.
MANUAL PRINTED: June, 1973
MANUAL PART NO: 03760-95002
CHANGE DATE: 10th April, 1975

SERIAL PREFIX	MAKE CHANGE	SERIAL PREFIX	MAKE CHANGE	SERIAL PREFIX	MAKE CHANGE
1423U-00176	(3760A) 1				
1429U-00176	(3761A) 1				
1439U-00186	(3760A) 2				
1440U-00181	(3761A) 2				

ERRATA

Page 2-13, Para 2
Change : third line to read : with reference to the WORD BIT SELECT switches, see sync pulse notes.
Add : to end of 2nd Para : since all zeros is a forbidden state in the maximal length PRBS.

Page 2-18, Para 2-20
Delete : Complete Paragraph
Add : New Paragraph 2-20 : pages 2, 3 and 4 of this change note.

Page 3-9, Para 5
Change : the second half of Para 5 from the third line onwards to read:- The Phasing is correct when the phase indicator lamp is ON. Optimum phasing is obtained at the mid point of the control excursion for which the phasing lamp is ON. Although in RZ operation at high frequencies the phasing may be correct without this indication. In this case adjust for minimum error rate.

Page 3-9
Delete : the NOTE which reads : Incorrect settings will produce a sync loss display flag, or an incorrect display.

Page 3-13, Para 3-14
Insert : between the third and fourth paragraph the following:- Result acquisition times when using the Data Generator in PRBS ERROR ADD mode are given in Table 2-3, page 14 of this change note.

Page 3-14, Para 3-17
Change : 6th Para. 1st & 2nd lines to read:- When setting up the gating interval at high error rates it may be useful to measure the error rate in BER mode

Page 4-1, Para 4-2
Change : the third line to read:- length 3, word switches to 110 and the Error Detector MODE to BER, sequence length 3.

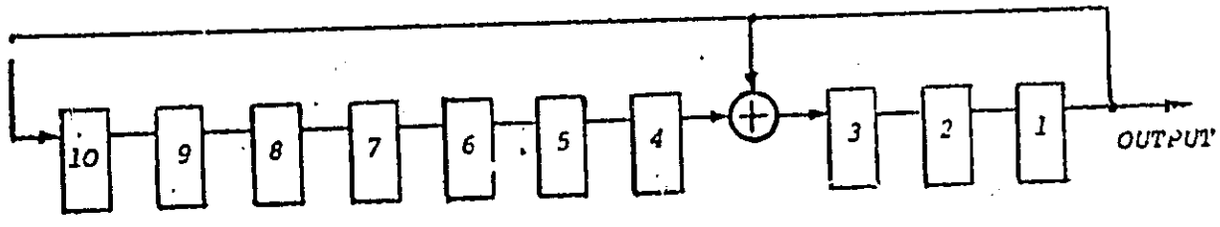
Model 3760A/6`A

2-20 THE SYNC PULSE A IV sync pulse is generated during each PRBS or WORD cycle when the shift register stages are in the states indicated by the WORD BIT SELECT switches. In the WORD NORMAL mode a sync pulse of one clock period duration is generated coincident with the last bit of the repetitive word, and the falling edge provides a convenient oscilloscope trigger for observation of the complete word.

In the PRBS NORMAL mode with n = 3 to 10 the sync pulse can be generated at any desired point in the sequence by selection of the appropriate configuration of the WORD BIT SELECT switches. This enables the whole of a long PRBS to be examined by sampling successive parts of the sequence (e.g. 16 bits) on an oscilloscope triggered with the sync pulse, and advancing the sync pulse for each sample using the WORD BIT SELECT switches

Since the configuration of the PRBS generator used in the 3760A involves the inclusion of modulo-2 adders within the shift register, i.e. between stages, the output word in the PRBS immediately following the sync pulse is not that set up on the front panel switches. These switches rather determine at which state of the register the sync pulse will be produced and the output word following it will depend on the action of the modulo-2 adders in the shift register. However, it is a simple matter to determine the switch settings required to give a specific word immediately following the sync pulse.

As an example, consider the case of a ten stage register (2^{10}-1 PRBS) with the word "abcdefghjk" required immediately following the sync pulse.



10 Stage Register giving 2^{10}-1 PRBS with polynomial $D^{10}+D^3+1 = 0$

In this register the modulo-2 adder is between the third and fourth stages when the stages are numbered from the output end of the register. The reason for numbering the stages in this way is so that the characteristic polynomial clearly indicates the stages whose inputs are connected to the feedback line when the modulo-2 adders are placed within the shift register as shown.

When sync is detected, the data present in stages 1 to 3 will be merely shifted out as output data during the following three clock periods. Hence word switches 1 to 3 must be set to a, b, c respectively (remembering that word switch 1 corresponds to bit 1 of the output word). The following seven bits however, depend on a, b, c as well as the content of stages 4 to 10 at the time of sync detection. Since the fourth output bit after the sync pulse will be the modulo-2 sum of the initial states of stages 4 and 1, word switch 4 should be set to d ⊕ a to ensure that the fourth output bit after the sync pulse is d (for d ⊕ a ⊕ a = d). In the same way it can be shown that switches 5 to 10 should be set to e⊕b, f⊕c, g⊕d, h⊕e, j⊕f, k⊕g respectively. This can be seen more clearly by reference to the shift table below:

REGISTER STAGE	*10*	*9*	*8*	*7*	*6*	*5*	*4*	*3*	*2*	*1*	*OUTPUT*	*TIME*
SWITCH SETTING	*k⊕g*	*j⊕f*	*h⊕e*	*g⊕d*	*f⊕c*	*e⊕b*	*d⊕a*	*c*	*b*	*a*	-	t_0
	-	*k⊕g*	*j⊕f*	*h⊕e*	*g⊕d*	*f⊕c*	*e⊕b*	*d*	*c*	*b*	*a*	t_1
	-	-	*k⊕g*	*j⊕f*	*h⊕e*	*g⊕d*	*f⊕c*	*e*	*d*	*c*	*b*	t_2
	-	-	-	*k⊕g*	*j⊕f*	*h⊕e*	*g⊕d*	*f*	*e*	*d*	*c*	t_3
	-	-	-	-	*k⊕g*	*j⊕f*	*h⊕e*	*g*	*f*	*e*	*d*	t_4
	-	-	-	-	-	*k⊕g*	*j⊕f*	*h*	*g*	*f*	*e*	t_5
	-	-	-	-	-	-	*k⊕g*	*j*	*h*	*g*	*f*	t_6
	-	-	-	-	-	-	-	*k*	*j*	*h*	*g*	t_7
	-	-	-	-	-	-	-	-	*k*	*j*	*h*	t_8
	-	-	-	-	-	-	-	-	-	*k*	*j*	t_9
	-	-	-	-	-	-	-	-	-	-	*k*	t_{10}

Table 2-4.

NB: On each clock pulse the register stages accept the data previously held in the next higher stage with two exceptions:-

- stage 10 takes the data previously held in stage 1
- stage 3 takes the modulo-2 sum of the data previously held in stages 4 and 1.

t_0 is the time when the sync pulse occurs.

In a similar manner the switch settings can be determined for the other register lengths from n=3 to 10. For the eight stage register which contains three modulo-2 adders, the calculation is slightly more involved and results in longer expressions.

In the case of the fifteen stage register, the states of only ten of the stages can be detected for sync pulse generation - the remaining five stages (i.e. stages 11 to 15) have to be all at zero before the sync pulse is generated. This does not necessarily result in bits 11 to 15 after the sync pulse being all zero. Instead, they are all the same as the tenth bit. Hence it is only possible to set the word switches such that the output word immediately following the sync pulse is "abcdefghjkkkkkk".

A complete list of word switch settings is given in Table 2-5

REQUIRED WORD	*a*	*b*	*c*	*d*	*e*	*f*	*g*	*h*	*j*	*k*	*kkkkk*
SWITCHES	*1*	*2*	*3*	*4*	*5*	*6*	*7*	*8*	*9*	*10*	-
n = 3	a	b	c⊕a	-	-	-	-	-	-	-	-
4	a	b	c	d⊕a	-	-	-	-	-	-	-
5	a	b	c⊕a	d⊕b	e⊕c	-	-	-	-	-	-
6	a	b⊕a	c⊕b	d⊕c	e⊕d	f⊕e	-	-	-	-	-
7	a	b⊕a	c⊕b	d⊕c	e⊕d	f⊕e	g⊕f	-	-	-	-
8	a	b	c⊕a	d⊕b ⊕a	e⊕c ⊕b⊕a	f⊕d ⊕c⊕b	g⊕e ⊕d⊕c	h⊕f ⊕e⊕d	-	-	-
9	a	b	c	d	e⊕a	f⊕b	g⊕c	h⊕d	j⊕e	-	-
10	a	b	c	d⊕a	e⊕b	f⊕c	g⊕d	h⊕e	j⊕f	k⊕g	-
15	a	b⊕a	c⊕b	d⊕c	e⊕d	f⊕e	g⊕f	h⊕g	j⊕h	k⊕j	-

Table 2-5 Word Switch Settings for Sync Pulse

When the PRBS or WORD, ZERO ADD modes are selected the sync pulse is stretched to the length of the zero block plus one clock period. As the rising edge of the sync pulse initiates the zero block, it occurs one clock period before the first zero. The rising and falling edges may therefore be used as triggers for the examination of the zero block period or the part of the sequence immediately after as shown in Figures 2-16 and 2-17. The effect of delays both within the instrument and in the external cabling may affect the timing of the sync pulse relative to the data.

In PRBS ERROR ADD mode, the sync pulse is used to initiate two errors every 4000 sequences and thus determines the position of these errors.

In PRBS modes no sync pulses are produced with a 2^n-1 PRBS if the first n WORD BIT SELECT switches are at 0. In the WORD mode, words which are multiples of shorter words, e.g. 110110110 produce a sync pulse for each of the shorter words. No data or sync is produced for words containing all 1's or all 0's and no sync pulses are produced with the maximum change word 1010.

CHANGE 1

Page 2-6, Para 15
Delete : PRBS with one ERROR in 2000 sequences
Add : PRBS with two ERRORS in 4000 sequences

Page 2-6, Para 18
Add : and Added Errors in PRBS

Page 2-14, Para 2-15
Delete : Selection of PRBS ERROR ADD with the MODE switch deliberately introduces errors by changing two consecutive bits in every 4000 sequence to their logic complements.
Add : Selection of PRBS ERROR ADD with the MODE switch deliberately introduces errors at a rate of two errors per 4000 sequences by changing one bit in two consecutive sequences to its logic complement.

Page 3-1, Para 7, third line
Delete : An output of one pulse per error is also available at the rear panel for further analysis.
Add : An output of one transition per error is also available at the rear panel for further analysis.

Page 3-7, Para 23
Delete : Paragraph 23
Add : FLAG SIGNALS are displayed as follows:
GATING when the error detector is in sync and the counter is accumulating errors.
SYNC LOSS during a search for synchronism.
OVERFLOW when the error count or display overflow.
The flag is retained until the next measurement is displayed.

Page 3-8, Para 1
Delete : ERROR OUTPUT provides one pulse per error in both BER and COUNT modes. The pulse width is the same as the clock input pulse and.
Add : ERROR OUTPUT provides one transition per error in both BER and COUNT modes, its amplitude is +1V into 50Ω.

Page 3-13
Delete : Paragraphs 3-14 to 3-16
Add : New Paragraphs 3-14 to 3-16 : Page 6 of this change note

Page 3-14, Para 3-19
Delete : One pulse per error
Add : One transition per error

Page 3-15
Delete : Paragraphs 3-20 and 3-21
Add : New Paragraphs 3-20 and 3-21 : Page 7 of this change note.

Page 3-16, Para 3-23
Delete : Complete Paragraph
Add : An output transition is provided once per error in both BER and COUNT modes at the rear panel error output socket
Its amplitude is +1V into 50Ω

Page's 4-2 & 4-3
Delete : Data Generator Error Add Performance Test
Add : New Performance Test, Pages 8 & 9 of this change note

3-14 THE BER MODE

With the MODE switch set to BER follow the setting up procedure on Page 3-9. The method of measurement in the BER mode is to accumulate 100 errors, continue counting until the next clock decade is reached, and then to display the two most significant digits of the error count with an exponent derived from the clock counter as shown in Figure 3-7

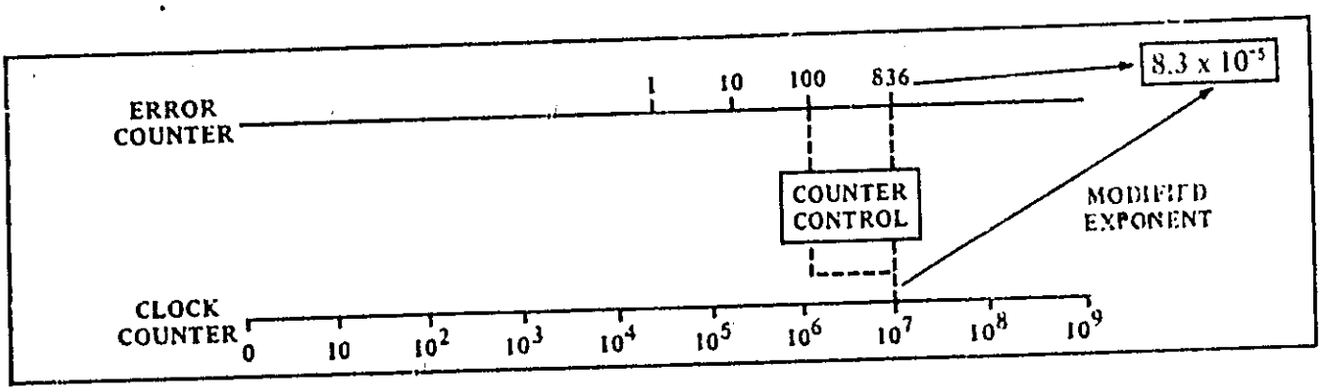


Figure 3-7 BER Measurement

If sync loss is continuously flagged check the following:

Error Detector phase and data polarity are correctly set.
Data Generator and Error Detector sequence lengths are the same.

The Gating flag indicates that synchronism has been achieved and that the counter is in operation. This is particularly useful at low error rates when a significant time might elapse before the first 100 errors are accumulated. Result Acquisition times when using the Data Generator in PRBS ERROR ADD mode are given in Table 2-3, Page 14 of this change note.

At very low error rates operation of the measuring system may be confirmed by inserting deliberate errors at the rate of two errors per 4000 sequences. The error rates are given in Table 2-3, Page 2-14.

In the BER mode the display rate is controlled with the DISPLAY HOLD control and an indication of the refreshment rate is given by the strobe lamp on the display. Operation of this lamp is described in the flag signal section on Page 3-15.

3-15 SYNC MODES AVAILABLE WITH BER OPERATION

Manual, Auto, External.

Synchronisation mode details are given on Page 3-12.

3-16 OUTPUTS AVAILABLE IN BER MODE

LED display of BER, BCD output of current display. One transition per error

3-20 REFRESHMENT RATE

At high error rates the measurements may be completed faster than they can be read from the display. In order to reduce the rate of change of the display, refreshment rate, a hold control is provided which holds the measurement and delays the display change for periods of 200ms to 3s approximately. A strobed lamp is provided, on the left hand side of the display, to indicate the times at which the display may be refreshed. The display changes at the first refreshment time after the completion of a measurement as shown in Figure 3-8. When the display can be refreshed faster than measurements can be made, the strobed lamp will indicate possible refreshment times.

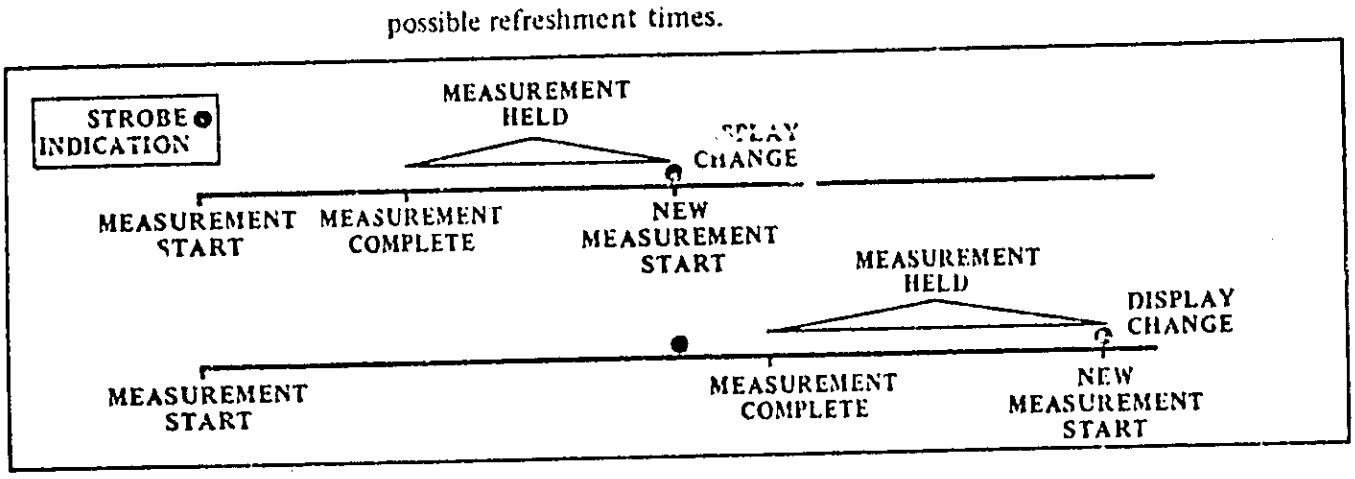


Figure 3-8 Display Refreshment

3-21 FLAG SIGNALS

The three flag signals, GATING, SYNC LOSS, and OVERFLOW, provided on the display, apply to both BER and COUNT modes of operation. The conditions indicated by these flag signals are listed below:

GATING indicates that the error detector is in sync and an error count is taking place.

SYNC LOSS indicates that a search for synchronism is taking place.

OVERFLOW indicates display overflow in COUNT and error counter overflow in BER. The flag will continue to be indicated until a fresh computation has been made. During internal single shot, manual or external counts the least significant digits of the error count will always be displayed even during overflow conditions.

The display of the current BER or COUNT is blanked during SYNC LOSS conditions. Two typical displays are shown in Figure 3-9.

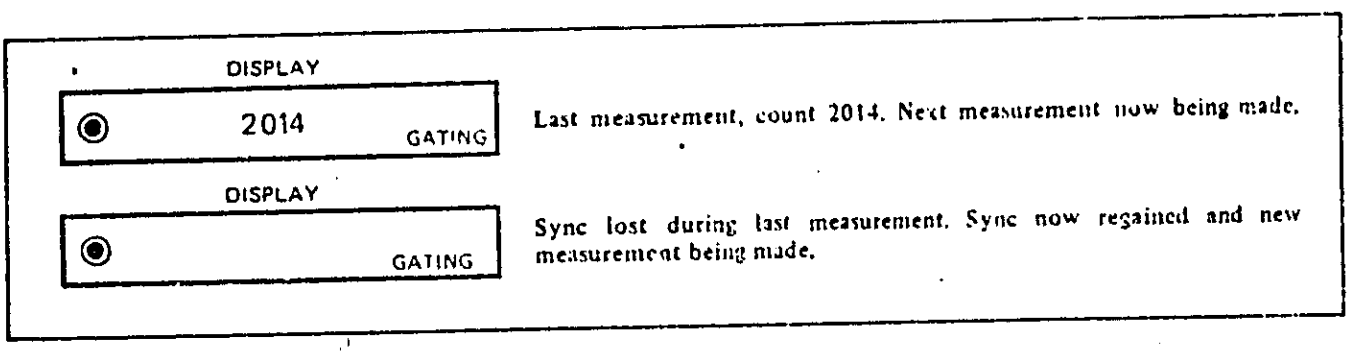


Figure 3-9 Typical Flag Displays

PRBS – ERROR ADD
PERFORMANCE TEST

SPECIFICATION:

Introduction of errors at a rate of two errors per 4000 sequences by changing one bit in two consecutive sequences to its logic complement.

PROCEDURE:

1. Set the 3760A Data Mode to PRBS NORMAL, n = 3, the Data Format to NRZ and the internal Sync Mode switch mounted on assembly A37 to ÷2.

2. Connect a 608E VHF Signal Generator set to 150MHz at >200mV rms to the 3760A CLOCK INPUT.

3. Connect the 3760A DATA OUTPUT terminated in 50Ω to INPUT C on a 5327A Timer/Counter. Connect the 3760A SYNC OUTPUT to the counter EXT OSCILLATOR input (rear panel). Set the counter controls as follows:

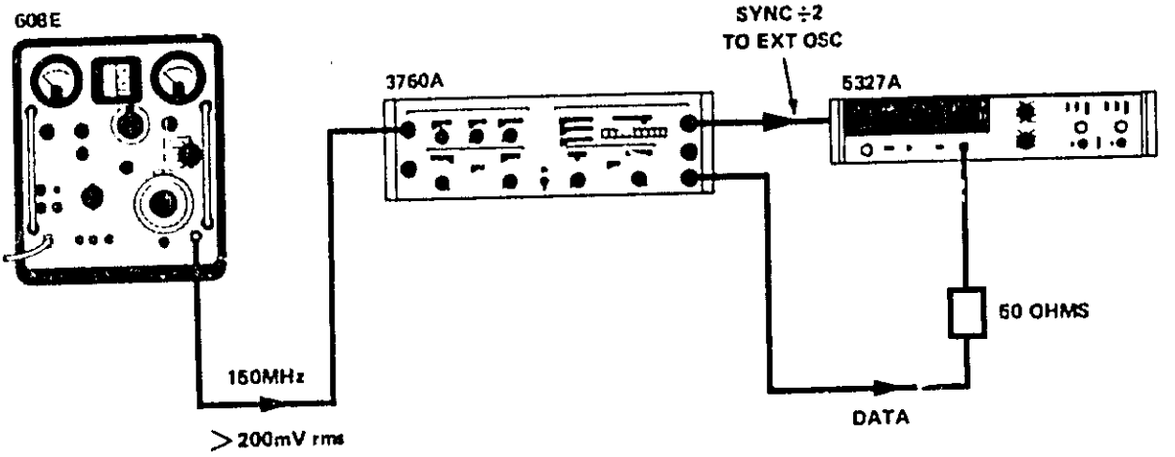
   INPUT C .. .. ÷10
   FUNCTION .. .. FREQ C
   MULTIPLIER .. .. 10^7
   OSC (rear panel) .. .. EXT

4. Set the WORD switches to 110.

5. The counter reading should be 40000.00 ±.01.

6. Change the Data Mode switch to PRBS – ERROR ADD and check that the counter reading is now 40010.00 ±.01.

7. Change the WORD switches to 100. The counter reading should now be 39990.0 ±.01.



DATA MODE	WORD CONTENT	COUNTER READING
PRBS NORMAL	110	40000.00 ±.01
PRBS – ERROR ADD	110	40010.00 ±.01
PRBS – ERROR ADD	100	39990.00 ±.01

Figure 4-2 Error Add Performance Test

CHANGE 2

Page 2-0
Delete : 3760A Data Generator Specification
Add : New Data Generator Specification, Page 12 of this change note

Page 2-1
Delete : 1st Paragraph
Add . The Hewlett-Packard Model 3760A Data Generator produces both digital words and Psuedo Random Binary Sequences, PRBS.
Digital words at rates from 1.5Mb/s up to 150Mb/s.
PRBS at rates from .001Mb/s to 150Mb/s.

Page 2-1
Delete : 2nd Paragraph
Add : The clock frequency in the range 1.5 to 150MHz can be derived from an internal clock generator (Optional)or the unit can be Manually or Automatically triggered from an external clock. In the external clock mode the clock frequency range is from 1KHz to 150MHz. A clock output, variable in amplitude from 0.1 to 3.2V pk-pk with a rise rime of better than 1.4nS, is also provided.

Page 2-4, Para 5
Delete : Ranges 1.5 to 15, 15 to 150MHz
Add : External source ranges 1KHz to 150MHz
Internal generator ranges 1.5 to 15, 15 to 150MHz

Page 2-9, Para 2-10
Delete : The Data Generator has a 50Ω external clock input which accepts any wave shape in the 1.5 to 150MHz range.
Add : The Data Generator has a 50Ω external clock input which accepts any wave shape in the 1KHz to 150MHz range

Page 2-14
Delete : Para 2-14 and 2-15
Add : New Paragraph 2-14 and 2-15, Page 14 of this change note.

Page 3-0
Delete : 3761A Error Detector Specification
Add : New Error Detector Specification, Page 13 of this change note.

Page 3-1, Para 4 second line
Delete : In the frequency range 1.5 to 150MHz
Add : In the frequency range 1K to 150MHz

Page 3-4, Para 5
Add : The 0-12nS range also applies for the 1Kb/s to 1.5Mb/s position or when the 3761A is being operated in Burst Mode.

Page 3-5, Para 6
Delete : The range is 0 to 180° for 1.5 to 50MHz and 0 to 12nS for 50 to 150MHz
Add : The range is 0 to 180° for 1.5 to 50MHz and 0 to 12nS for 1KHz to 1.5MHz and 50 to 150MHz.

Page 3-11, Para 3-12
Change : The last two lines of the 1st paragraph to read:
For bit rates of 1.5 to 50Mb/s the range is 0 to 180° using a phase shifter and for bit rates of 0.001 to 1.5Mb/s and 50 to 150Mb/s it is 0 to 12nS using a delay line.

CHANGE 2 CONT. Page 3-16

Add : New Paragraph 3-24 BURST MODE OPERATION

For specialised situations where Clock and Data signals occur in Bursts, the 3760A and 3761A Clock Trigger Mode switches should be set to the MAN triggering position. The 3761A Data Input Amplifier triggering threshold should be internally switched to GND. This switch is located on the 3761A A21 assembly (03761-71021).

In this mode the Data signal presented to the 3761A must be arranged to have positive and negative excursions with respect to ground. An example of how to use the 3760A to produce Burst Data and Clock is shown in Figure 1.

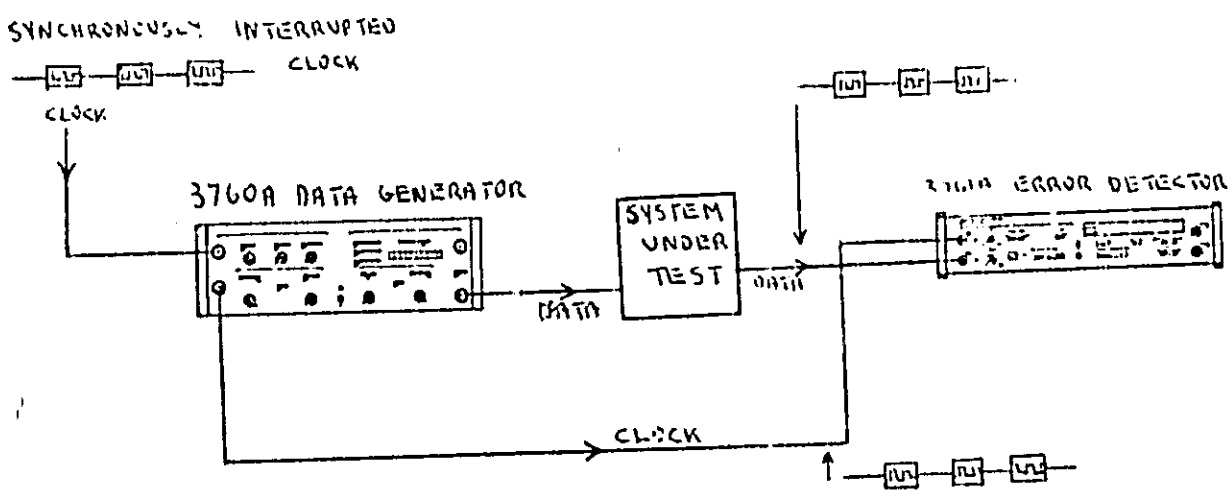


Figure 1.

The 3760A/3761A may be used as shown (Fig. 1) to measure error rate or count. After initial synchronisation the 3760A/3761A will remain synchronised and errors will only be accumulated during the presence of clock.

The 3761A should have its range switch in the 50 - 150 Mbit/s position as this ensures that the 3761A phase adjustment is obtained with a delay line and not with a ramp phase shifter which cannot tolerate loss of clock.

Model 3760A/61A

3760A Data Generator Specifications

MODES OF OPERATION

PRBS NORMAL	Generates a repetitive $2^N - 1$ bit, maximal length, Pseudo Random Binary Sequence where N = 3 to 10 and 15
PRBS ADD ZEROS	Addition of a block of 1 to 99 zeros into PRBS NORMAL, occurring after the sync pulse
PRBS ADD ERROR	Introduction of errors at a rate of two errors per 4000 sequences by changing one bit in two consecutive sequences to its logic complement.
1010	Generates a preset repetitive word, content 1010.
WORD NORMAL	Generates a continuous 3 to 10-bit word with selectable content.
WORD ADD ZEROS	Addition of a block of 1 to 99 zeros into WORD NORMAL, occurring between words.

CLOCK INPUT

Rate	1kHz to 150MHz.
Impedance	50Ω ±5% dc coupled (75Ω optional)
Trigger:	
Manual	Level range: -3 to +3V. Slope +ve or -ve.
Auto	Input mark space ratio range 10:1 to 1:10.
Sensitivity	Better than 500mV pk-pk.
Amplitude	5V pk-pk maximum. Limits ±5V
Pulse Width	3ns minimum at 50% pulse amplitude.

CLOCK OUTPUT

Outputs	CLOCK or $\overline{\text{CLOCK}}$, from external or optional internal clock.
Impedance	Source impedance 50Ω ±5% (75Ω optional).
Amplitude	Continuously variable in 5 ranges from 0.1 to 3.2V symmetrical about offset level.
Rise/Fall time	<1.4ns into 50Ω <1.6ns into 75Ω (75Ω impedance option)
DC Offset	Zero: <2% of pulse amplitude Variable: Continuous 0 ±3V

OPTIONS

Option 001	75Ω CLOCK and DATA input/output impedances
Option 002	Internal, variable frequency clock. Rate: 1.5 to 150MHz Jitter: <0.5% of period +0.05ns pk-pk
Option 003	Options 001 and 002 combined.

DATA OUTPUT

Outputs	DATA or $\overline{\text{DATA}}$.
Format	NRZ. RZ (up to 130Mb/s).
Impedance	Source impedance 50Ω ±5% (75Ω Optional).
Amplitude	Continuously variable in 5 ranges from 0.1 to 3.2V into 50Ω symmetrical about offset level
Rise/Fall time	<1.4ns into 50Ω <1.6ns into 75Ω (75Ω impedance option)
Overshoot	<10% of pulse amplitude
DC Offset	Zero: <2% of pulse amplitude Variable: Continuous 0 to +3V
DELAY	Data (and sync) delayed with respect to clock continuously in 10 ranges from 0 to 100ns.

SYNC OUTPUT

Rate	Once per PRBS or WORD cycle
Duration:	
PRBS and WORD	
Normal	1 CLOCK period
Add Zeros	Length of zero block plus one clock period.
Position:	
PRBS	
Normal	Front panel selectable
WORD	
Normal	Precedes word
Add Zeros	Precedes zero block by one clock period
Impedance	Source impedance 50Ω ±5%
Amplitude	+1V nominal

GENERAL

Power: 90 to 125 or 200 to 250V 40 to 400Hz, consumption 90W	Weight: 30lbs (13.6kg)	Dimensions: 16.8in wide, 5.6in high, 19.7in deep (427mm x 140mm x 498mm)

3761A Error Detector Specifications

MEASUREMENTS

Bit Error Rate, BER

Range	9.9×10^{-1} to 0.1×10^{-9}, automatically scaled.
Gating	Automatic, at least 100 errors before computation

Total Error Count, COUNT

Range	0 to 9999.
Gating:	
Internal	Repetitive or single shot
Interval	10^n clock periods where integer n = 5 to 11.
External	Logic level TTL
Manual	Front panel switch.
Sequences	Maximal length PRBS
Lengths	$2^N - 1$ where N = 3 to 10 and 15

CLOCK INPUT

Rate	1kHz to 150MHz.
Impedance	50Ω ±5% dc coupled (75Ω optional).
Trigger:	
Slope	+ve or -ve.
Manual	Level range -3 to +3V
Auto	Input mark:space ratio range 10:1 to 1:10.
Sensitivity	Better than 500mV pk-pk
Amplitude	5V pk-pk max. Limits ±5V
Pulse Width	3ns minimum at 50% pulse amplitude.

DATA INPUT

Input	DATA or $\overline{\text{DATA}}$, selectable
Rate	1kHz to 150Mb/s.
Impedance	50Ω ±5% dc coupled (75Ω optional).
Trigger Level	Automatic. Input mark:space ratio range 10:1 to 1:10.
Sensitivity	Better than 500mV pk-pk
DC Offset	±3V maximum.
Amplitude	5V pk-pk max. Limits ±5V.
Pulse Width	5ns minimum at 50% pulse amplitude.

PHASING

Control	Clock phase variable relative to data.
Indication	Lamp off when clock and data edges coincide

Range			
1.5 to 50Mb/s	0 to 180°	50 to 150Mb/s	0 to 12ns.

SYNCHRONISATION

Modes	Auto, Manual, External External and Manual initiate single shot Auto sync
Auto	Automatically searches for synchronism if more than 20,000 errors in 100,000 bits.
External	Resynchronisation commanded by TTL input.
Manual	Resynchronisation commanded from front panel

DISPLAY

BER	Two digits plus exponent a.b x 10^{-x}.
COUNT	Four digits.
Flags	Sync loss, overflow and gating.

OUTPUTS

Printer	8421 BCD.
BER and COUNT	Current display on command
Flags:	
Sync loss	0 printed in column 1
Overflow	Output inhibited
Print command	False at display change
Error output	
Rate	One transition per error.
Amplitude	+1V into 50Ω nominal

ACCURACY

BER	Computation based on at least 10 errors.
COUNT	Internal gating, ±1 error.

OPTIONS

Option 001	75Ω CLOCK and DATA input impedances.
Option 002	Printer interface cable

GENERAL

Power	90 to 125 or 200 to 250V 40 to 400Hz, consumption 70W	Weight	23lbs 10.4kg	Dimensions	16¾in wide. 3¾in high, 15¾in deep (425mm x 95mm x 400mm)

2-14 ZERO ADDITION

A block of 1 to 99 zeros can be added into a WORD or PRBS by selecting the WORD ZERO ADD or PRBS ZERO ADD positions of the MODE switch. The zero block is initiated by, and occurs immediately after, the sync pulse. The position of the zero block in the sequence is therefore controlled by the WORD BIT SELECT switches which determine the position of the sync pulse as shown in the sync pulse notes on Page 2-18. In the WORD ZERO ADD mode the zero block occurs between words and in the PRBS ZERO ADD mode the zero block occurs at the point in sequence determined by the WORD BIT SELECT switches.

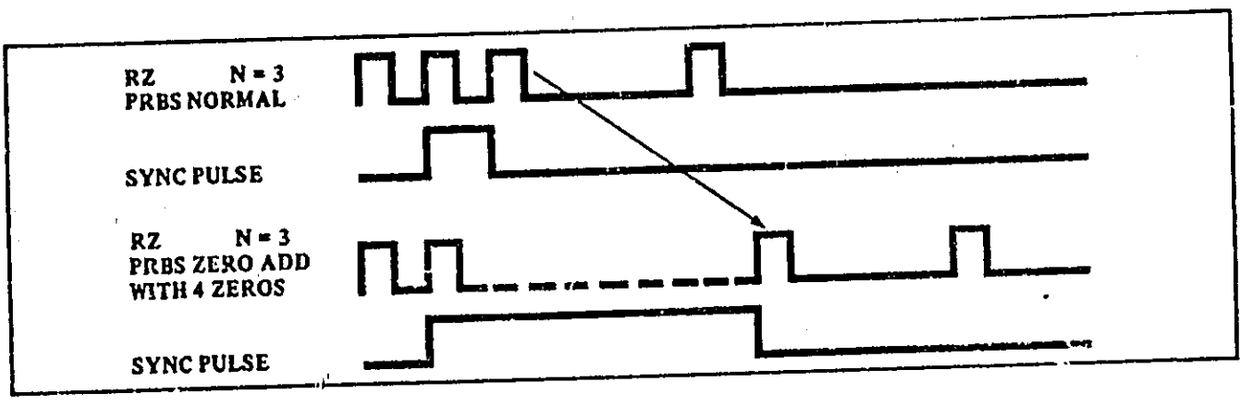


Figure 2-11 Zero addition

2-15 ERROR ADDITION

Selection of PRBS ERROR ADD with the MODE switch deliberately introduces errors at a rate of two errors per 4000 sequences by changing one bit in two consecutive sequences to its logic complement. The actual bits changed are determined by the position of the sync pulse which may be selected with the WORD BIT SELECT switches as shown in the sync pulse notes on Page 2-18. Note that the errors will only be introduced if sync pulses are being generated i.e. at least one of the first n word switches must be set to logic '1'. The Error Rate, which will depend on the register length selected, may be used to confirm the correct operation of the 3761A Error Detector. The error rates produced in the error add mode are listed with the sequence lengths in Table 2-3, for all positions of the REGISTER LENGTH switch.

TABLE 2-3 ERROR RATES IN THE PRBS ERROR ADD MODE

REGISTER LENGTH (n)	SEQUENCE LENGTH (bits)	ERROR RATE (BER)	RESULT ACQUISITION TIMES			
			1 Kb/s	1.5 Mb/s	50 Mb/s	150 Mb/s
3	7	7.1×10^{-5}	2.78 hrs	6.67 secs	0.20 secs	0.07 secs
4	15	3.3×10^{-5}	2.78 hrs	6.67 secs	0.20 secs	0.07 secs
5	31	1.6×10^{-5}	2.78 hrs	6.67 secs	0.20 secs	0.07 secs
6	63	7.9×10^{-6}	1.16 days	1.11 mins	2.00 secs	0.67 secs
7	127	3.9×10^{-6}	1.16 days	1.11 mins	2.00 secs	0.67 secs
8	255	1.9×10^{-6}	1.16 days	1.11 mins	2.00 secs	0.67 secs
9	511	9.7×10^{-7}	1.65 wks	11.11 mins	20.00 secs	6.67 secs
10	1023	4.8×10^{-7}	1.65 wks	11.11 mins	20.00 secs	6.67 secs
15	32767	1.5×10^{-8}	16.53 wks	1.85 hrs	3.33 mins	1.11 mins