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Plextek RFI

KEYSIGHT TECHNOLOGIES

Plextek RFI

How to Design an X-band MMIC PA

Stuart Glynn and Liam Devlin

Introduction

- Target specification and application
- Design approach
- Device size and bias selection
- Load-pull simulation to select terminating impedances
- Circuit schematic
- Layout
- EM simulation and layout optimisation
- Final simulated performance
- Fabrication
- Measured performance
- Summary/Conclusions

Target Specification

Intended application: phased array radar

Parameter	Units	Target
Frequency	GHz	9 to 11
SS Gain	dB	> 12
P_{sat}	W	> 6
	dBm	> 37.7
PAE at P_{sat}	%	> 40
IRL	dB	> 9
ORL	dB	> 8
Drain Voltage	V	25

Design Approach

1. Device Level Simulations, (including load pull) to Identify:
   - Unit Device Size
   - Bias Point
   - Fundamental and Harmonic Impedance Targets (Load / Source)
   - Number of Stages
   - Number of Devices in Output Stage
2. Schematic Design
   - Matching Network Topology
   - Bias Network Topology
3. Layout
   - Preliminary Layout
   - EM Simulation and Layout Optimization
   - DRC

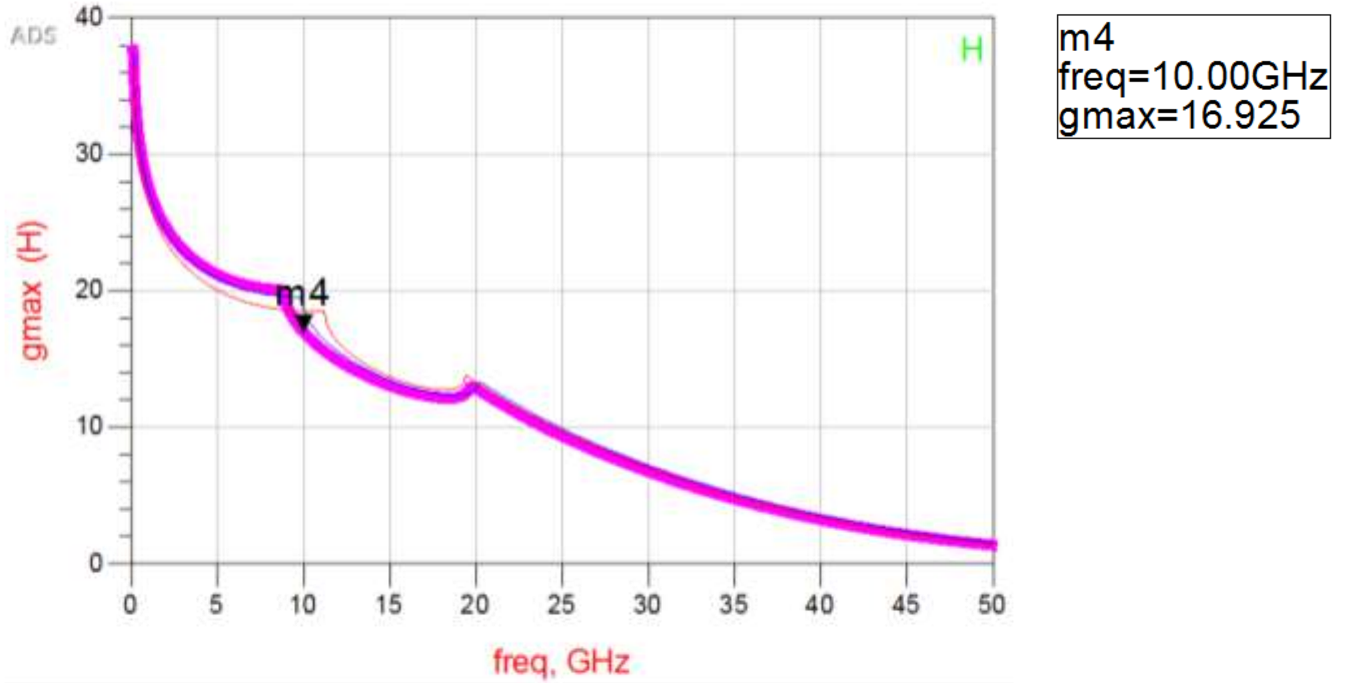
Device Selection

Gmax of three, 8 finger devices, biased at 100mA/mm from 25V. Each has a different finger width.

Red is for an 8x75µm device,

Blue is for an 8x125µm device,

Magenta is for an 8x150µm device



- Largest device provides most RF power but must have adequate available gain
- Performance trade-off compared (gain, power and impedances) for different transistors
- The 8x150µm device was selected - also desirable as the break points in the Gmax plot indicate that it is unconditionally stable from 9GHz to 20GHz

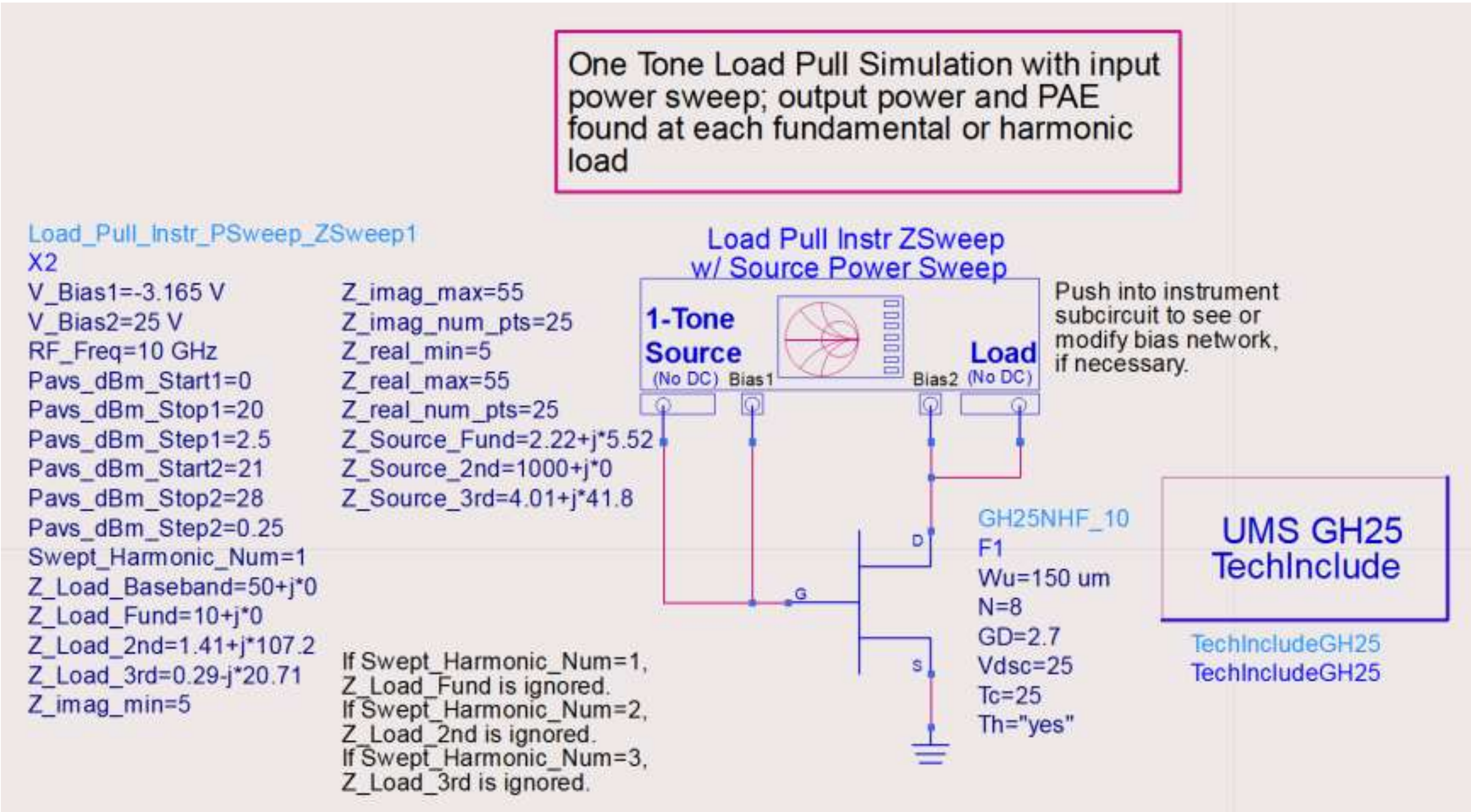
Device Bias Point Selection

Vdd (V)	Ids/mm (mA)	P_{4dB} (dBm)	PAE at P_{4dB} (%)	Gain at P_{4dB} (dB)
25	100	36.44	52.47	11.44
25	75	36.56	53.01	11.06
25	50	36.67	53.45	10.67

Load and Source Pull analysis was carried out on the selected 8x150µm device at various current densities for Vds=25V. Key parameters such as power, gain and power added efficiency (PAE) at 4dB compression were assessed.

Quiescent bias points of 75mA/mm and 37.5mA/mm were considered during the design, corresponding to a transistor bias of 90mA and 45mA at 25V.

Device Level Simulations



Load Pull on Selected Device at 10GHz at 4dB Compression

Power and PAE contours are shown at 10GHz at 4dB compression.

The corresponding load harmonic terminations are:-

1.41Ω + j*107.2Ω at 2nd Harmonic

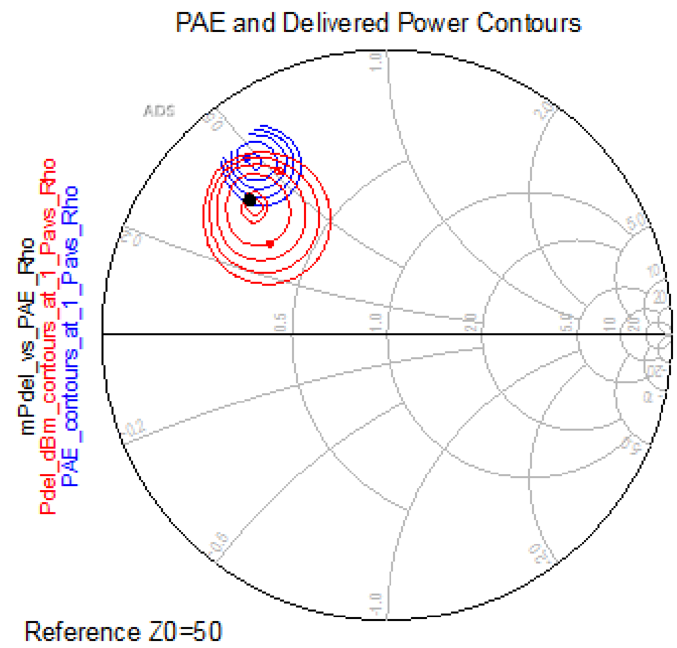
0.29Ω – j*20.71Ω at 3rd Harmonic

The corresponding source impedances are:-

2.22Ω + j*5.52Ω at the fundamental

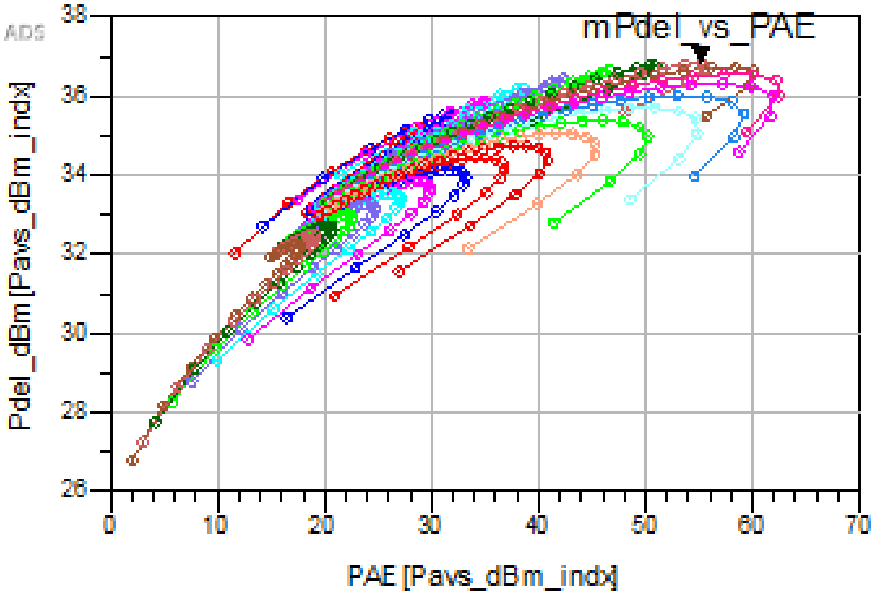
1000Ω + j0Ω at 2nd Harmonic

4.01Ω + j*41.80Ω at 3rd Harmonic



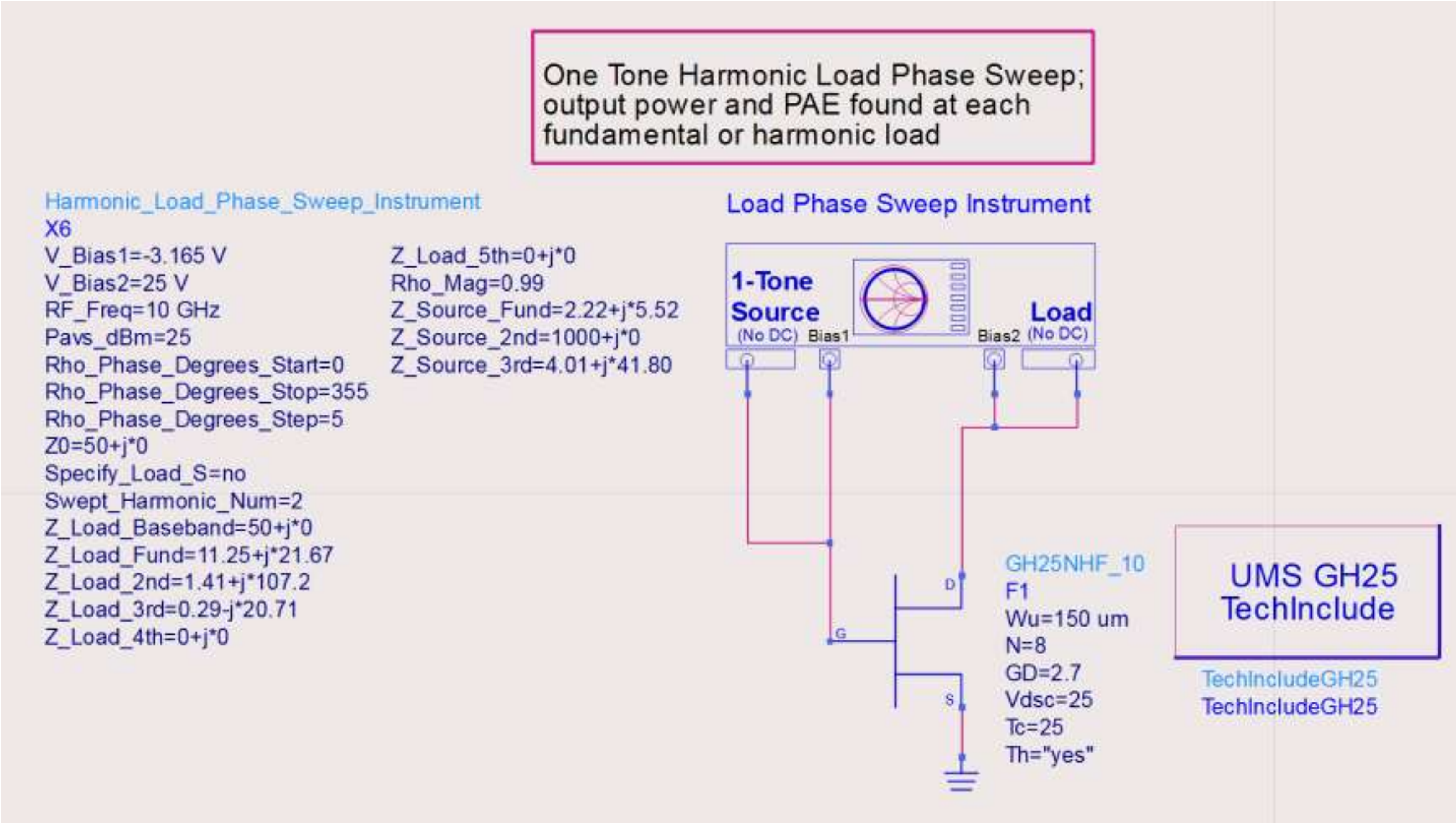
Maximum PAE and contour levels, %:	Maximum Power Delivered and contour levels, dBm:
62.382	36.785
62.000	36.750
60.000	36.500
58.000	36.250
56.000	36.000
54.000	35.750

Load Pull on Selected Device at 10GHz at 4dB Compression



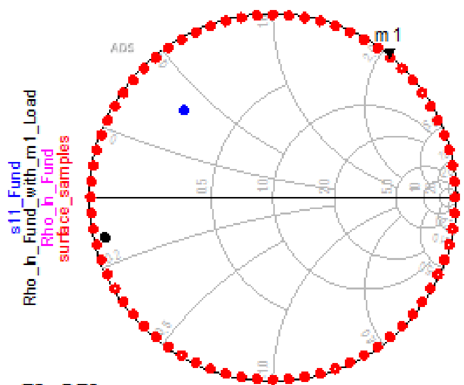
- Above plot was used to select the fundamental load impedance that would be the best compromise between output power and PAE at 4dB compression
- The selected fundamental load Z target was 11.25Ω + j*21.67Ω

Device Level Simulations



Device Level Simulations – Load 2nd Harmonic

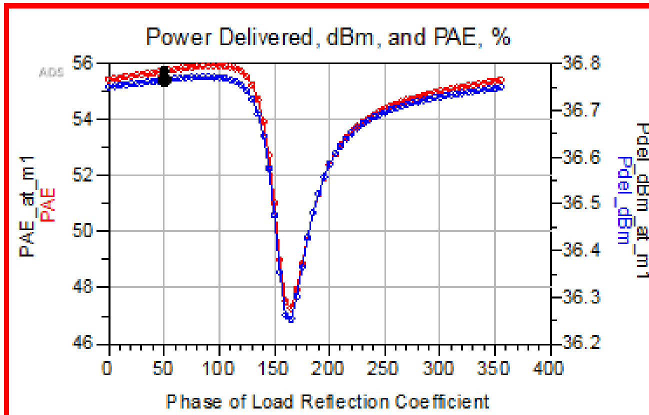
The data inside the red polygon corresponds to the load selected by the m1 marker and will only change if you move the marker to a different load.



Reference Z0=@Z0

● Blue dot is load reflection coefficient at fundamental.

● Black dot is input reflection coefficient with harmonic load selected by marker m1.



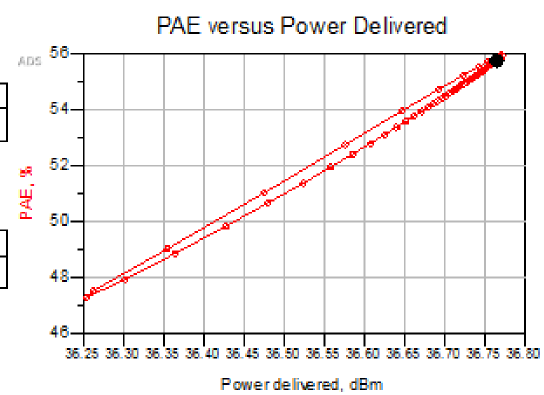
At load selected by marker m1:

BiasCurrent_at_m1	Zload_at_m1	Rho_at_m1
0.316	1.407 + j107.210	0.990 / 50.000

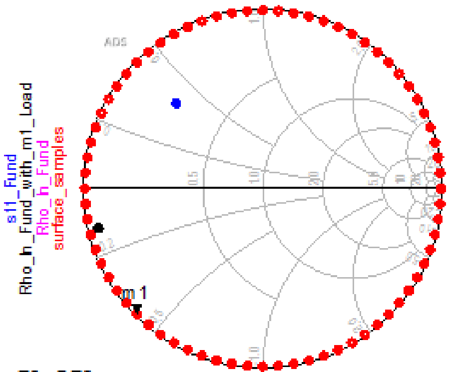
PAE_at_m1
55.741

Z_In_at_m1	Gain_at_m1
1.631 -j5.901	11.265

Pdel_dBm_at_m1
36.765



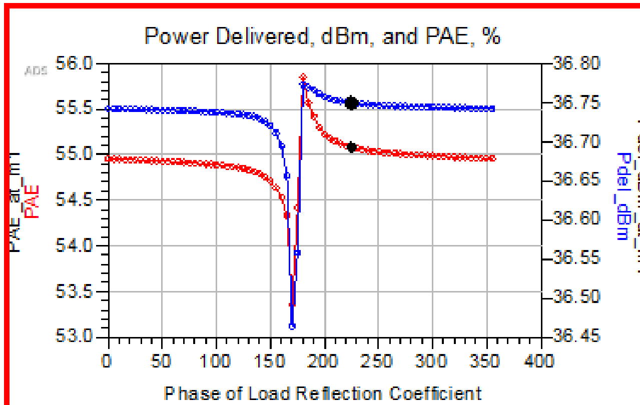
Device Level Simulations – Load 3rd Harmonic



Blue dot is load reflection coefficient at fundamental.

Black dot is input reflection coefficient with harmonic load selected by marker m1.

The data inside the red polygon corresponds to the load selected by the m1 marker and will only change if you move the marker to a different load.



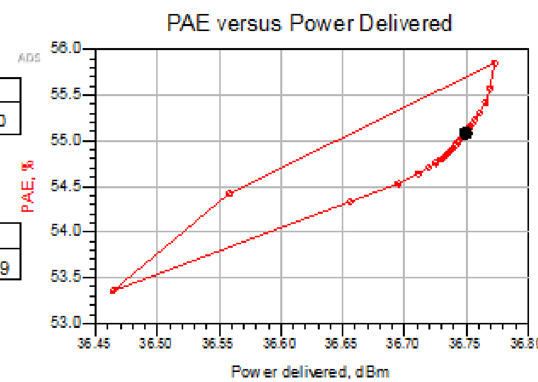
At load selected by marker m1:

BiasCurrent_at_m1	Zload_at_m1	Rho_at_m1
0.319	0.294 - j20.710	0.990 / -135.000

PAE_at_m1
55.080

Z_In_at_m1	Gain_at_m1
1.534 - j5.945	11.249

Pdel_dBm_at_m1
36.749



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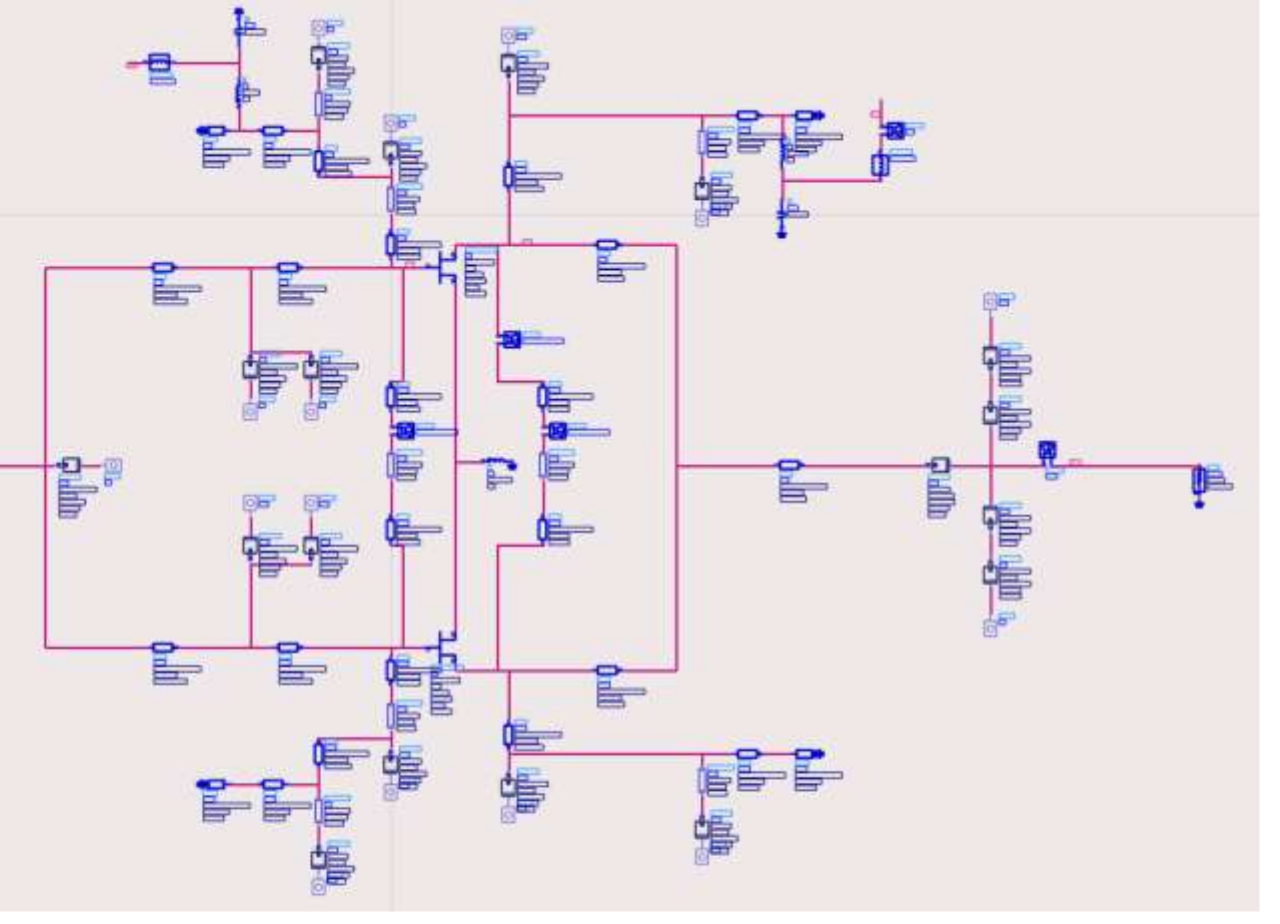
Device Level Simulations

- Unit Device Size = 8x150μm
- Bias Point = 75 / 37.5 mA/mm at 25V
- Fundamental and Harmonic Impedance Targets (Load / Source) @ 10GHz
  - Fundamental Load Target = 11.25Ω + j21.67Ω
  - 2nd Harmonic Load Target Phase = 50°, avoid 170°
  - 3rd Harmonic Load Target Phase = -135°, avoid 170°
  - Fundamental Source Target = 2.22Ω + j5.52Ω
  - 2nd Harmonic Source Target Phase = avoid 180° ± 20°
  - 3rd Harmonic Source Target Phase = avoid -160° ± 20°
- Number of Stages = 1
- Number of Devices in Output Stage = 2
  - Total quiescent current = 180mA / 90mA
- Expected performance:
  - Psat > 38dBm
  - PAE > 40%

Power Amplifier Schematic

(prior to layout and EM)

A single stage design consisting of 2, 8x150µm devices.

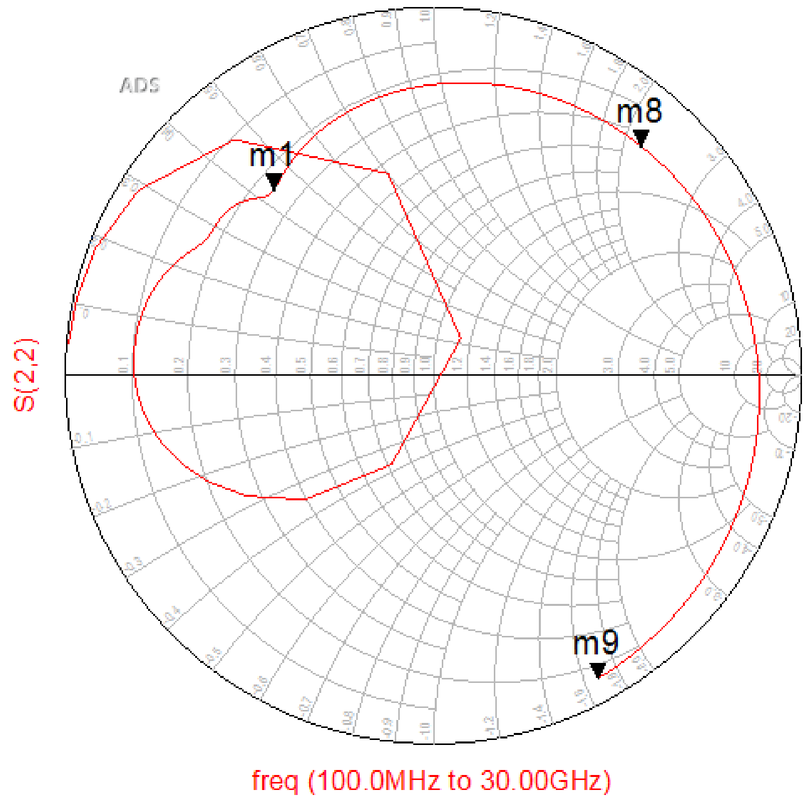


Schematic Design – Load Impedance

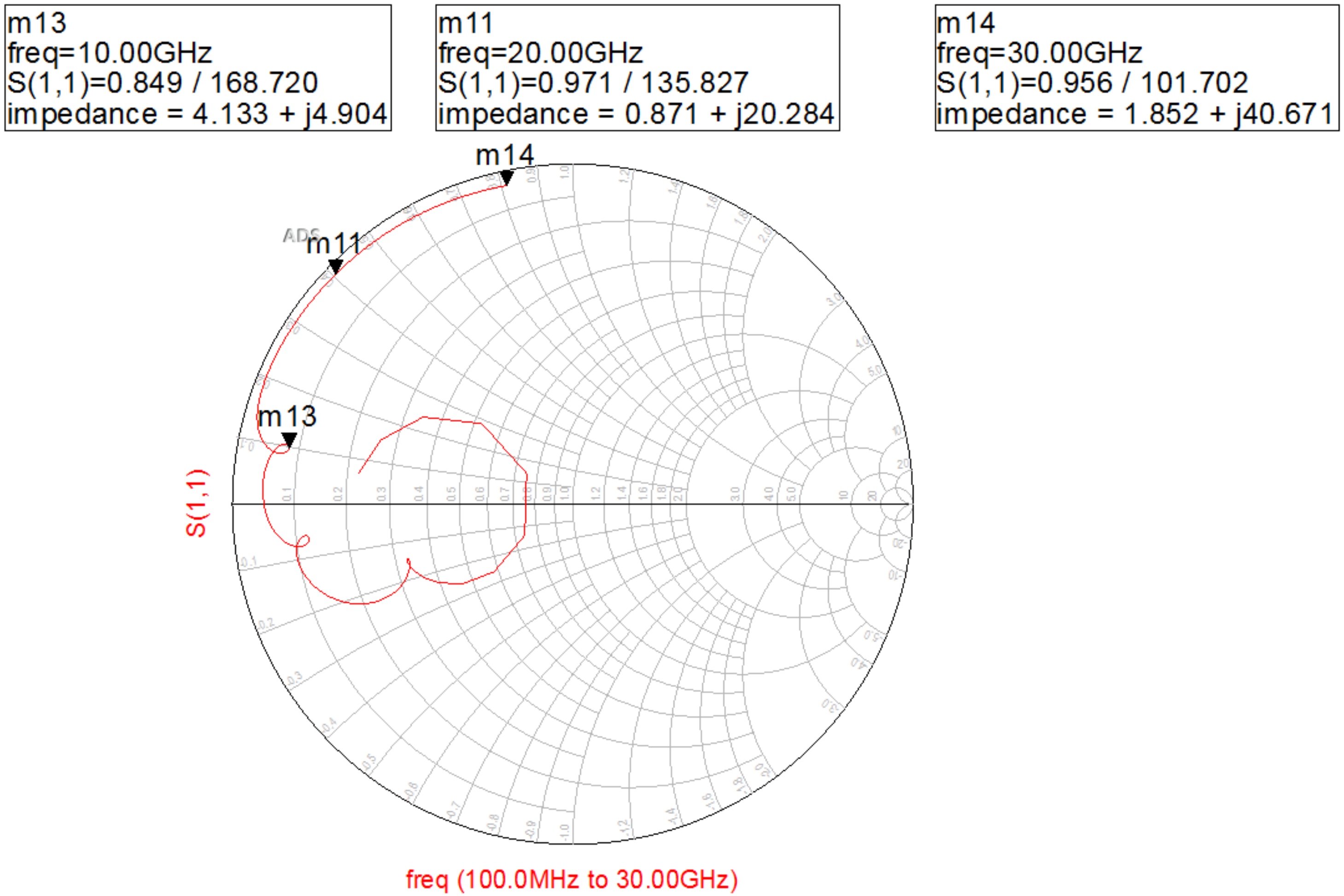
m1
freq=10.00GHz
S(2,2)=0.665 / 130.673
impedance = 12.081 + j21.842

m8
freq=20.00GHz
S(2,2)=0.840 / 47.833
impedance = 25.426 + j107.769

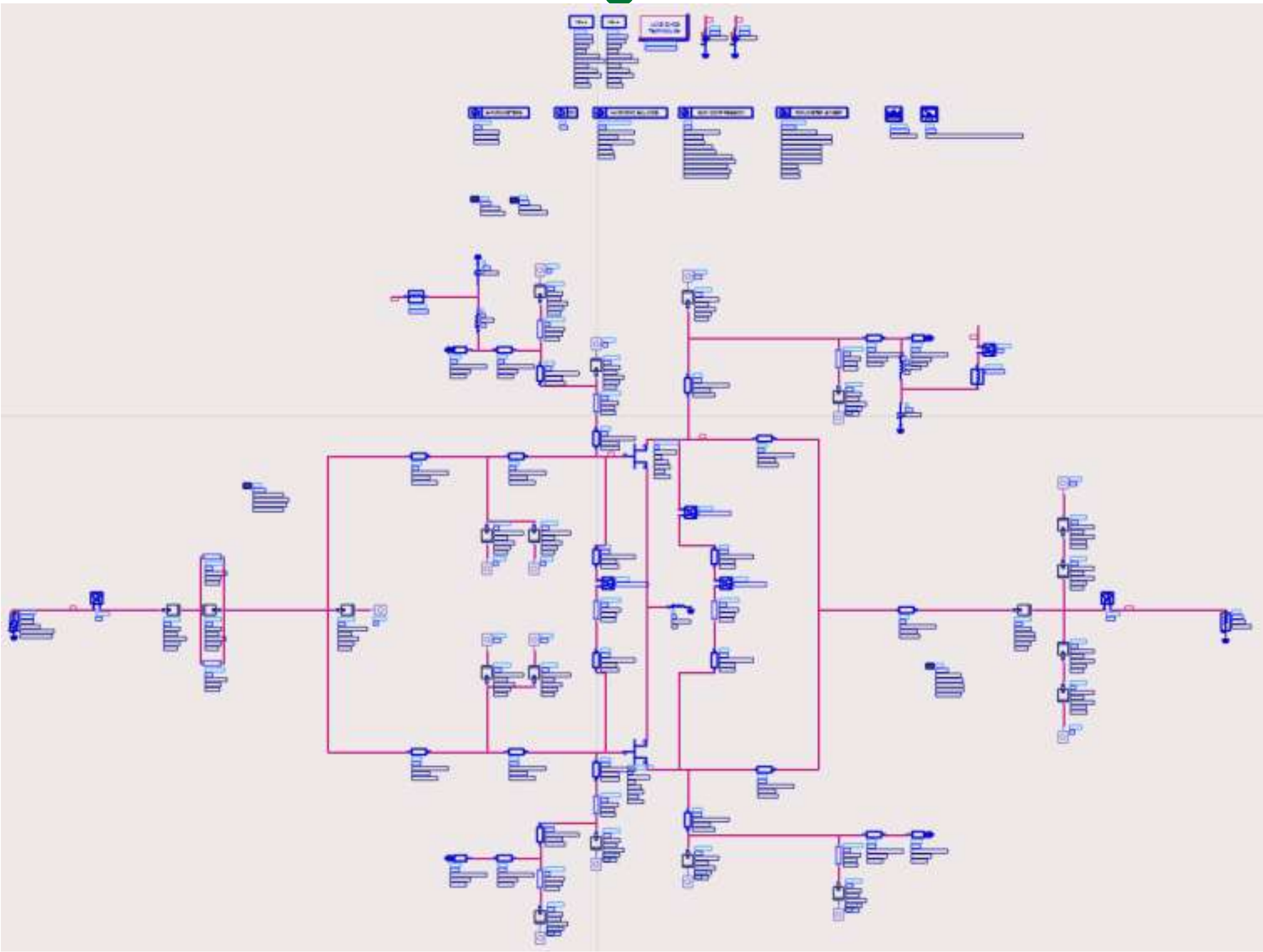
m9
freq=30.00GHz
S(2,2)=0.936 / -61.478
impedance = 6.312 - j83.727



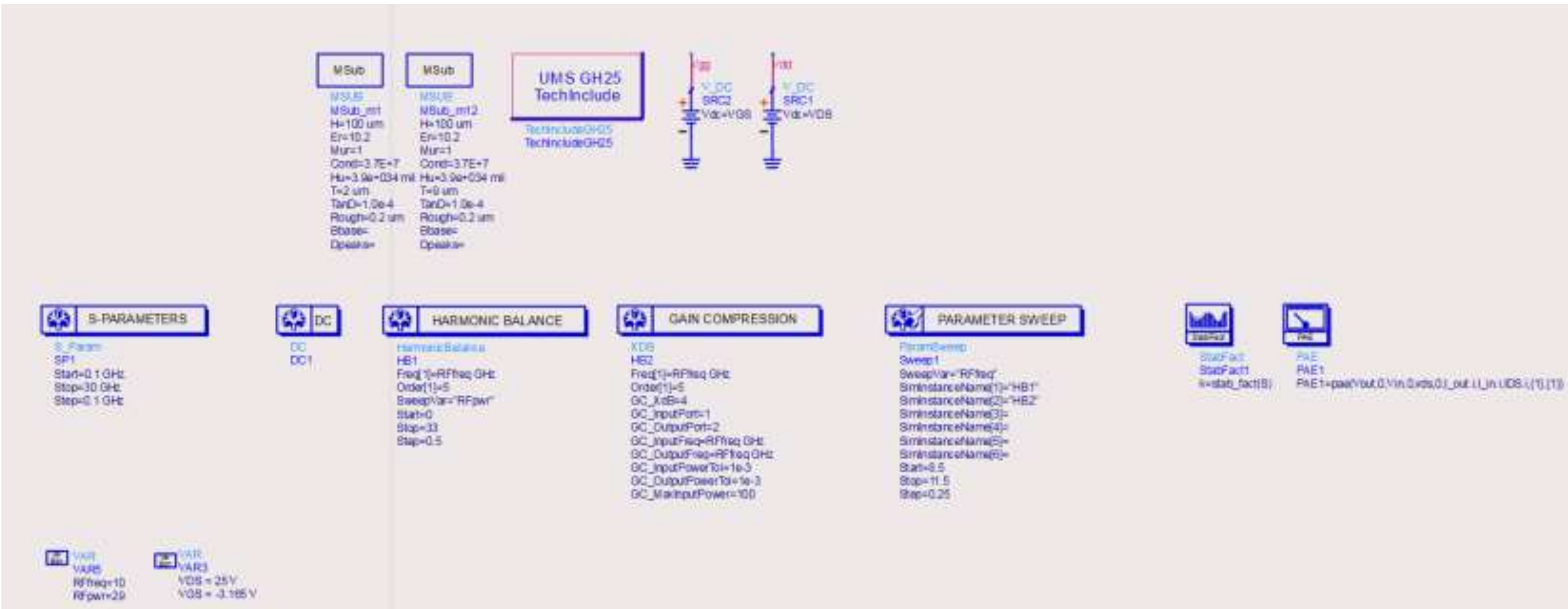
Schematic Design – Source Impedance



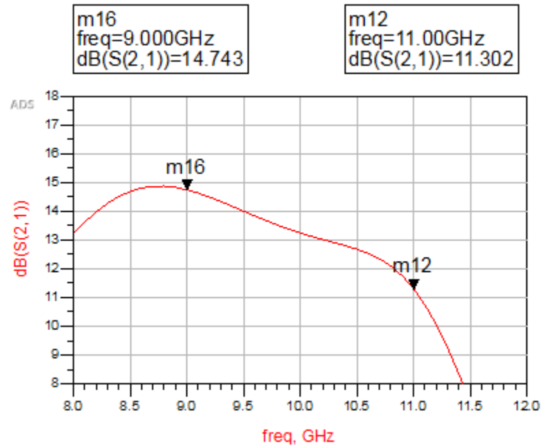
Schematic Design – Test Bench

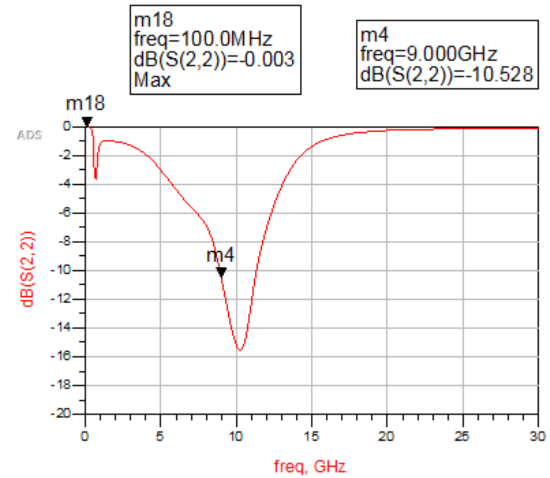


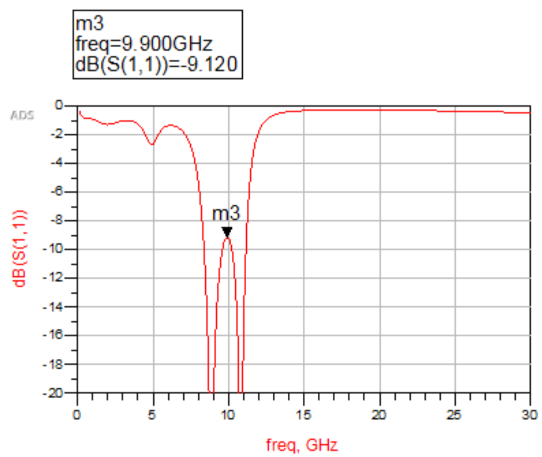
Schematic Design – Test Bench

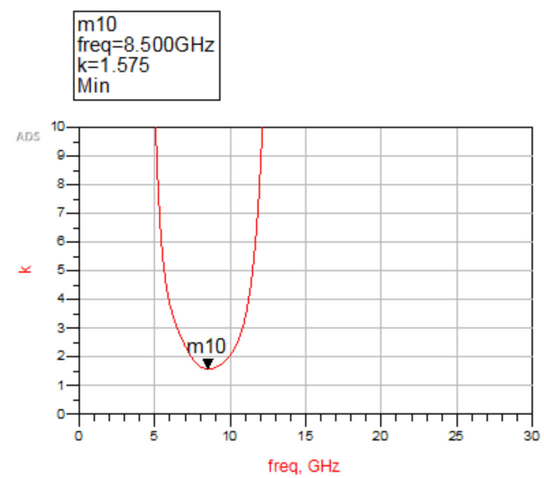


Schematic Design – Small Signal



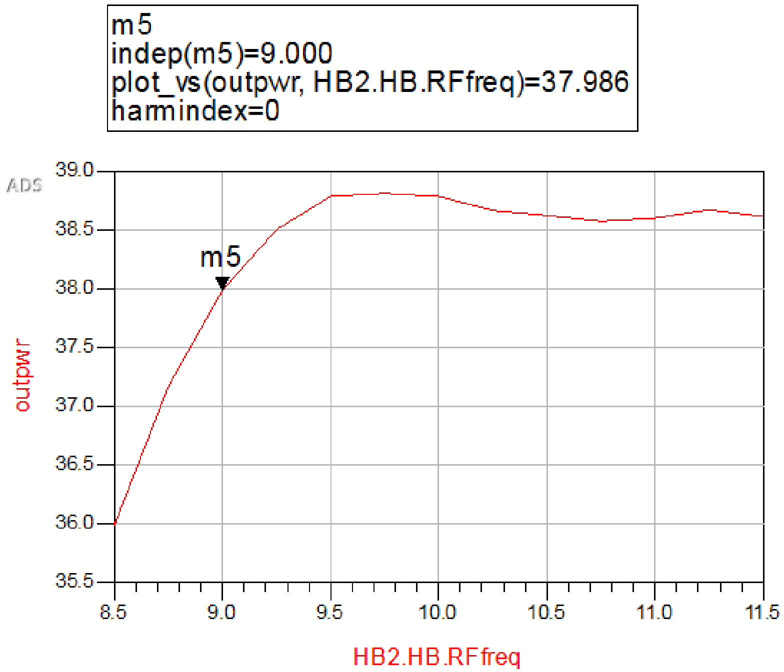


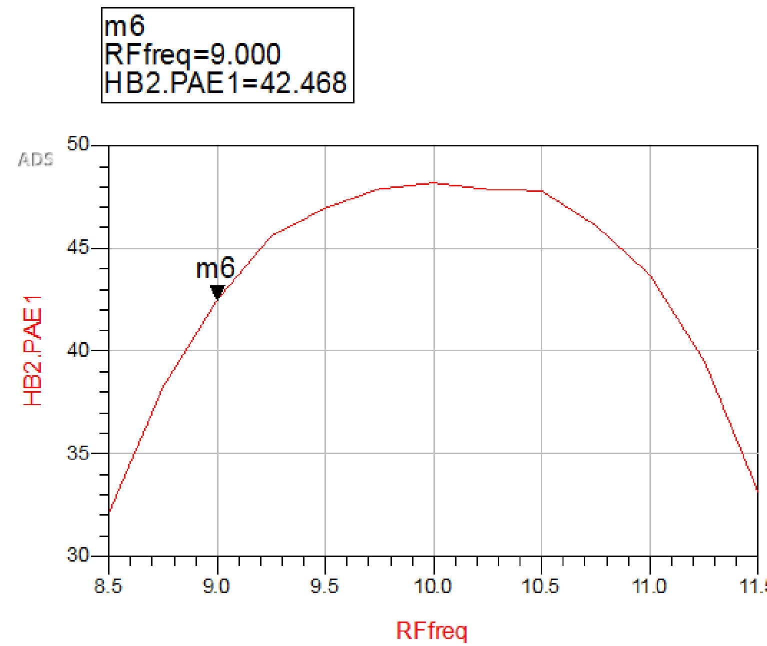




Quiescent Bias Point = 180mA at 25V

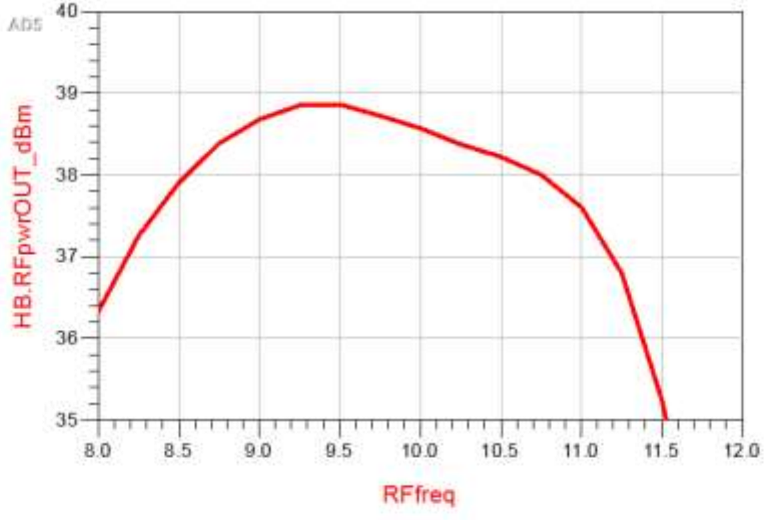
Schematic Design – Large Signal at 4dB Compression

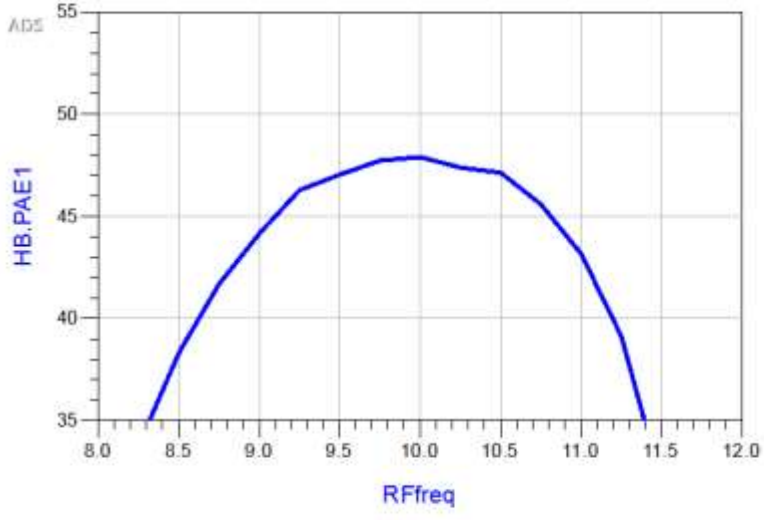




Quiescent Bias Point = 180mA at 25V

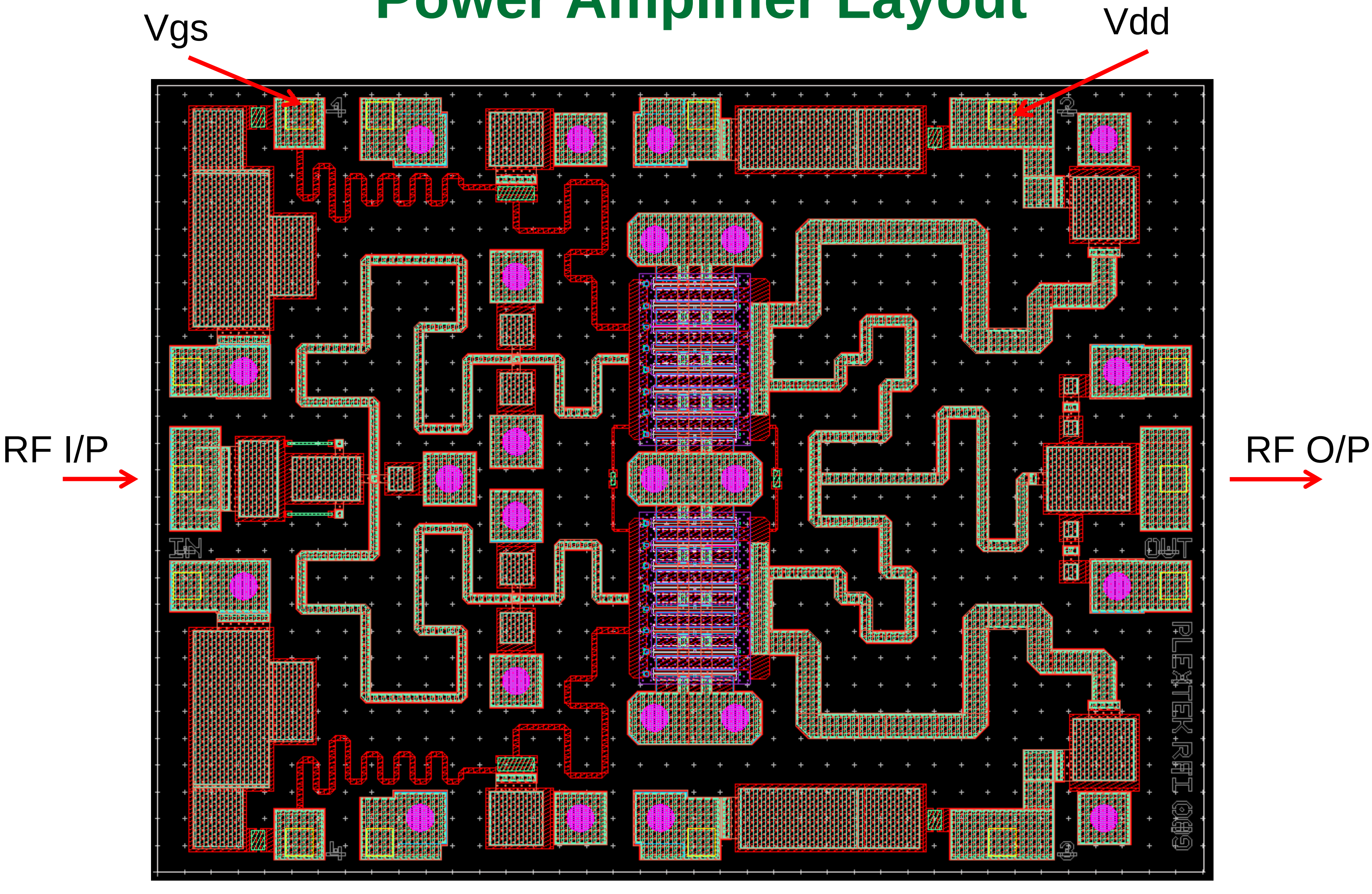
Pout and PAE for +29dBm Drive



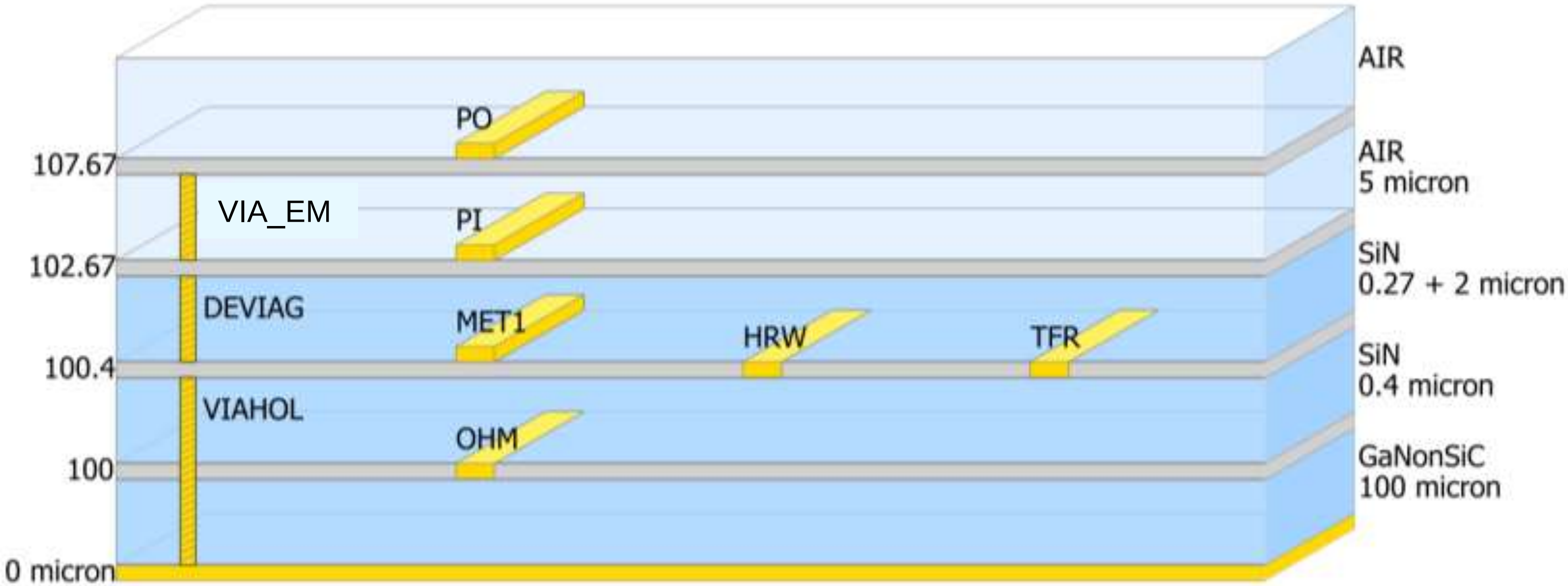


Quiescent Bias Point = 180mA at 25V

Power Amplifier Layout



EM Simulation Stack-Up



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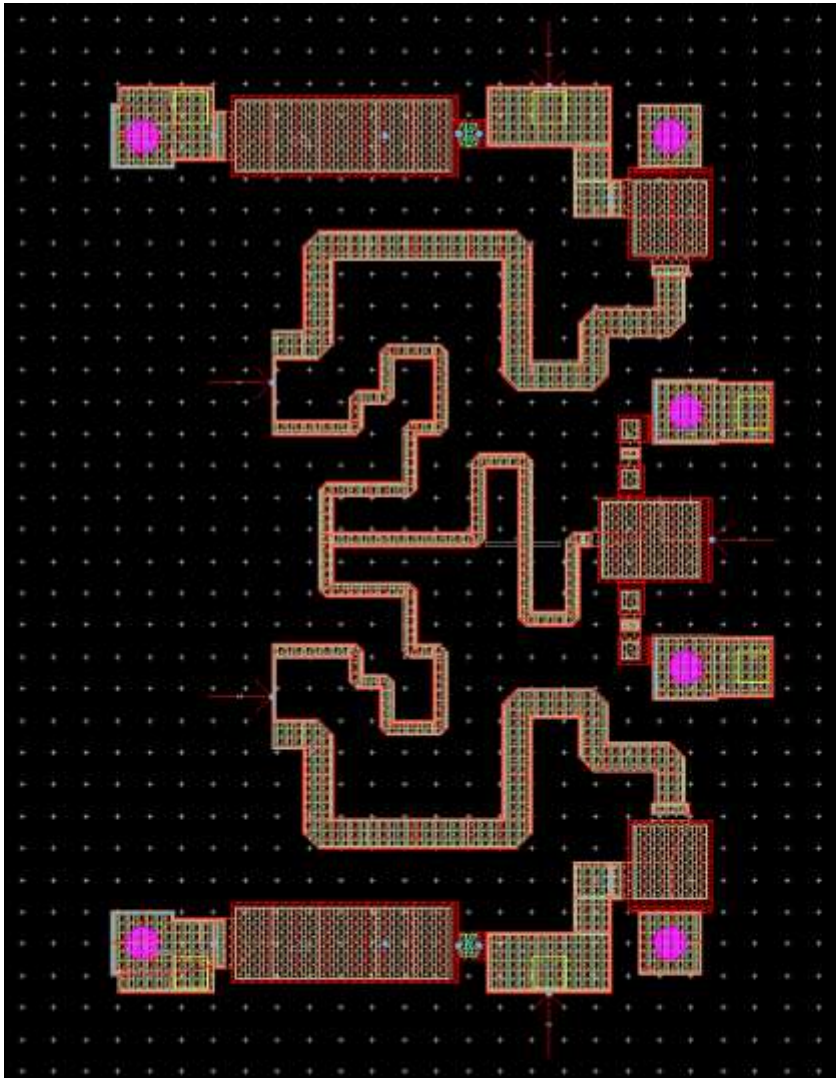
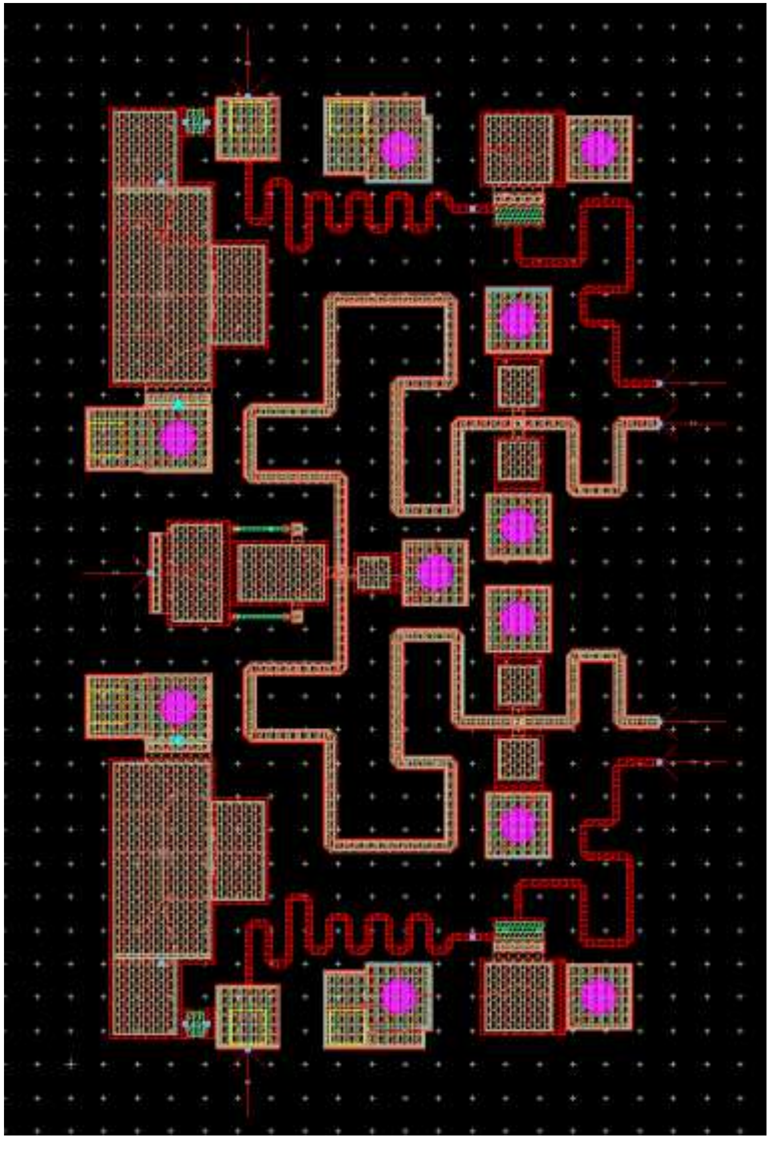
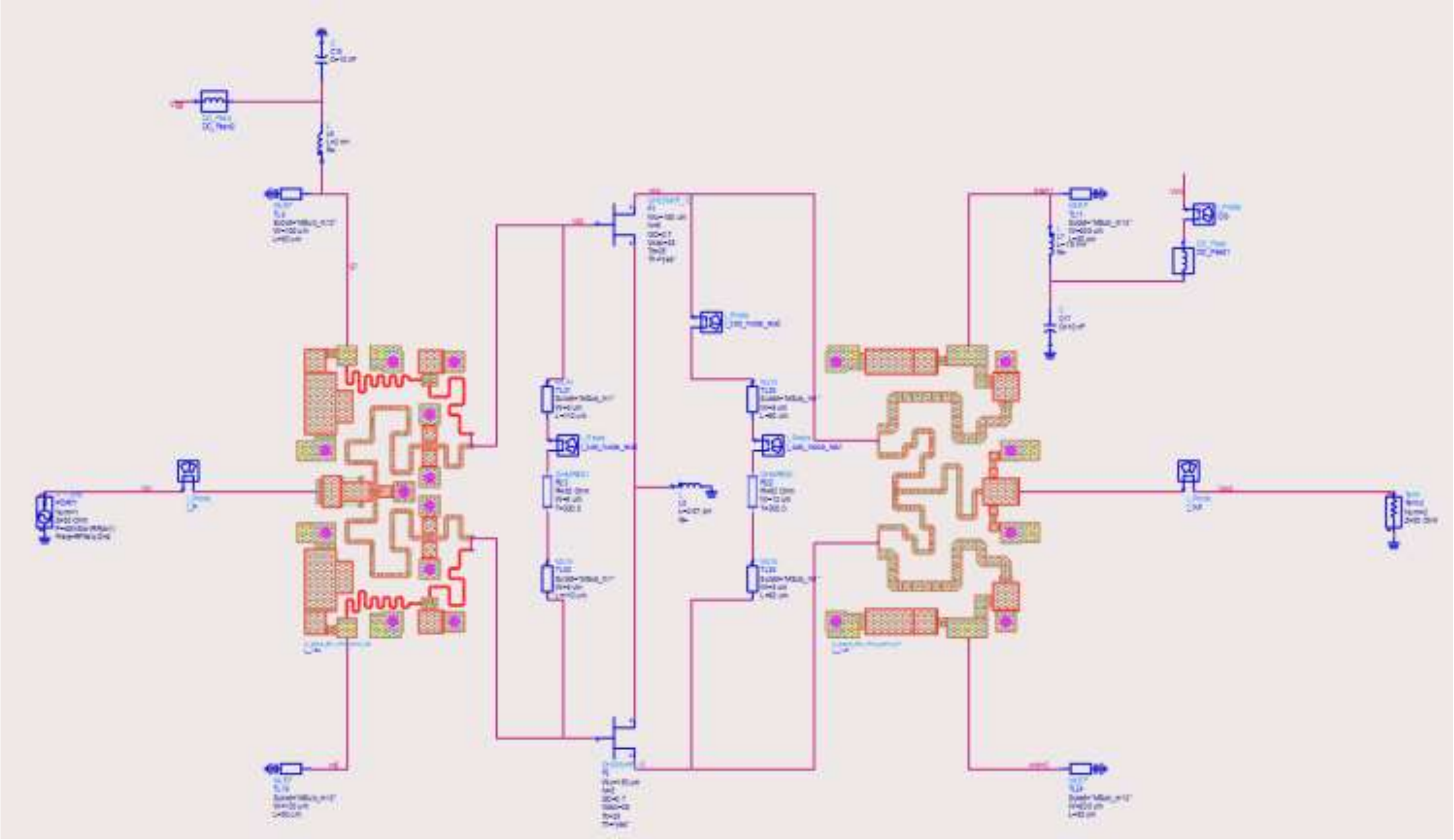
EM Simulation OPMN



EM Simulation IPMN



Updated Schematic – Full EM Simulation



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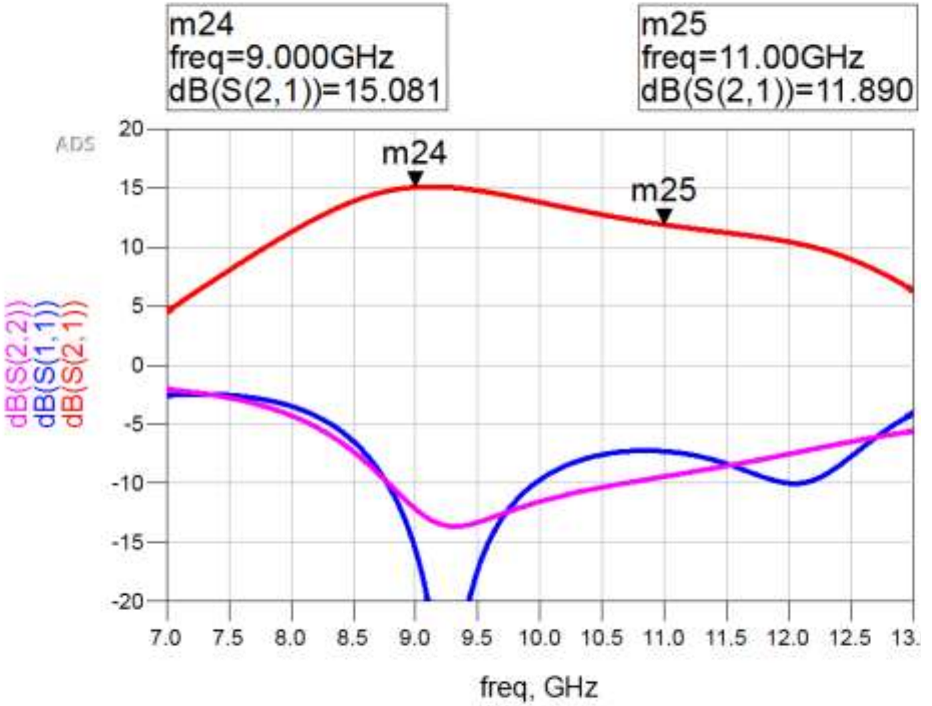
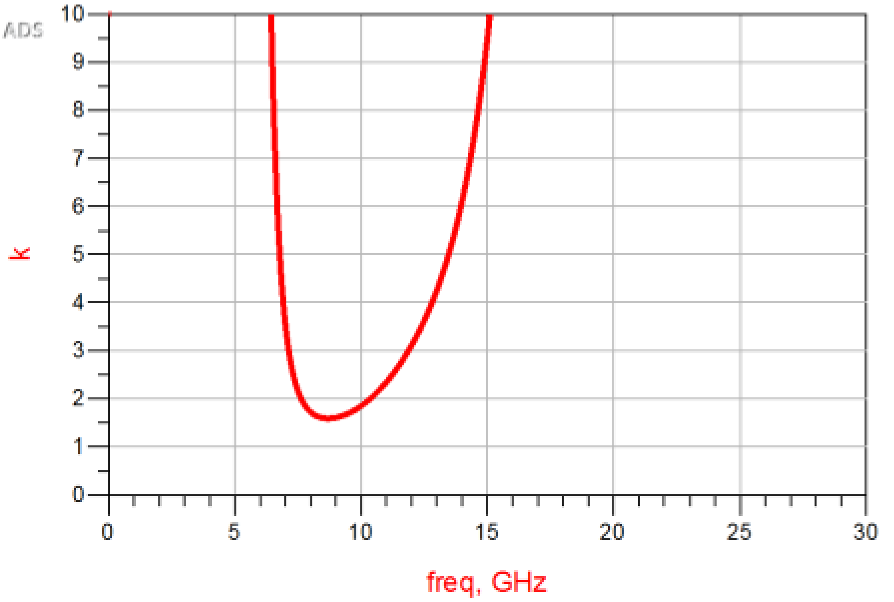
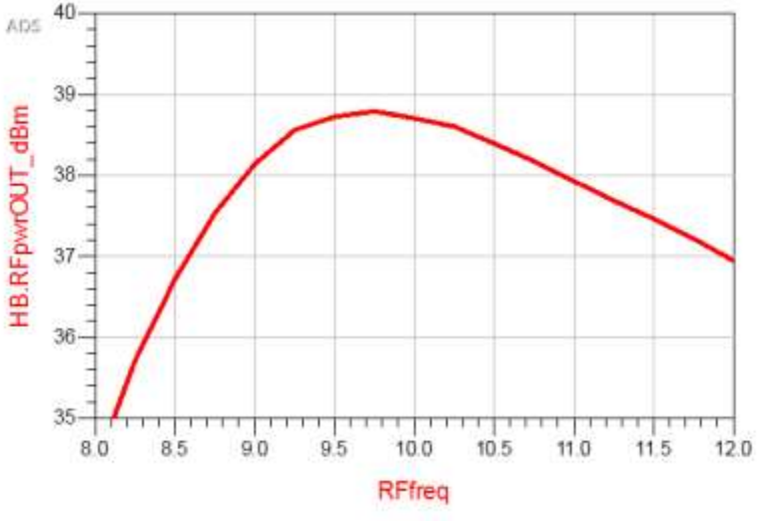
Power Amplifier Simulated Performance Including Full EM – Small Signal

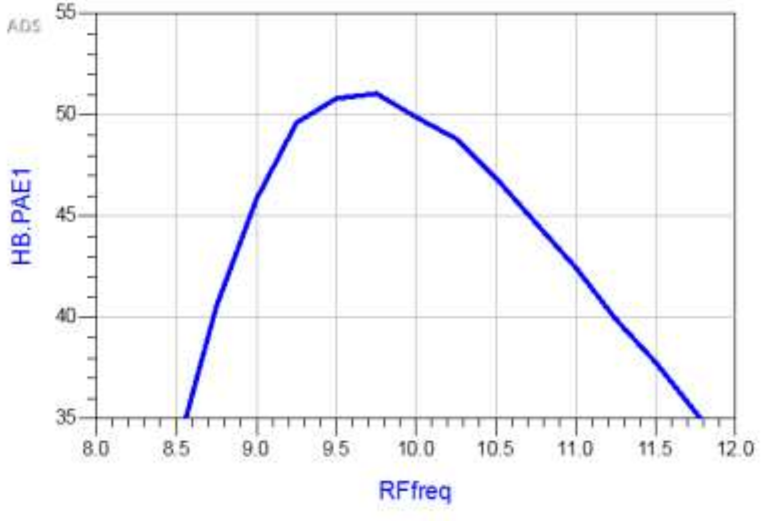




Quiescent Bias Point = 180mA at 25V

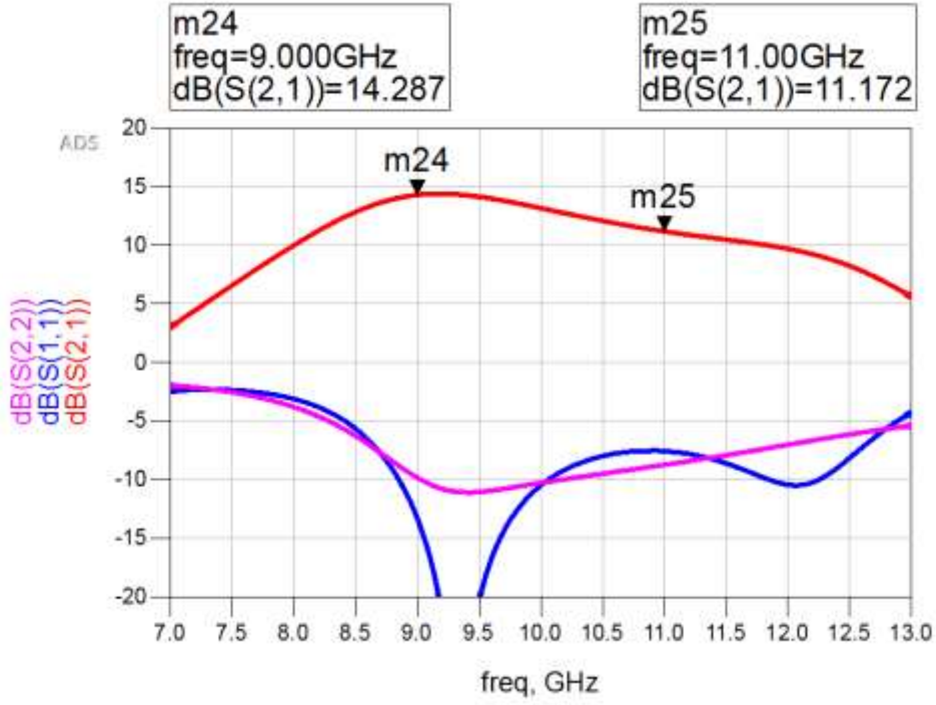
Pout and PAE for +29dBm Drive
Full EM Simulation

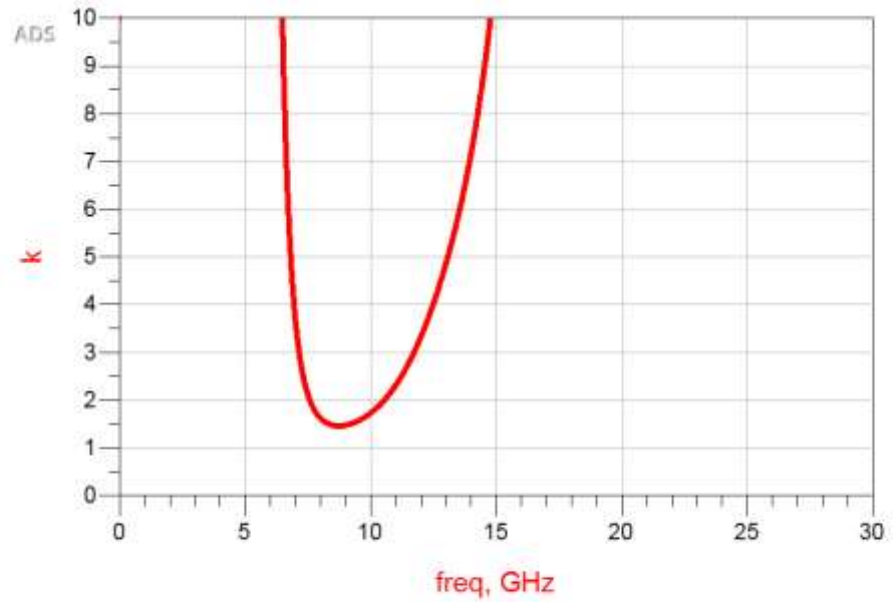




Quiescent Bias Point = 180mA at 25V

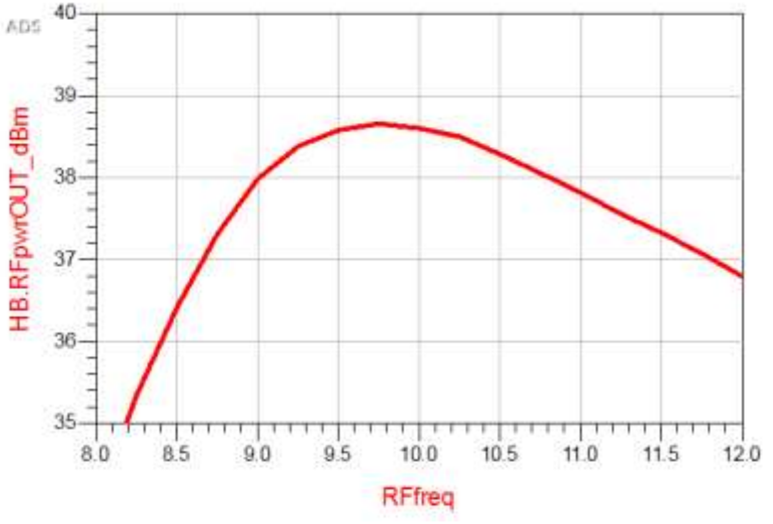
Power Amplifier Simulated Performance Including Full EM – Small Signal

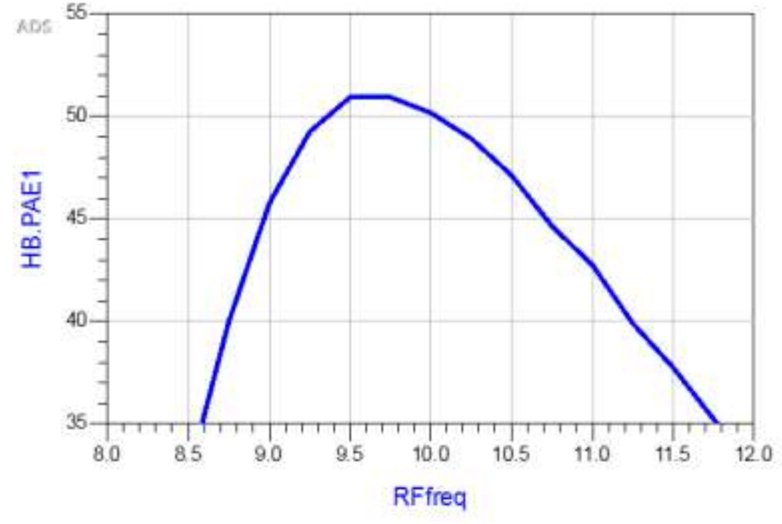




Quiescent Bias Point = 90mA at 25V

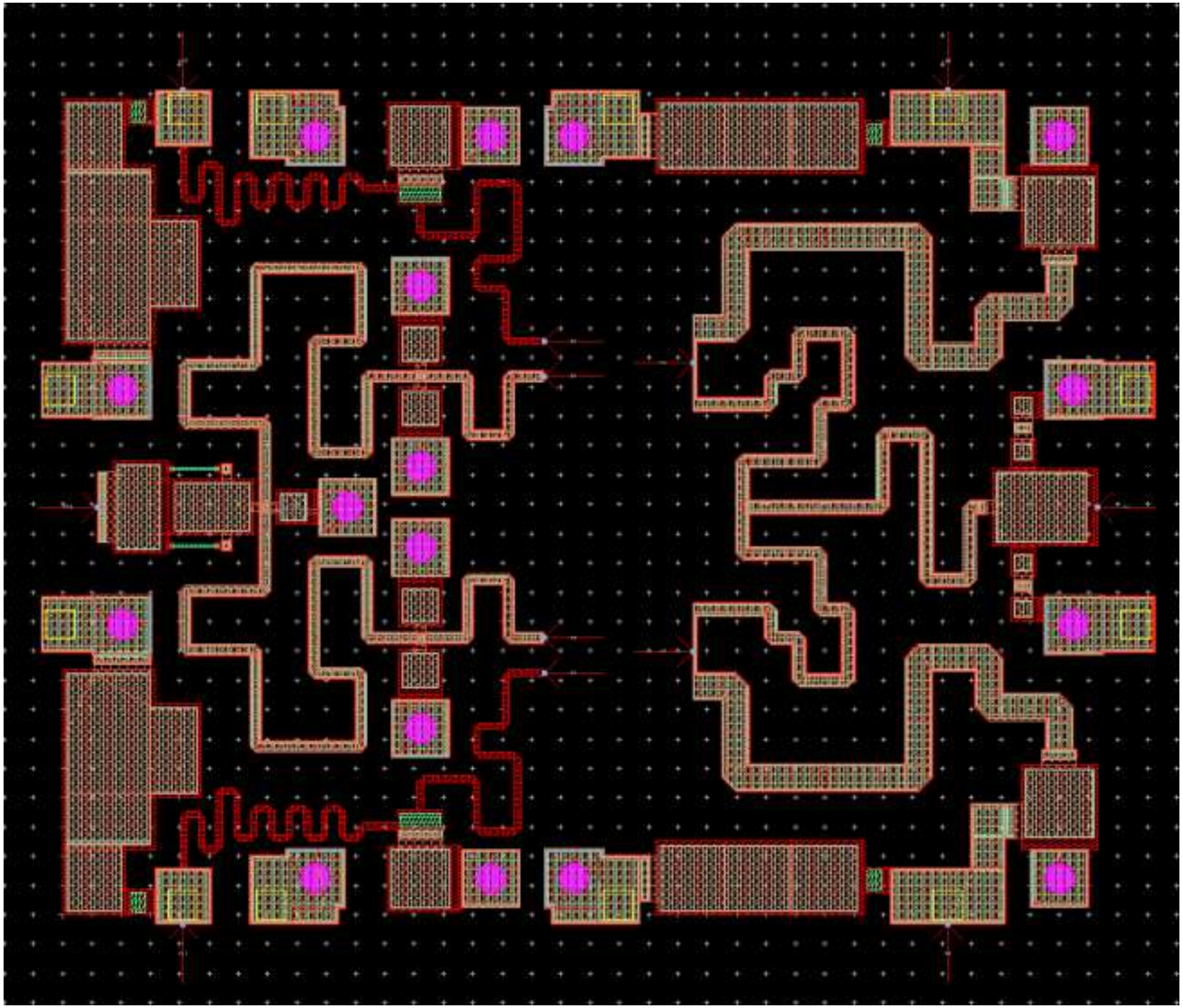
Pout and PAE for +29dBm Drive
Full EM Simulation





Quiescent Bias Point = 90mA at 25V

EM Simulation IPMN and OPMN Together



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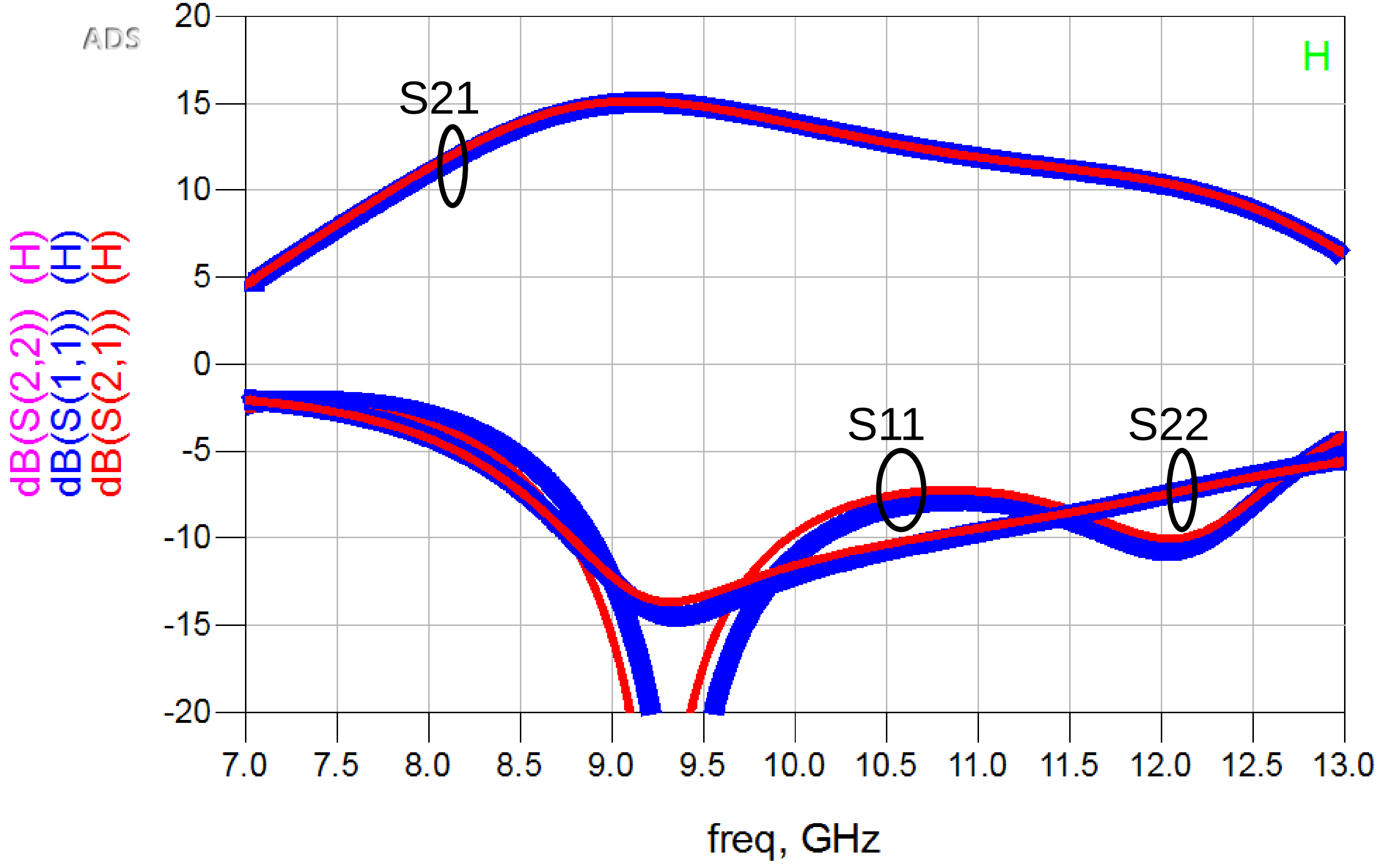
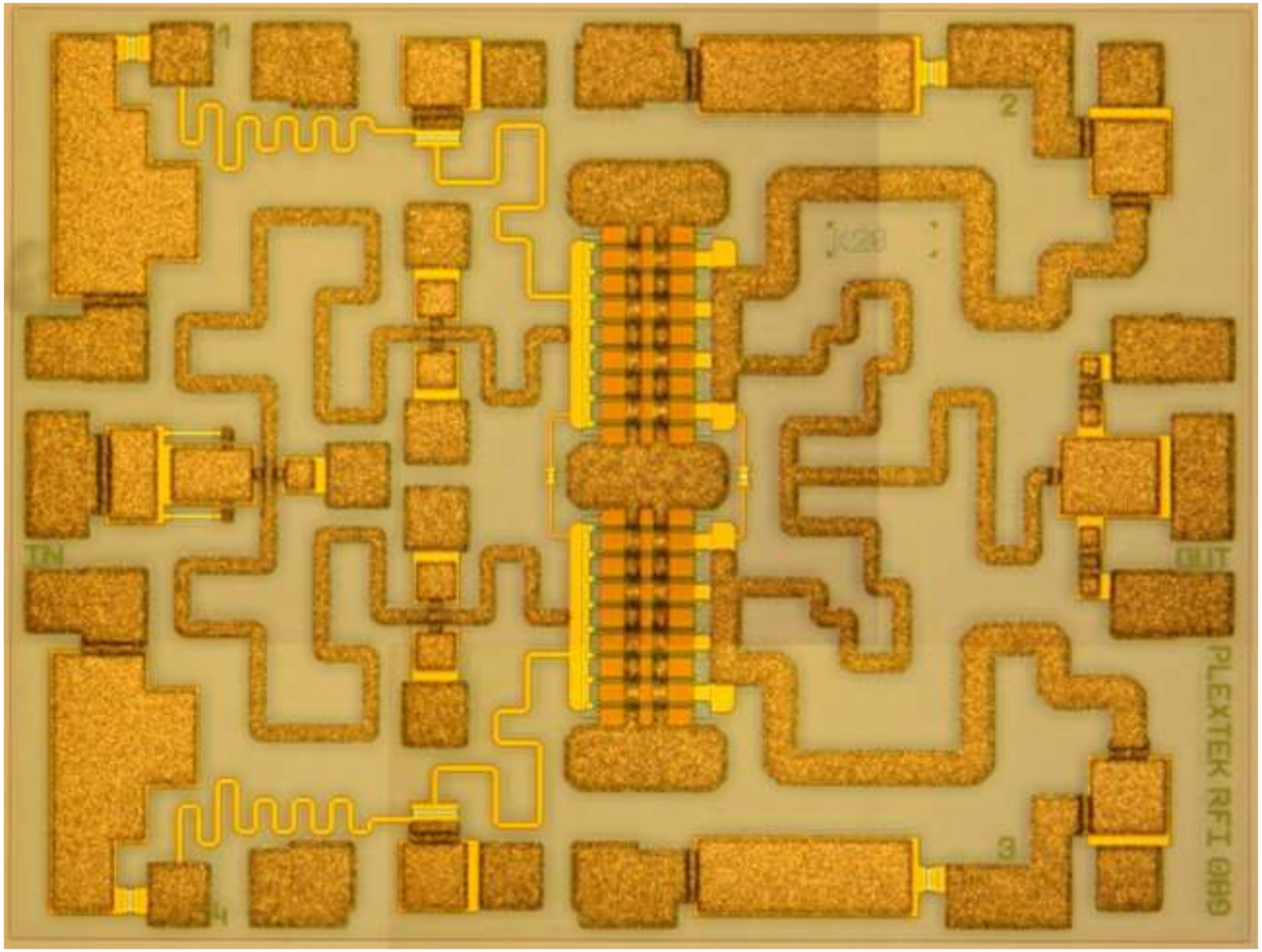
Comparing effect of EM simulating IPMN and OPMN together and separately



Quiescent Bias Point = 180mA at 25V

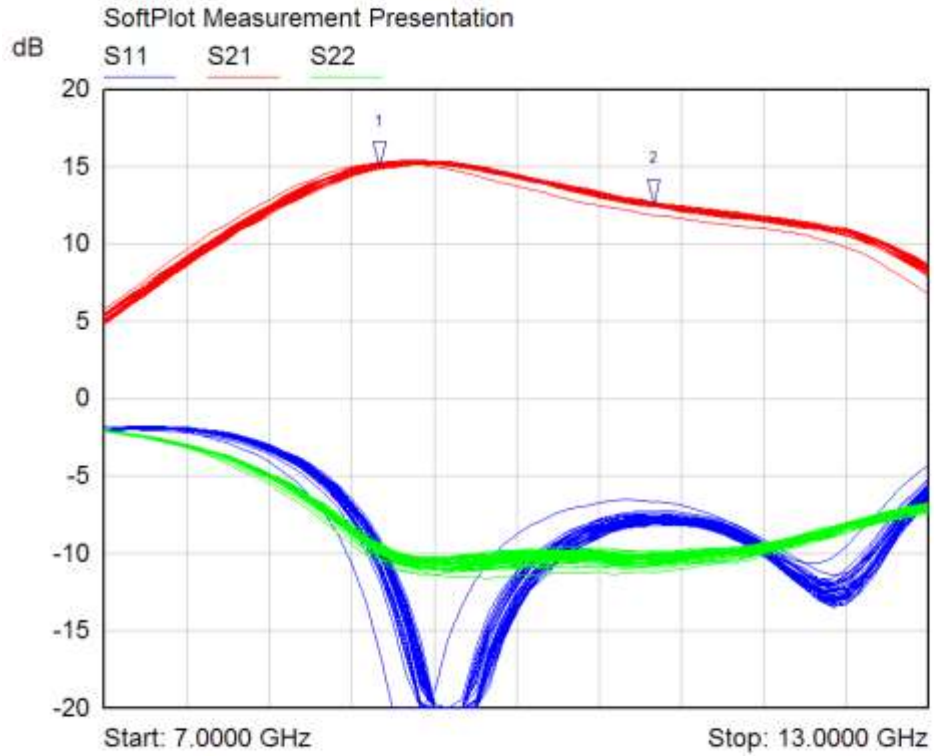
Photograph of the GaN PA MMIC



Die size: 1.5mm x 2mm (*around 2,300 die per 4" diameter wafer*)

Power Amplifier Measured S-Parameters

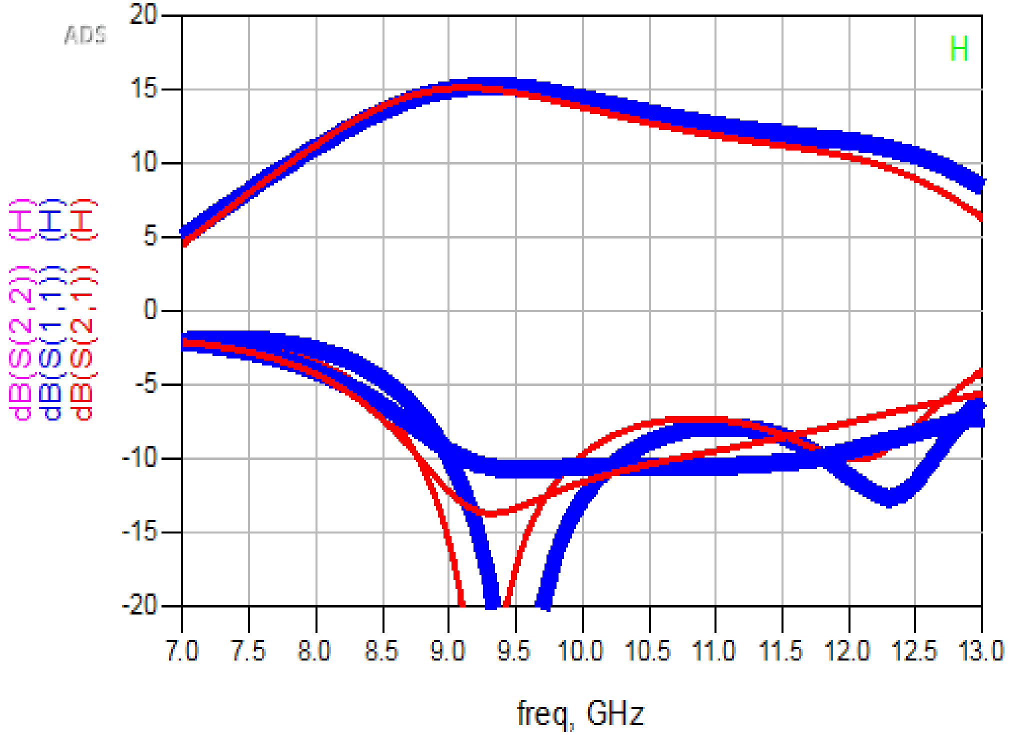
40 devices



Mkr	Trace	X-Axis	Value	Notes
1 ∇	S21	9.0000 GHz	15.00 dB	
2 ∇	S21	11.0000 GHz	12.60 dB	

Quiescent Bias Point = 180mA at 25V

Power Amplifier Measured Vs Modelled S-Parameters



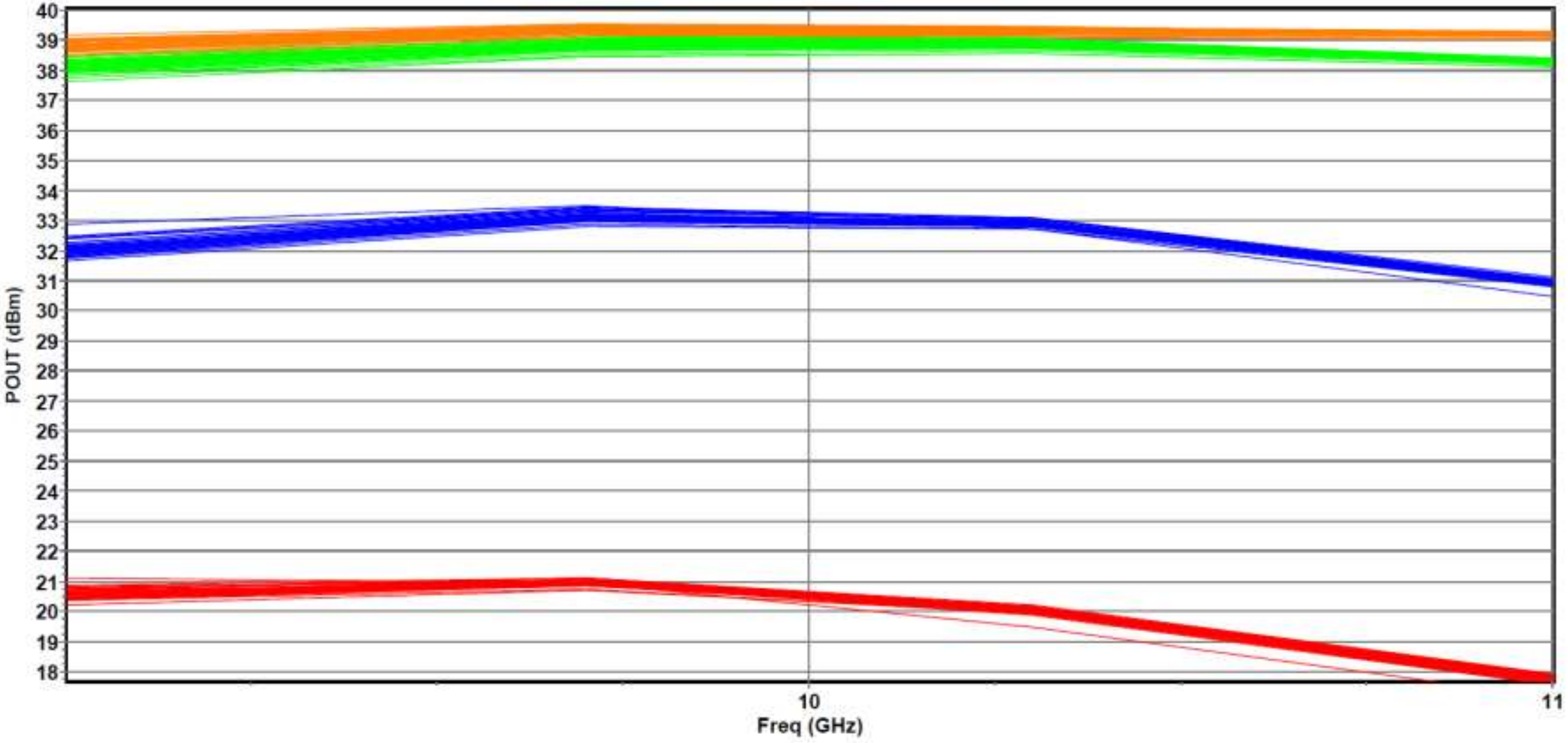
Measured in blue

Modelled in red

Quiescent Bias Point = 180mA at 25V

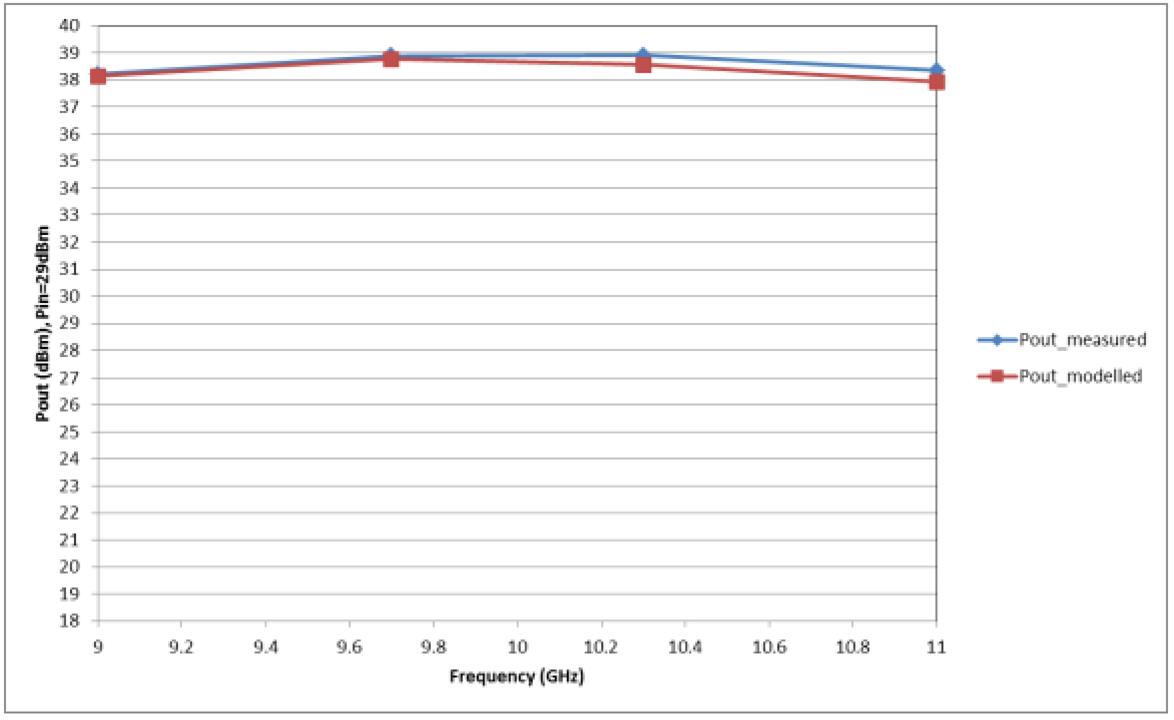
RFOW Measured Output Power

25µs and 10% Duty Cycle, input powers: 5dBm, 19dBm, 29dBm, 32dBm



Quiescent Bias Point = 180mA at 25V

Power Amplifier Measured Vs Modelled Pout for +29dBm input power

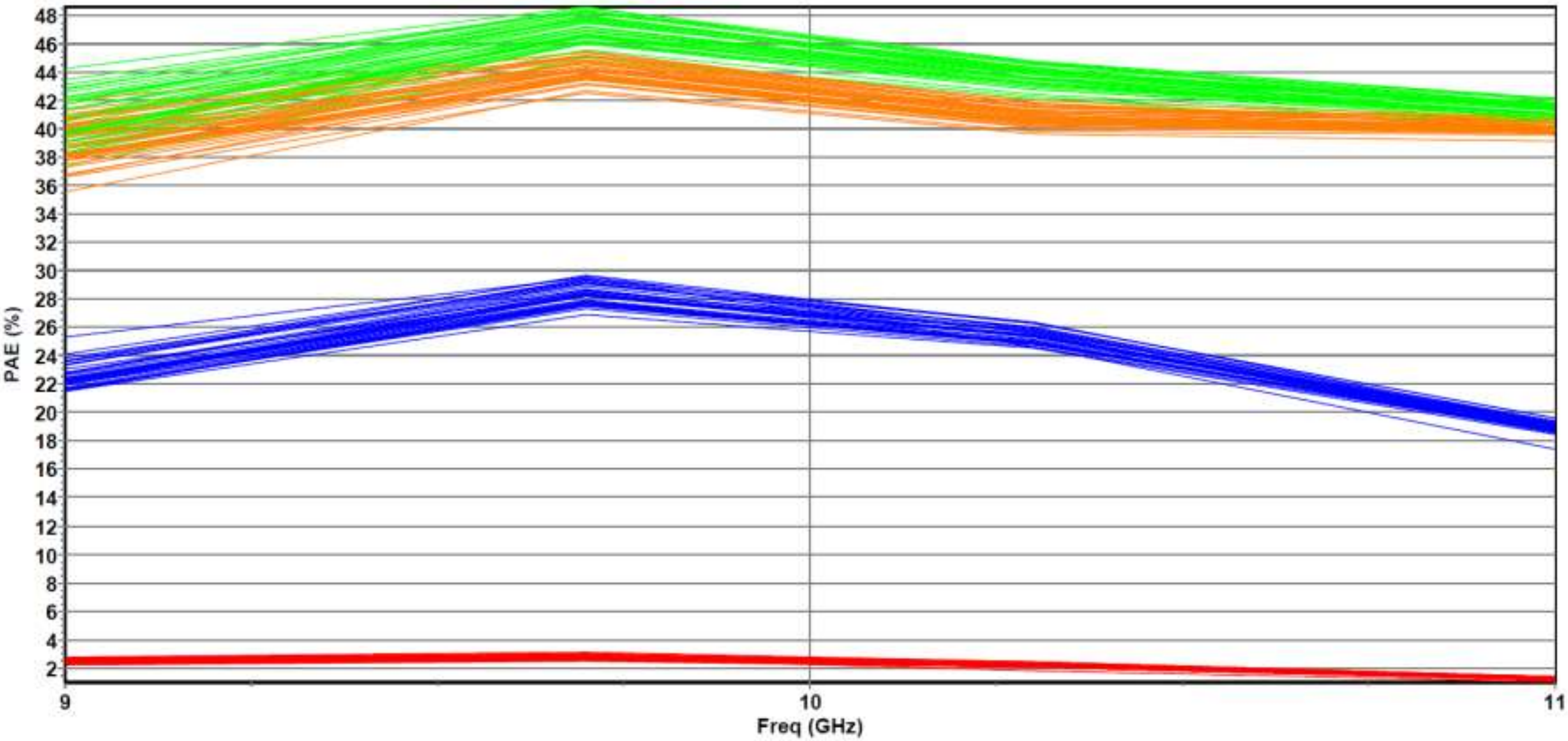


Measured in blue
Modelled in red

Quiescent Bias Point = 180mA at 25V

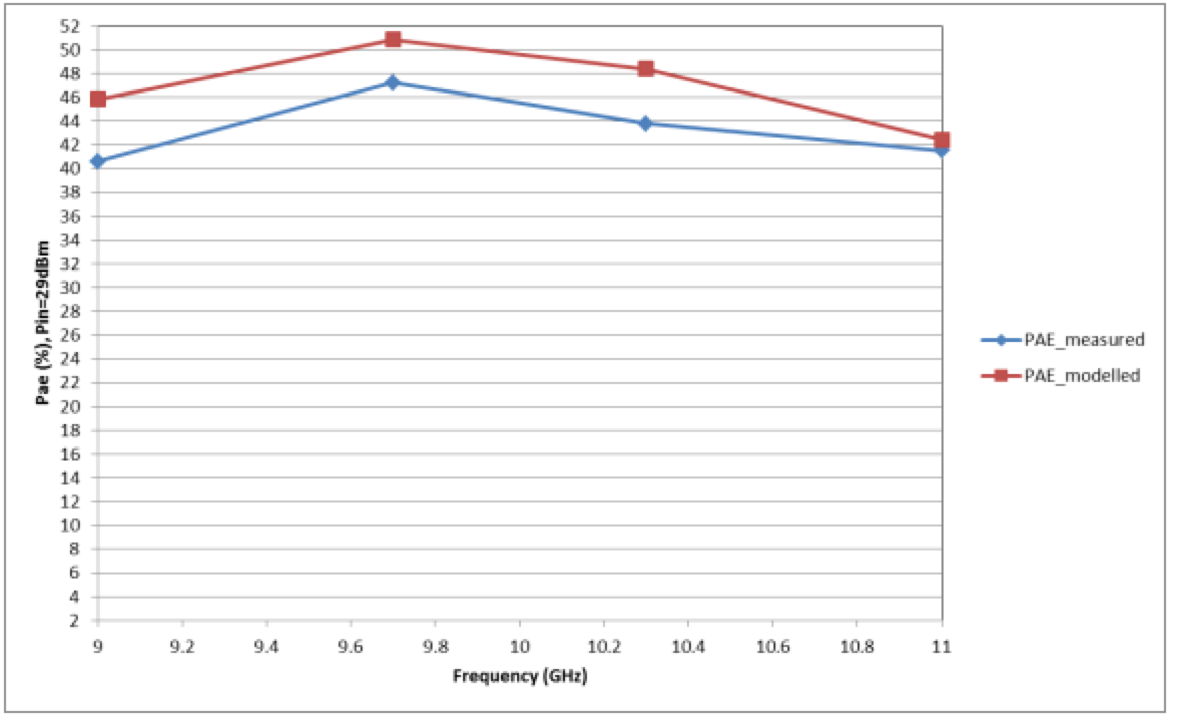
RFOW Measured PAE

25µs and 10% Duty Cycle, input powers: 5dBm, 19dBm, 29dBm, 32dBm



Quiescent Bias Point = 180mA at 25V

Power Amplifier Measured Vs Modelled PAE for +29dBm input power



Measured in blue
Modelled in red

Quiescent Bias Point = 180mA at 25V

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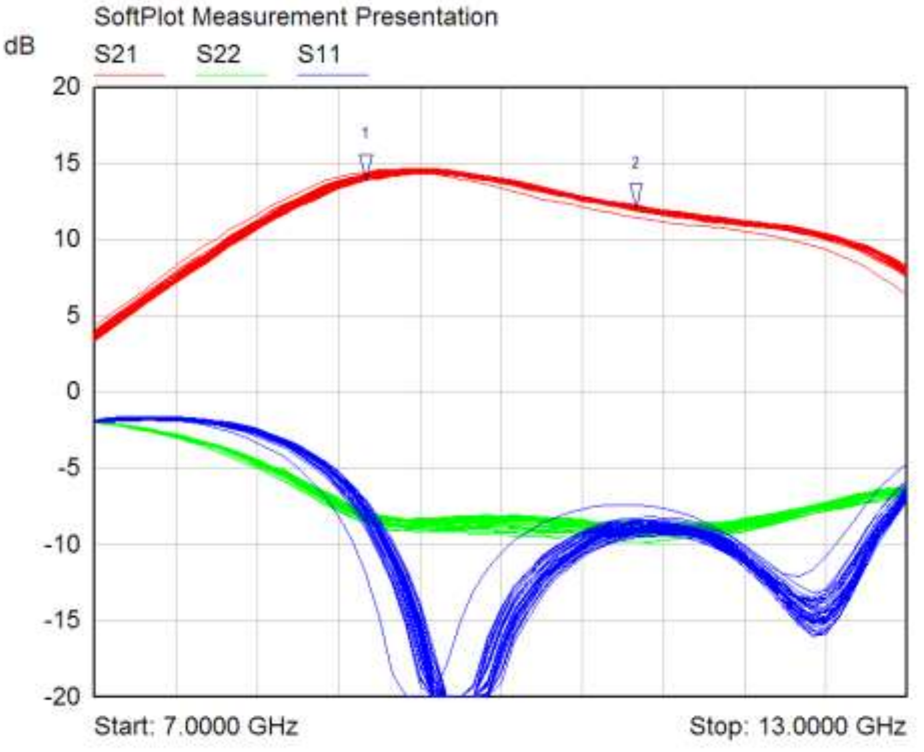
Power Amplifier Measured S-Parameters

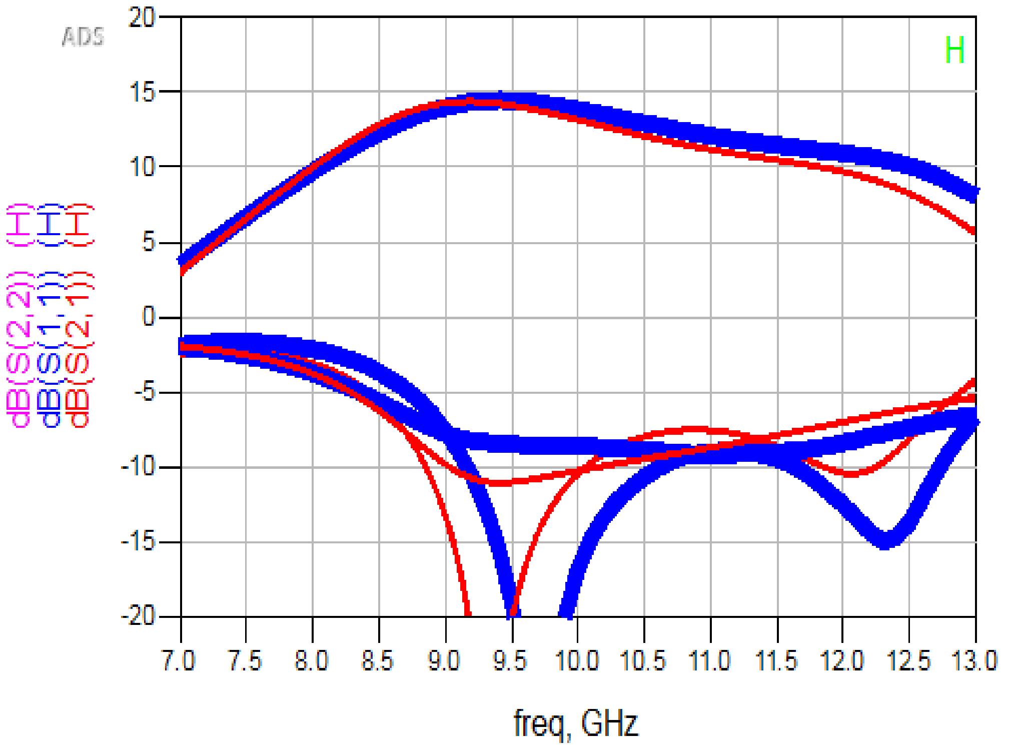
40 devices



Mkr	Trace	X-Axis	Value	Notes
1 ▽	S21	9.0000 GHz	14.00 dB	
2 ▽	S21	11.0000 GHz	12.09 dB	

Quiescent Bias Point = 90mA at 25V

Power Amplifier Measured Vs Modelled S-Parameters



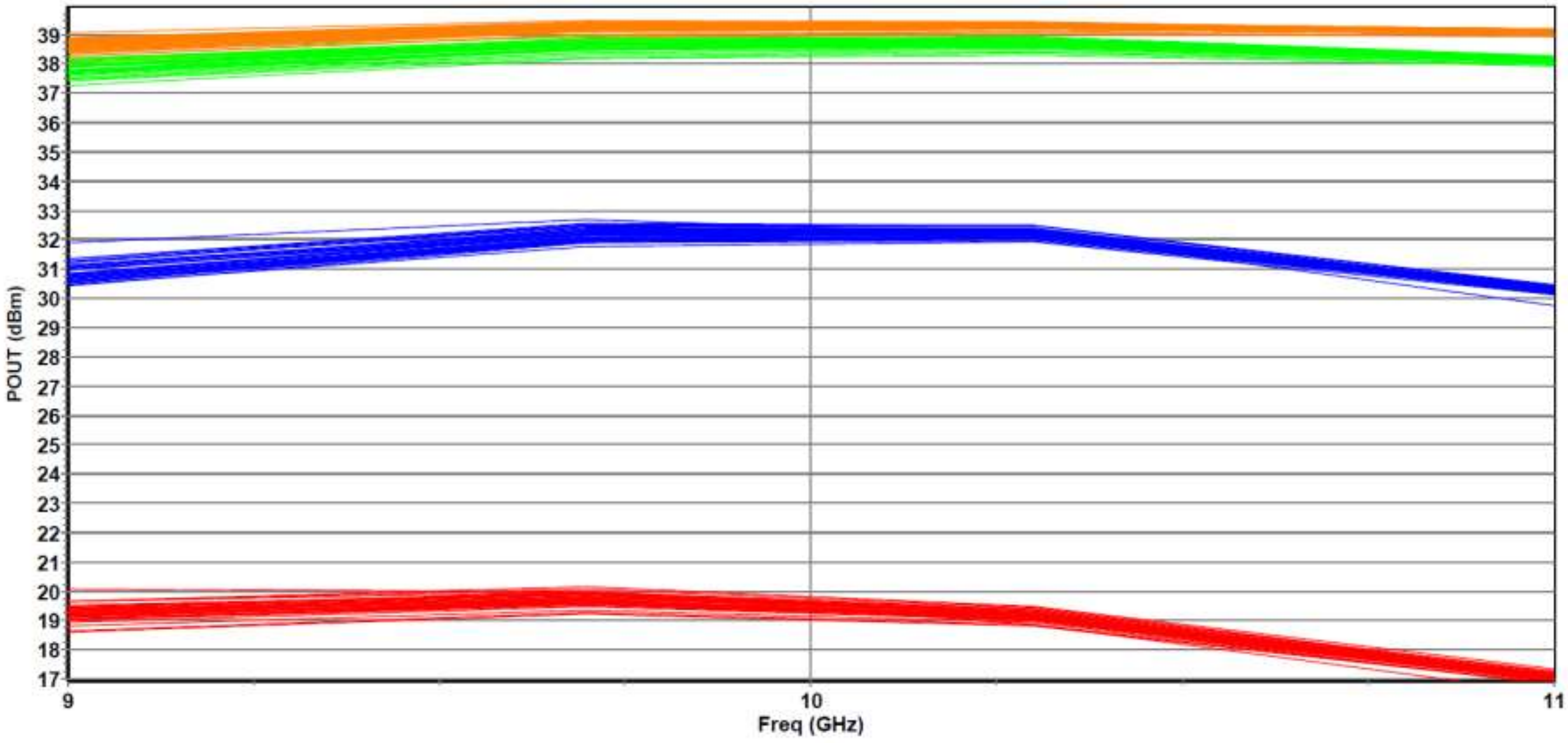
Measured in blue

Modelled in red

Quiescent Bias Point = 90mA at 25V

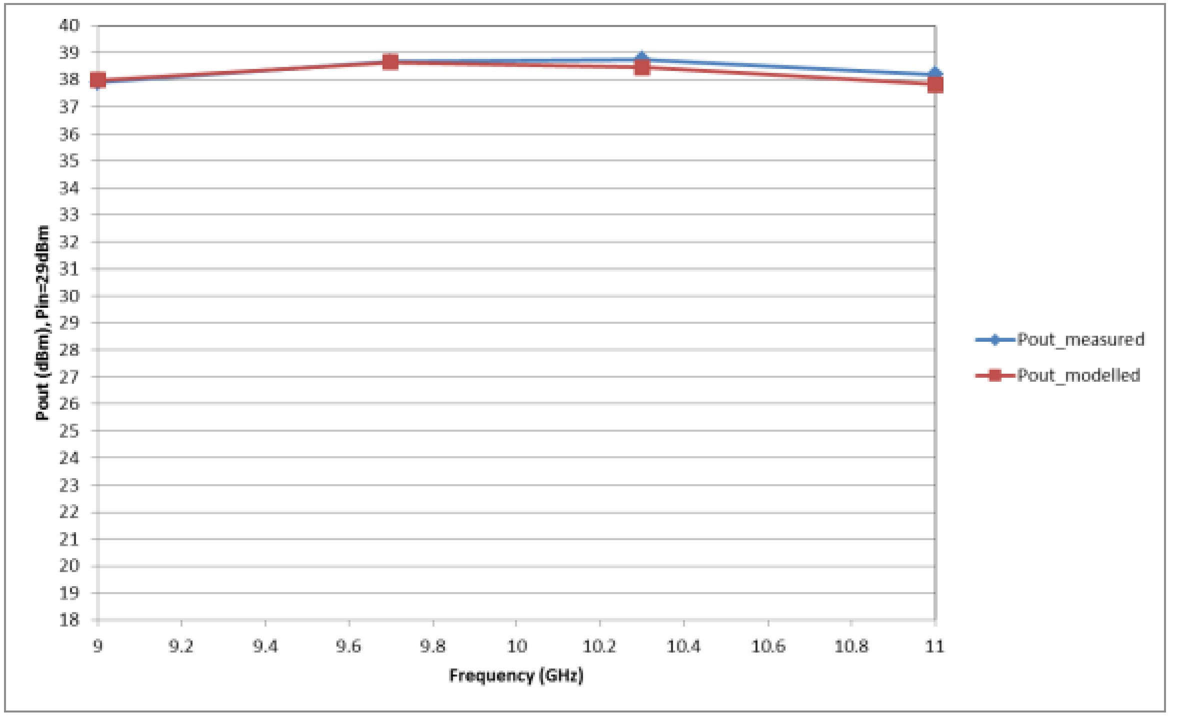
RFOW Measured Output Power

25µs and 10% Duty Cycle, input powers: 5dBm, 19dBm, 29dBm, 32dBm



Quiescent Bias Point = 90mA at 25V

Power Amplifier Measured Vs Modelled Pout for +29dBm input power



Measured in blue
Modelled in red

Quiescent Bias Point = 90mA at 25V

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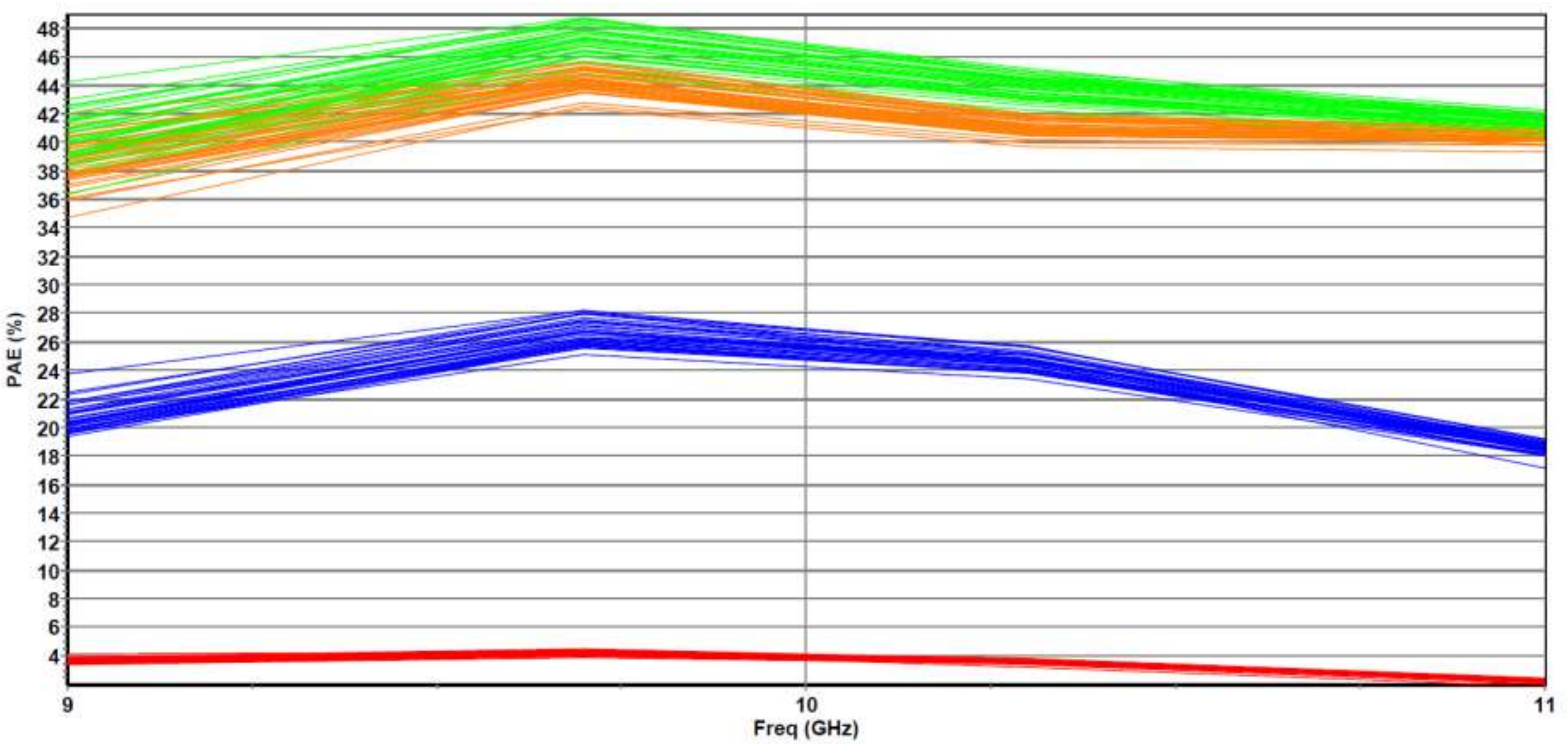
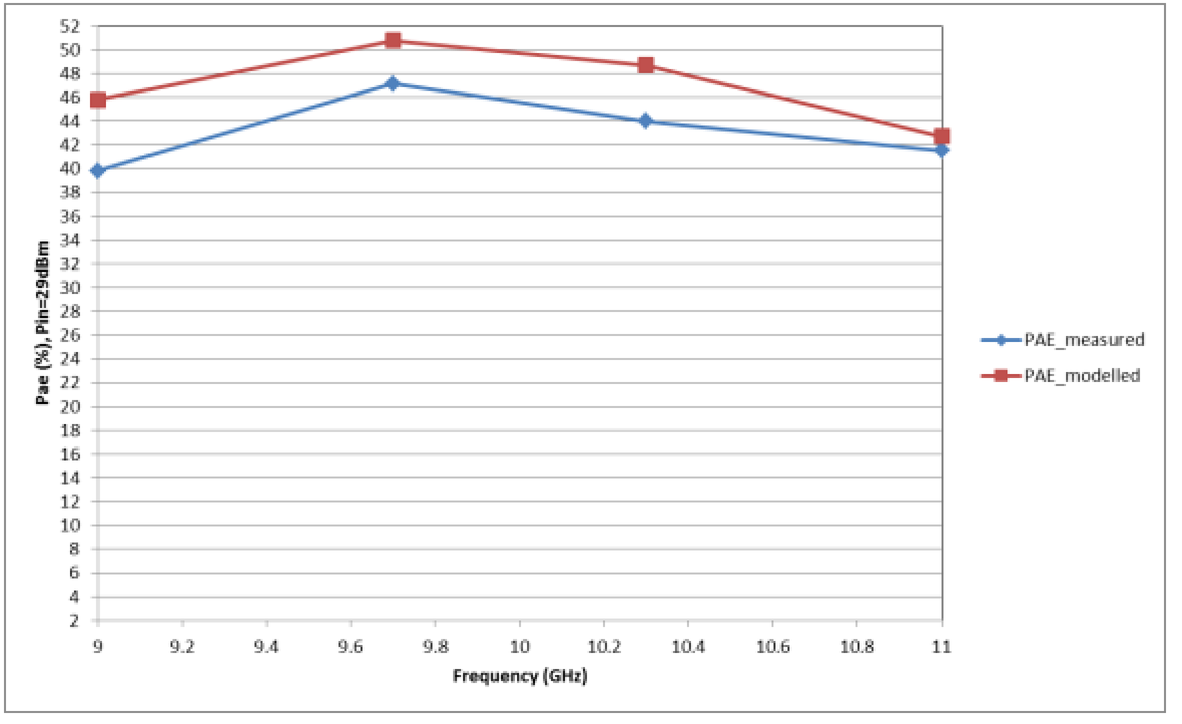
RFOW Measured PAE

25µs and 10% Duty Cycle, input powers: 5dBm, 19dBm, 29dBm, 32dBm



Quiescent Bias Point = 90mA at 25V

Power Amplifier Measured Vs Modelled PAE for +29dBm input power



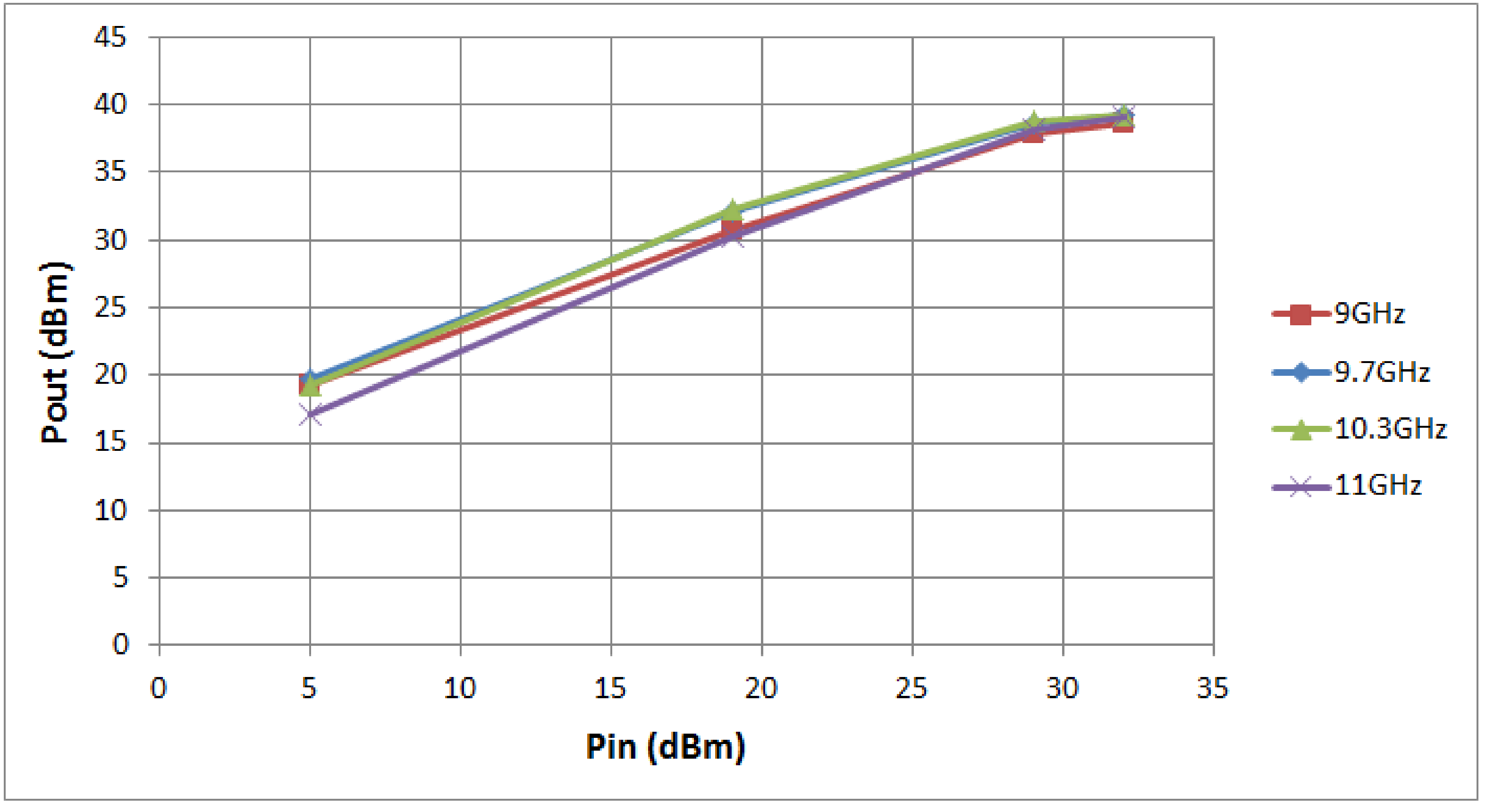
Measured in blue

Modelled in red

Quiescent Bias Point = 90mA at 25V

RFOW Measured Power Transfer

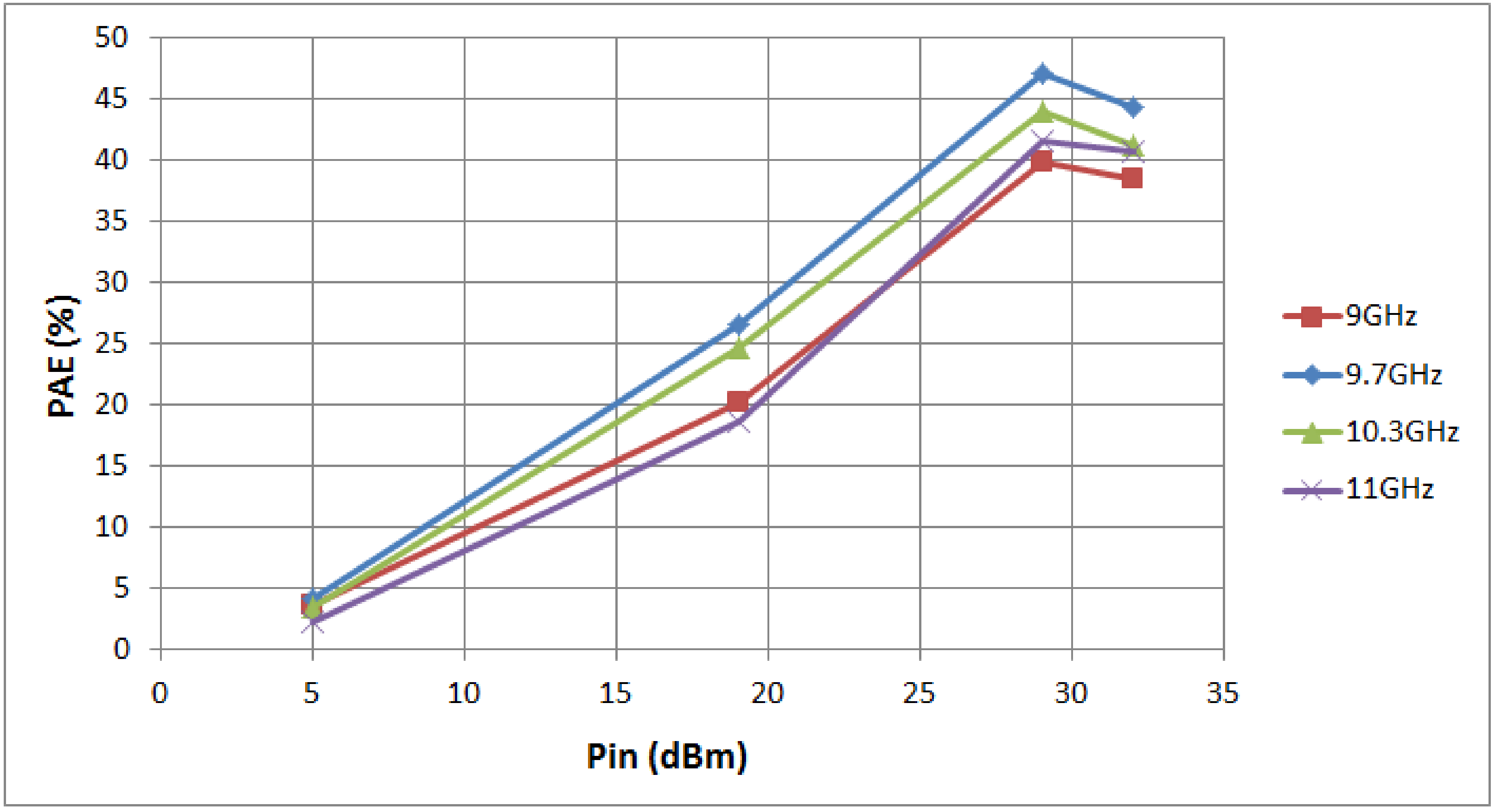
10% Duty Cycle



Quiescent Bias Point = 90mA at 25V

RFOW Measured PAE vs RF Drive

10% Duty Cycle



Quiescent Bias Point = 90mA at 25V

Plextek RFI

Measured Performance Summary

Quiescent bias, 25V and 90mA

Parameter	Units	Measured	Comment
Frequency	GHz	9 to 11.5	
SS Gain	dB	~ 13	
IRL	dB	> 8	
ORL	dB	> 8	
P_{sat}	dBm	~ 7W (38.5dBm)	+29dBm drive
PAE at Psat	%	~ 42	+29dBm drive
LS gain flatness	dB	± 0.5	

Conclusion

- How to Design an X-Band MMIC PA
  - Thorough device level simulations
  - Careful choice of matching network topology
  - Thorough EM simulations to optimize the layout
- Thankyou for attending
- For more information please see our website
  - www.plextekrfi.com
- Any Questions?

You're Invited

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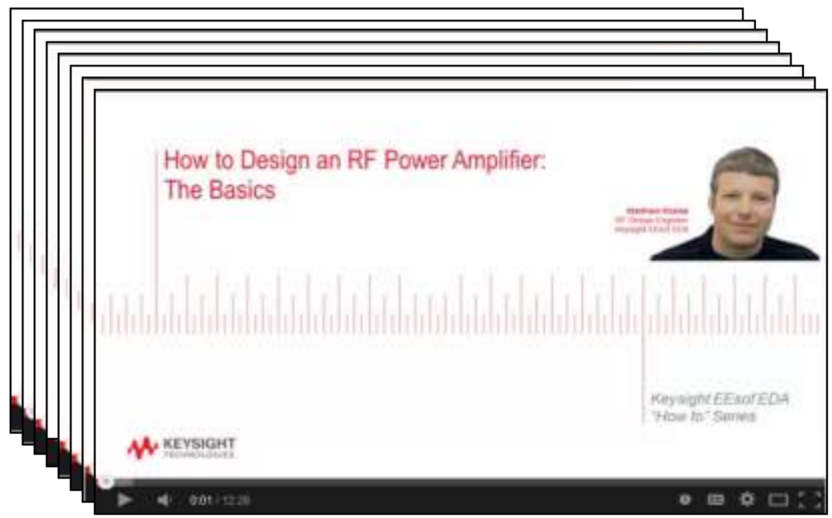

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