N5991HP1A HDMI 2.1 Receiver Compliance Test Automation Software - User Guide

KEYSIGHT

USER GUIDE

Notices

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A CAUTION notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in damage to the product or loss of important data. Do not proceed beyond a CAUTION notice until the indicated conditions are fully understood and met.

WARNING

A WARNING notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in personal injury or death. Do not proceed beyond a WARNING notice until the indicated conditions are fully understood and met.

Contents

5 HDMI Cable Calibrations

6 FRL Waveform Calculation

7 HDMI Receiver Tests for Sinks

Keysight N5991HP1A HDMI 2.1 Receiver Compliance Test Automation Software

User Guide

1 Introduction

KEYSIGHT TECHNOLOGIES

Overview

This guide provides a detailed description of the Keysight N5991 HDMI Test Automation Software Platform.

The BitifEye “ValiFrame” Test Automation software is globally marketed and supported by Keysight Technologies as N5991. This document describes the calibrations and test procedures conducted by N5991 ValiFrame for HDMI in detail.

The N5991 software implements compliance tests according to the requirements of the CTS for HDMI Version 1.4, the CTS for Sink Devices of HDMI Version 2.1, and the Generic CTS for Cat 3 Cables of HDMI Version 2.1. It also offers additional custom characterization tests to provide more details of the DUT behavior beyond the limits of compliance testing.

The ValiFrame HDMI Receiver Tests support automatic control of Keysight Technologies M8195A AWG. It calibrates the stress conditions and controls all test electronic equipment for automated receiver tolerance tests.

NOTE The definitions of the acronyms and abbreviations used throughout this User Guide are given in Chapter 10, Appendix: Acronyms and Abbreviations.

Document History

First Edition (December 2020)

The first edition of this user guide describes the functionality of software version N5991 ValiFrame HDMI_1.0.

Second Edition (January 2021)

The second edition of this user guide describes the functionality of software version N5991 ValiFrame HDMI_1.20 based on the HDMI Base specification.

Third Edition (May 2021)

The third edition of this user guide describes the functionality of software version N5991 ValiFrame HDMI_1.2.4 based on the HDMI Base specification.

Fourth Edition (May 2022)

The fourth edition of this user guide describes the functionality of software version N5991 ValiFrame HDMI_1.2.4 based on the HDMI Specification Version 2.1.

Fifth Edition (December 2023)

The fifth edition of this user guide describes the functionality of software version N5991 ValiFrame HDMI_1.3.0 based on the HDMI Specification Version 2.1 (gCTS Revisions 1.4b and 2.1h).

Support and Troubleshooting

In case of problems when running the software, check the log list at the bottom of the main window. The log file can be viewed by right-clicking within the log list section (see red frame in Figure 1). The log file is temporarily saved at C:\ProgramData\BitifEye\ValiFrameK1\Tmp. Note that all log information will be lost when the N5991 application is terminated unless you save the log file.

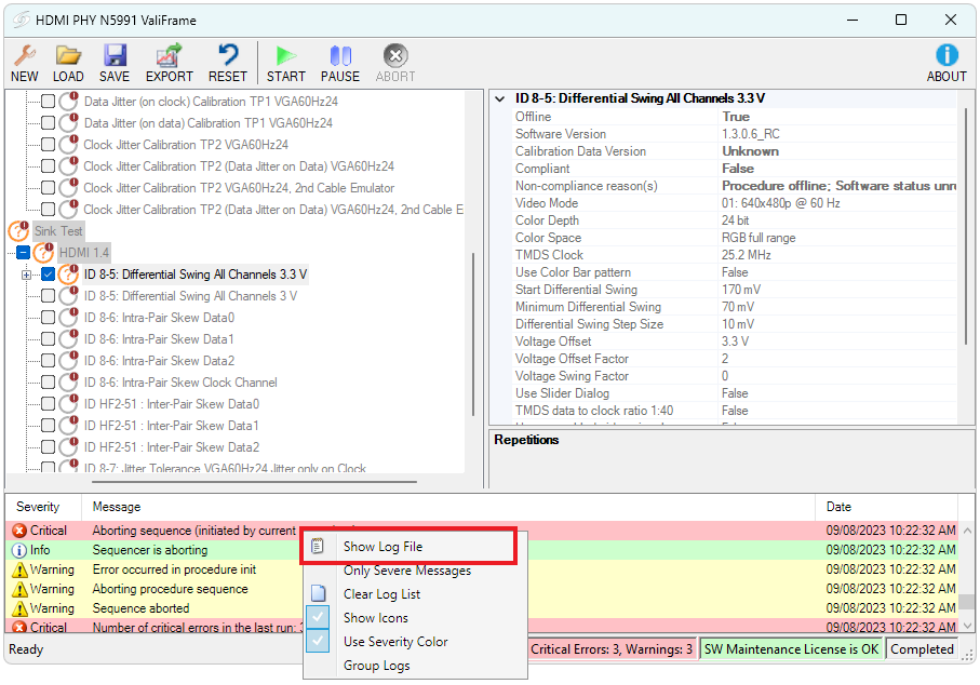


Figure 1 Accessing the log file

If a problem with an application persists, send the log file with the problem to Keysight support.

The Keysight support team is also happy to help you should you require further information about a particular application.

For support options, visit www.keysight.com/find/contactus.

2 ValiFrame HDMI Test Station

The test instruments that are together used for Test Automation are referred to as a Test Station. This chapter describes how to configure and start the N5991 ValiFrame HDMI Test Station.

ValiFrame HDMI Station Configuration

The set of test instruments that are used for HDMI test automation are referred to in the following as the “Test Station” or simply “Station”. The test station is controlled by a suitable PC and the N5991 Test Automation Software Platform.

First install the BitifEye N5991 ValiFrame HDMI software. Further details about this and the licenses required can be found in the N5991 Getting Started Guide.

The ValiFrame HDMI Station Configurator must be started prior to launching ValiFrame. It allows you to select the required set of instruments. Double-click the Station Configurator icon (see Figure 2) to launch the software. Alternatively, to access the Valiframe Station Configuration on a Windows 10-based PC, click

Start > BitifEye HDMI PHY N5991 > HDMI PHY Station Configurator (N5991).

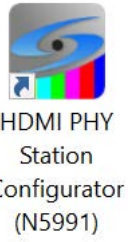


Figure 2 HDMI PHY Station Configurator icon

Test Station Configuration

When the Valiframe HDMI PHY Station Configurator is launched, the first ValiFrame Station Configurator window appears as shown in Figure 3. The station is already selected as HDMI PHY.

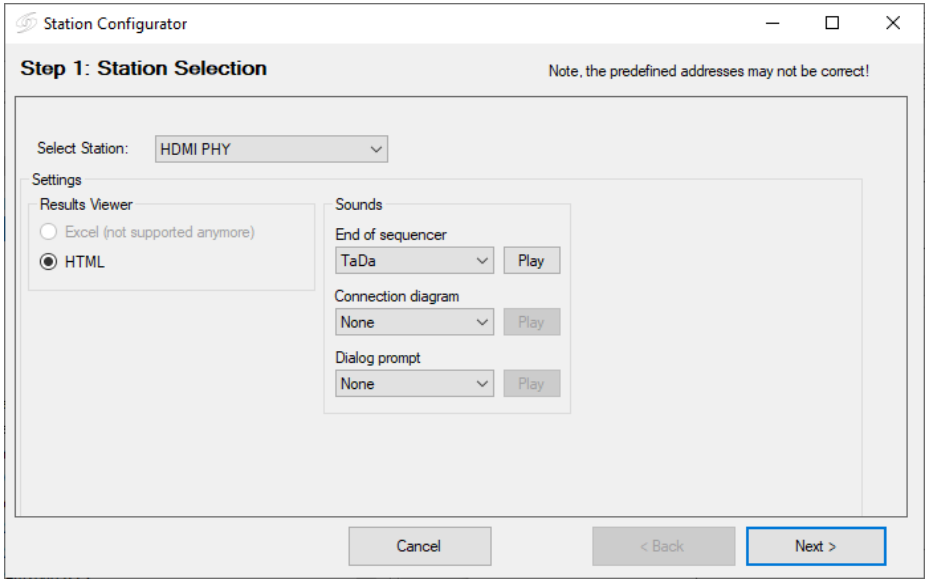


Figure 3 Station Selection window

You may optionally assign sounds to mark different states of the program being reached.

1 **End of sequencer** plays the selected sound at the end of a sequence.

2 **Connection diagram** plays the selected sound every time a connection diagram pops up.

3 **Dialog prompt** plays the selected sound at each dialog prompt.

In each case, select a sound from the drop-down options. 'None' disables the sound for the respective action. Click **Play** to test a sound before assigning it to a specific action.

When you have finished, click **Next** to continue.

The Station Configuration stage of the Station Configurator is displayed in Figure 4. It shows the various options for instruments that can be used for HDMI testing. The options are described here.

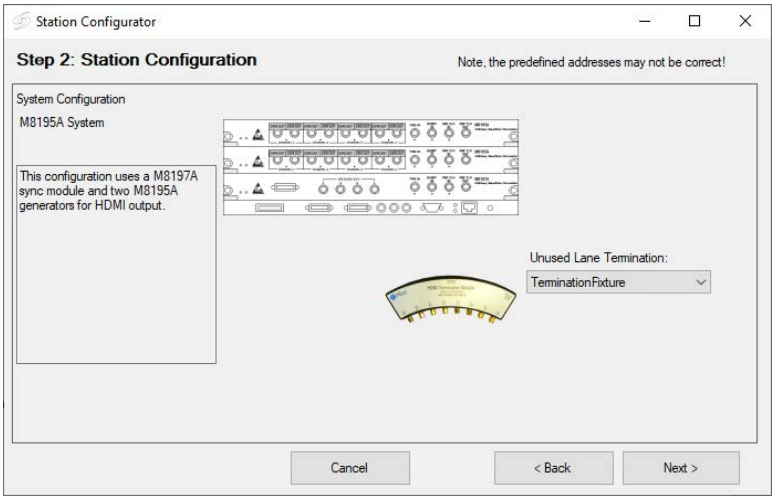


Figure 4 Station Configuration Window

System Configuration

The 'System Configuration' part of the "Station Configuration" stage defines the HDMI signal generator. By default, 'M8195A system' is the signal generator available.

- M8195A System. This configuration uses two M8195A generators for HDMI output and a M8197A synchronization module to de-skew the two M8195A modules.

Unused Lane Termination

Select an option as the method to terminate any unused lanes:

- Termination Fixture. Use a termination fixture.
- Scope Probe. Use a scope probe such as
  - N5444A/N280XA
  - N5380A/B

Test Instrument Configuration

Once the HDMI station is configured, the instrument addresses must be set. An example for instrument configuration is shown in Figure 5.

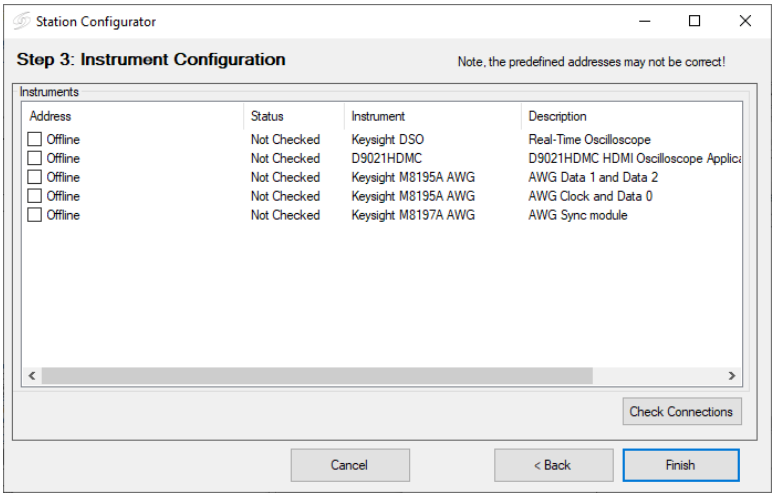


Figure 5 Instrument Configuration Window

NOTE **Make sure that all the selected instruments for the test station are connected to the test station PC controller by remote control interfaces such as LAN or USB.**

After the installation process, all instruments are configured by default in “Offline” mode. In this simulation mode, hardware does not need to be physically connected to the test controller PC. The ValiFrame software cannot connect to any instrument in this mode. In order to control the instruments that are connected to the PC, the instrument address must be entered. The address depends on the bus type used for the connection, for example, LAN or USB.

Most of the instruments used in the HDMI station require a VISA connection. To determine the VISA address, run the “Keysight Connection Expert”, which is part of the Keysight IO Libraries Suite. Either right-click the **Keysight IO Control icon** in the task bar and select the first entry “Connection Expert” or select “Keysight Connection Expert” directly from

the list of programs. For each instrument, copy the address string from the Connection Expert entries and paste it as the instrument address in the ValiFrame Station Configurator.

For further details about how to use the Keysight Connection Expert, see the N5991 Getting Started Guide.

After the address strings have been entered, click **Check Connections** to verify that the connections for the instruments are established properly. If anything is wrong in the instrument address, the Configurator displays a prompt to indicate so.

Click **Finish** to save the changes and close the ValiFrame Station Configurator.

NOTE

When starting a specific test station configuration for the first time, all instruments are set to the “Offline” mode. In this mode the test automation software does not connect to any instrument. This mode can be used for demonstrations or checks only. NO VALID DATA IS PRODUCED.

Starting the HDMI Station

Start the Valiframe HDMI Test Station by double-clicking the **HDMI PHY Valiframe (N5991)** icon on the desktop as shown in Figure 6. Alternatively, for a PC running Windows 10, start the Valiframe HDMI station from **Start / BitifEye HDMI PHY N5991 / HDMI PHY ValiFrame (N5991)**.

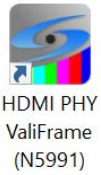


Figure 6 HDMI PHY ValiFrame (N5991) icon

The ValiFrame N5991 connects automatically to the instruments that are set to “Online” mode in the ValiFrame Instrument Configuration (see Figure 5). The application is ready for use once all the connections have been initialized successfully. Clicking the ValiFrame HDMI icon launches the N5991 Test Automation Software Platform window as shown in Figure 7.

The test parameters must be configured before you run any test or calibration procedure. Click **NEW** (red frame in Figure 7) to open the “Configure Product” window (Figure 9).

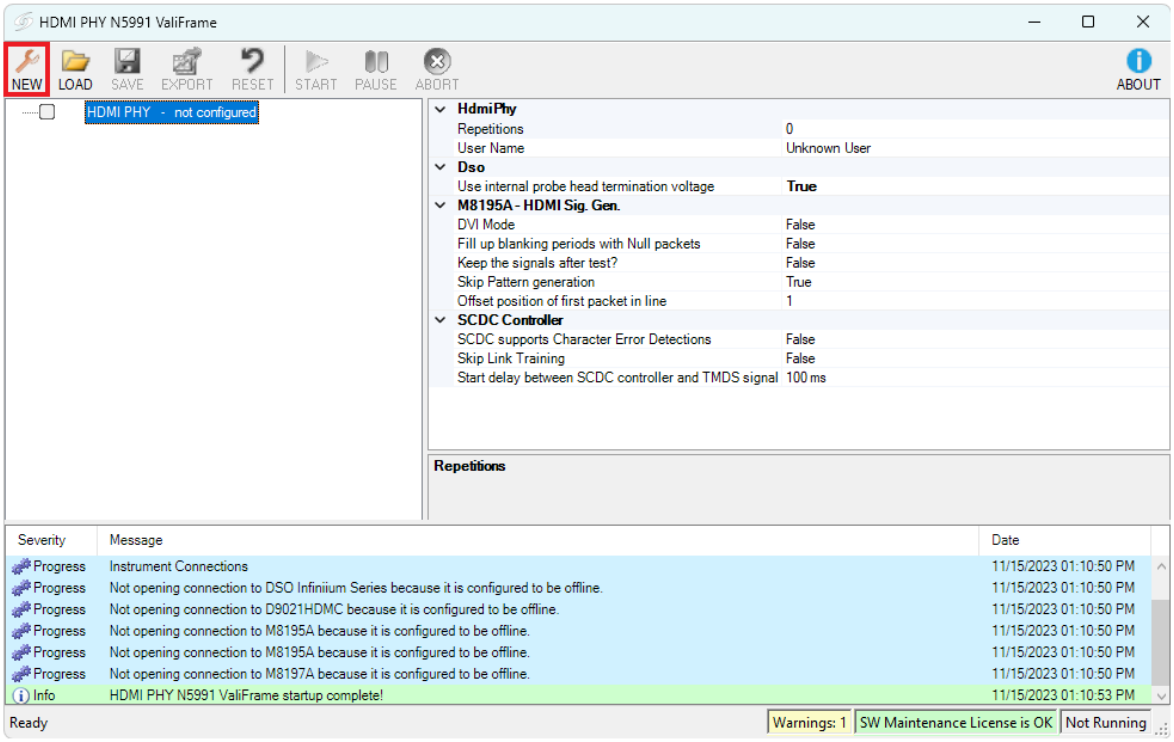


Figure 7 ValiFrame HDMI user interface

FRL IP Auxiliary Files

When you launch the ValiFrame Station for the first time, a dialog prompting for FRL IP Auxiliary files appears (see Figure 8). Note that FRL cable tests are available only if the WCM and PCB loss models are located on the same machine as the ValiFrame software. These files can be added by using the HDMI IP Auxiliary installer (provided by BitifEye) or by downloading them from the HDMI Forum.

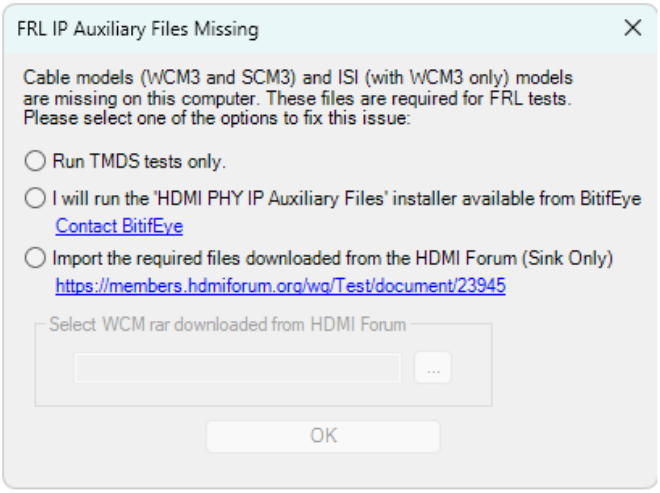


Figure 8 FRL IP Auxiliary dialog

Configuring the DUT

The “Configure Product” window (Figure 9) allows you to select the DUT parameters, such as Product Type and Test Mode (either Compliance Mode or Expert Mode), but also other parameters that are related to the Sink/Cable test configuration. These parameters will be used later in several calibrations and test procedures.

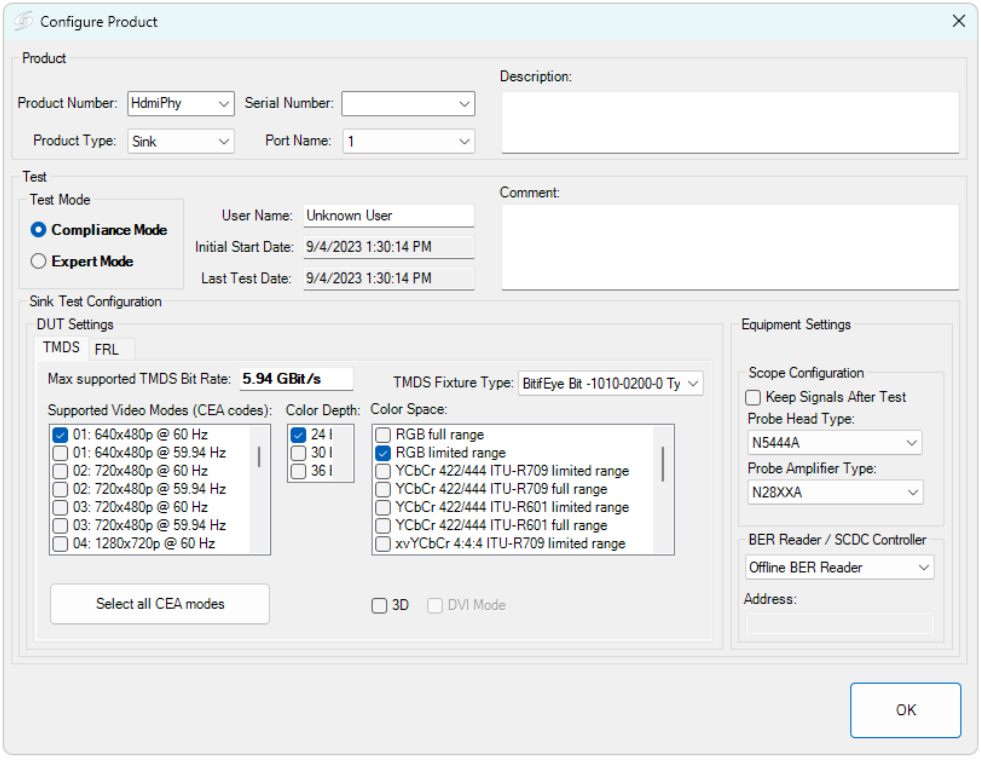


Figure 9 Configure Product panel for product type ‘Sink’

Configuration Parameters

The names and descriptions of parameters that appear in the “Configure Product” window are divided up in the Configure Product panel as follows:

- Product Parameters (Table 1 on page 23)
- Test Parameters (Table 2 on page 24)
  - Test Mode
  - Sink Test Configuration Parameters (for Product Type “Sink”)
    - DUT Settings
      - TMDS (Table 3 on page 25)
      - FRL (Table 4 on page 26)
    - Equipment Settings
      - Scope Configuration
      - BER Reader / SCDC Controller
  - Cable Test Configuration Parameters (for Product Type “Cable”)
    - Cable DUT Settings
    - Equipment Settings
      - Scope Configuration

These parameters are described in more detail in the following sections.

Product Parameters

The product parameters, which give details of the product (DUT), are listed and described in Table 1.

Table 1 Product parameters

Parameter name	Description
Product Number	Name of the product (set as HDMI PHY).
Serial Number	Serial number of the product.
Product Type	The available product types are ‘Sink’ and ‘Cable’. The list of calibrations and tests in the procedure tree will vary according to the type selected.
Port Name	Select a port number between 1 and 10.
Description	Text field to describe the product.

Test Parameters

The test parameters, which give details of the test situation, are considered in the following sections. First, the general parameters are listed and described in Table 2.

Table 2 Test Parameters (general)

Parameter name	Description
User Name	User name text field.
Comment	Text file for user comments.
Initial Start Date	Time stamp of the start of the current session.
Last Test Date	Time stamp of the last test conducted in the current session.
Test Mode	▪ **Compliance Mode**: Tests are conducted as mandated by the CTS. The parameters that are shown in the calibrations and test procedures cannot be modified by the user. ▪ **Expert Mode**: Calibration and tests can be conducted beyond the limits and constraints of the CTS. The parameters that are shown in the calibrations and test procedures can be modified by the user.

Sink Test Configuration Parameters

This section describes the parameters to configure a sink test. An example configuration is shown in the lower half of Figure 9 on page 22.

DUT Settings

The DUT Settings for sink test configuration are further divided into two sections: those for 'TMDS' testing (Table 3) and those for 'FRL' testing (Table 4), which have different "tabs" in the Configure Product panel.

Table 3 Sink Test Configuration Parameters (for TMDS)

TMDS Parameter Name	Description
Max supported TMDS Bit Rate	This parameter enables the test list to be filtered with respect to the maximum TMDS bit rate supported by the DUT. The list of test procedures will only include video mode, color depth and color space combinations with a TMDS bit rate equal to or below the entered value.
TMDS Fixture Type	Select different fixture types for the oscilloscope measurements where the fixture can be de-embedded. The options are: ▪ High Z Probe ▪ Wilder HDMI TPA-P ▪ BitifEye BIT-1010-0200-0 Type A ▪ Other
Supported Video Modes (CEA codes)	Select one or more video modes supported by the DUT.
Color Depth	Select one or more color depth options supported by the DUT.
Color Space	Select one or more pixel-encoding options supported by the DUT.
Select all CEA modes	Selecting this option enables all standard CEA video modes.
3D	Selecting this option adds 3-dimensional video modes to the test procedures.
DVI Mode	Selecting this option enables DVI compatibility. Available only in Expert Mode.

Table 4 Sink Test Configuration Parameters (for FRL)

FRL Parameter name	Description
FRL Test Patterns	Select the pattern used for sink tests.
Max supported FRL Lanes	Select the maximum number of FRL lanes supported by the DUT.
Max supported FRL Rate	This parameter enables the test procedure list to be filtered with respect to the maximum FRL bit rate supported by the DUT.
FRL Fixture Type	Select different fixture types for the oscilloscope measurements where the fixture can be de-embedded. The options are: ▪ BitifEye 2.1 TPA ▪ Wilder 2.1 TPA ▪ Luxshare 2.1 TPA

Equipment Settings

Table 5 gives the Equipment Settings available for sink test configuration.

Table 5 Sink Test Configuration Parameters (Equipment Settings)

Parameter name	Description
Keep Signals After Test	When this option is checked, the software allows you to pause and keep signal outputs active between test procedures so that signals can be checked after a test has been run with the DUT.
Probe Head Type	Select the probe head for the oscilloscope measurements. The options are: ▪ None ▪ N5444A ▪ N5380A/B (only in Expert Mode)
Probe Amplifier Type	Select the amplifier for the oscilloscope measurements. The options are: ▪ N28XXA ▪ N7010A ▪ N7003A
BER Reader / SCDC Controller	This parameter includes a BER Reader to improve test automation. You may also use an HDMI SCDC Controller to set HDMI 2.1 SCDC bits automatically and use the bit error ratio reading capability. ▪ HDMI SCDC Controller/Allion SCDC Controller. Select one of these options if an SCDC Controller should be used for SCDC bits. Optionally, it can be configured to read character errors automatically. The SCDC Controller can be connected directly to the PC running ValiFrame via USB or to a remote PC running the BitifEye Remote Instruments Server. If there is a direct connection, leave the 'Address' field blank. Otherwise you must enter the Host IP address for the BitifEye Remote Instruments Server. ▪ If no BER Reader is available, select the option 'Offline BER Reader'. ValiFrame will then use dialog boxes to guide you through setting SCDC bits and checking for errors during the tests. This option is only available for TMDS tests. If 'Offline BER Reader' is selected, HDMI 2.1 - FRL tests are not available.

Cable Test Configuration Parameters

This section describes the parameters to configure a cable test. An example configuration is shown in the lower half of Figure 10.

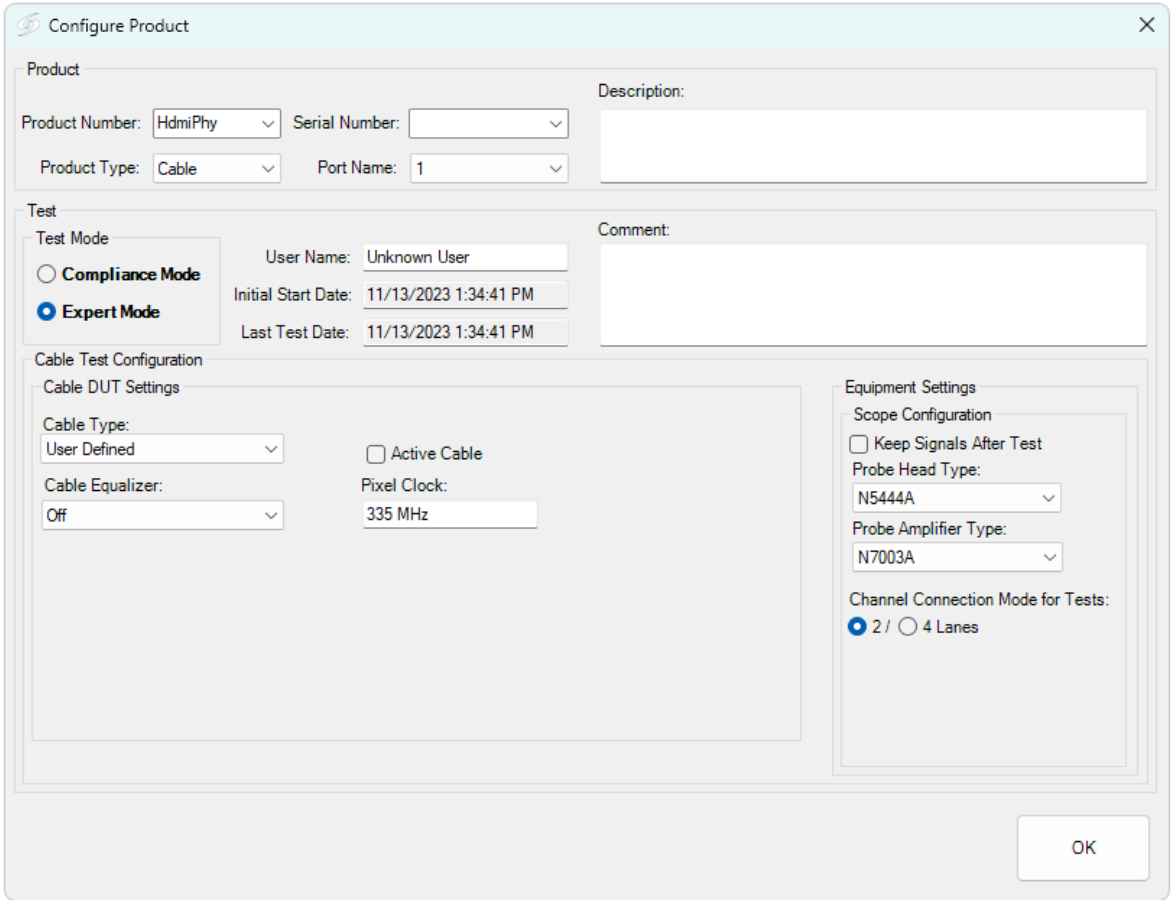


Figure 10 Configure Product panel for product type 'Cable'

NOTE FRL cable tests are available only if the WCM and PCB loss models are located on the same machine as the ValiFrame software. See FRL IP Auxiliary Files on page 21.

Cable DUT Settings

Table 6 describes the cable test configuration parameters found under cable DUT settings.

Table 6 Cable Test Configuration Parameters (Cable DUT Settings)

Parameter name	Description
Cable type	Select the category of the DUT. The options are: ▪ Category 1 (Home) ▪ Category 2 (Home) ▪ Category 3 (FRL) ▪ User Defined
Active cable	Select this check box if the connected DUT is of the 'active cable' type.
Cable Equalizer	Available only for Cable Types 'Category 2 (Home)' and 'User Defined' and only in Expert Mode. Select as ▪ Off ▪ 2 m Cable Equalizer ▪ 5 m Cable Equalizer ▪ 10 m Cable Equalizer
Max. Supported FRL Lanes	Available only for Cable Type 'Category 3 (FRL)' and only in Expert Mode. Select the maximum number of supported data lanes as: ▪ 3 Data Lanes ▪ 4 Data Lanes
Max. Supported FRL Rate	Available only for Cable Type 'Category 3 (FRL)' and only in Expert Mode. Select the maximum supported data rate as: ▪ 3 Gb/s ▪ 6 Gb/s ▪ 8 Gb/s ▪ 10 Gb/s ▪ 12 Gb/s
FRL Fixture Type	Available only for Cable Type 'Category 3 (FRL)'. Select the fixture type: ▪ BitifEye 2.1 TPA ▪ Wilder 2.1 TPA ▪ Luxshare 2.1 TPA ▪ (Only for User Defined type): Set the pixel clock rate of the cable here.
Pixel Clock	Available only for Cable Type 'User Defined', which is only available in Expert Mode. Set the pixel clock rate of the cable here.

Equipment Settings

The Equipment Settings available for cable test configuration are described in Table 7.

Table 7 Cable Test Configuration Parameters (Equipment Settings)

Parameter name	Description
Keep Signals After Test	When this option is checked, the software allows you to pause and keep signal outputs active between test procedures so that signals can be checked after a test has been run with the DUT.
Probe Head Type	Select different probe heads for the oscilloscope measurements. The options are: ▪ None ▪ N5444A ▪ N5380A/B (only in Expert Mode)
Probe Amplifier Type	Select different probe amplifiers for the oscilloscope measurements. The options are: ▪ N28XXA ▪ N7010A ▪ N7003A
Channel Connection Mode for Test	This parameter allows you to select the number of connections required for oscilloscope measurements. The available choices depend on the oscilloscope and may include ▪ 2 Lanes ▪ 4 Lanes If the accessories for a 4-connection setup are available and the generator does not have any limitations, the 4-connection setup should be chosen as this has the advantage that most of the tests can be run without altering the setup.

3 Using the Software

This chapter describes how to select the calibrations and test procedures that are to be run and how you can modify the parameters in expert mode – if required – to go beyond the tests specified by the CTS.

Introduction

Once the DUT has been configured, click ‘OK’ in the “Configure Product” panel. All calibration and test procedures are included in the respective groups in a manner similar to how they are organized in the specifications.

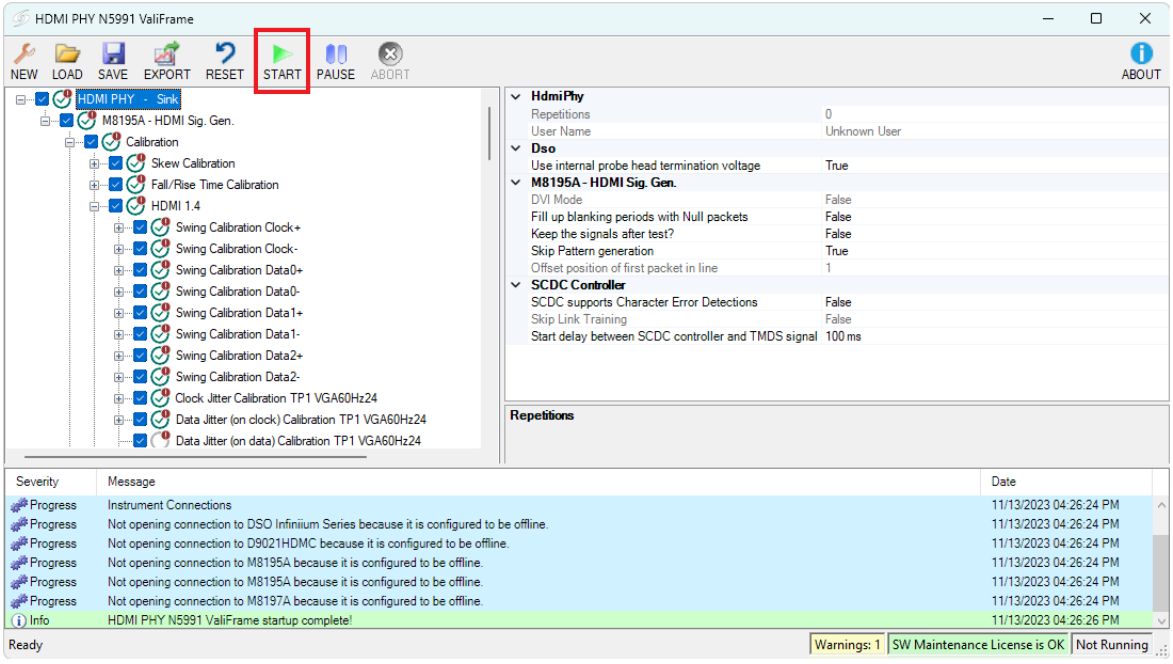


Figure 11 HDMI main window

The **parameter grid** on the right side of the window shows the parameters that are related to the individual procedure or group of procedures selected on the left.

The **log list** in the bottom pane of the window shows calibration and test status messages (regular progress updates as well as warnings and error messages).

The **status bar** at the very bottom provides information about how many critical errors have occurred, how many warnings have been sent, the status of the software maintenance license and whether ValiFrame is running.

To start one or more procedures, select the corresponding check box(es). Then the 'Start' button is enabled and turns green (outlined in red in Figure 11). Click Start to run the selected procedure(s).

Once all the procedures have been run, the N5991 configuration can be stored as a single '.vfp' file using the 'Save' button and recalled using the 'Load' button without the need to configure the DUT again.

CAUTION

Before executing the calibration or test procedures, ensure that the HDMI Station Configuration is conducted properly with all necessary instruments, such as the Infiniium oscilloscope, set to "online". All calibrations can be run in offline mode, that is, without any instrument connected. The offline mode is intended for product demonstrations with simulated data. CALIBRATIONS RUN IN OFFLINE MODE DO NOT GENERATE VALID CALIBRATION DATA.

NOTE

If you have already performed calibrations and tests, when you update ValiFrame and open it, you may see several log messages saying that the measurements are not compliant. This is because ValiFrame now records the exact setup and software version used for the calibrations and, even if your setup has not changed, the information required by ValiFrame to categorize the results as compliant is not available. Compliance information is also available in the result report of each procedure.

Selecting, Modifying, and Running Tests

Selecting Procedures

The calibration and receiver test procedure groups can be selected globally by clicking the check box at the top of the group. Alternatively, an individual test procedure can be selected by checking the corresponding check box. Click 'Start' to run the selected test procedures.

NOTE

Procedures available only in Expert Mode, that is, those that are not required for compliance, are listed in the procedure tree in a separate group "Expert Mode" after the groups HDMI 1.4, HDMI 2.1 – TMDS and HDMI 2.1 - FRL for sink DUTs and after the groups Cable Tests – Data and Cable Tests – Clock for cable DUTs (categories 1 and 2).

Modifying Parameters

Most calibration and test procedures as well as the groups containing them have parameters that control the details of how the procedures are run. In compliance mode, most of these parameters are read-only. In expert mode, almost all the parameters can be modified. First, select a specific calibration or test procedure or one of the groups contained in the N5991 procedure tree as shown in Figure 12. The parameters are displayed in a property list (parameter grid) on the right side of the window. These parameters can be configured only before the selected procedure subgroup or procedure is started. All of the selected test parameters are listed in the test results.

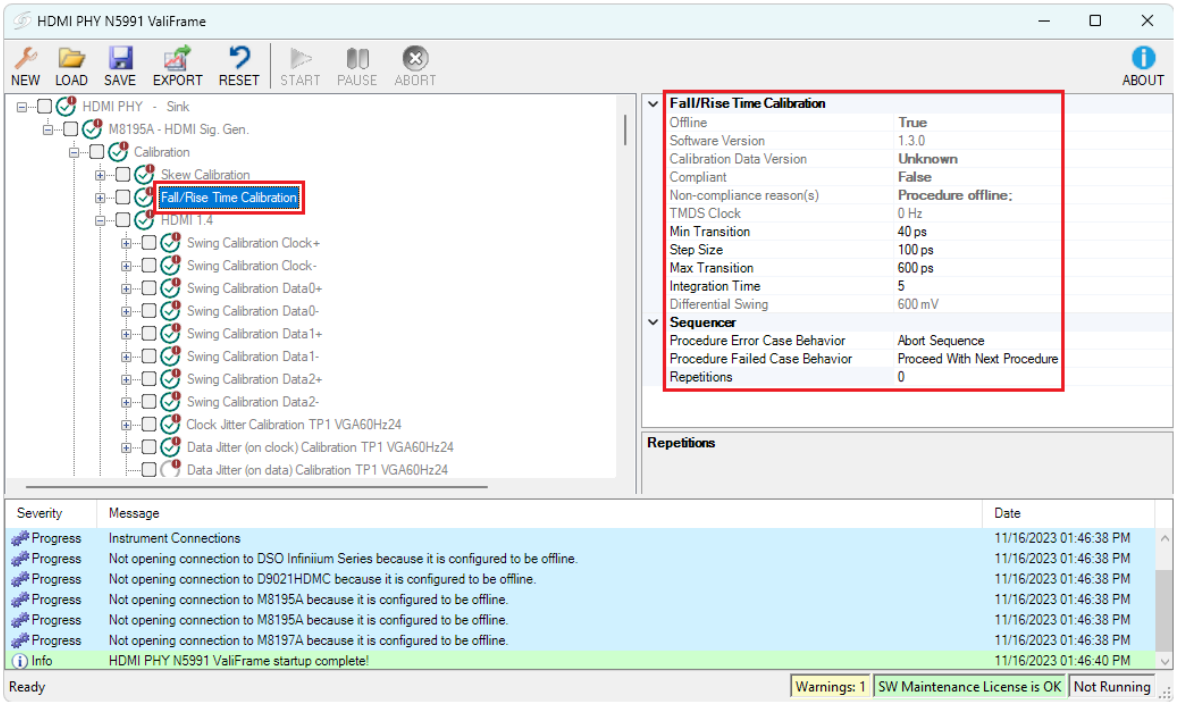


Figure 12 Modifying parameters in the HDMI PHY N5991 ValiFrame main window

Running Procedures

To run the selected procedure, click the **Start** button on the toolbar (see Figure 12). The procedures are run sequentially in the order shown in the procedure selection tree. Some procedures may require user intervention, such as changing cable connections or entering DUT parameters. The required action is prompted in pop-up dialog boxes before the calibration/test procedures are run.

To view the connection diagram, right-click the desired test or calibration. From the right-click menu, select “Show Connection...”.

The status of each procedure is indicated by the round icon next to its name in the procedure tree. For more details about the meanings of the icons, see the N5991 Getting Started Guide, which can be downloaded from the BitifEye homepage.

Required Calibration Data

Some of the calibration procedures and most of the test procedures require calibration data that has been measured previously. You can see the calibration data required by a particular procedure by right clicking its name in the procedure tree and selecting 'Required Calibrations'. A list of the prerequisite calibrations drops down (Figure 13).

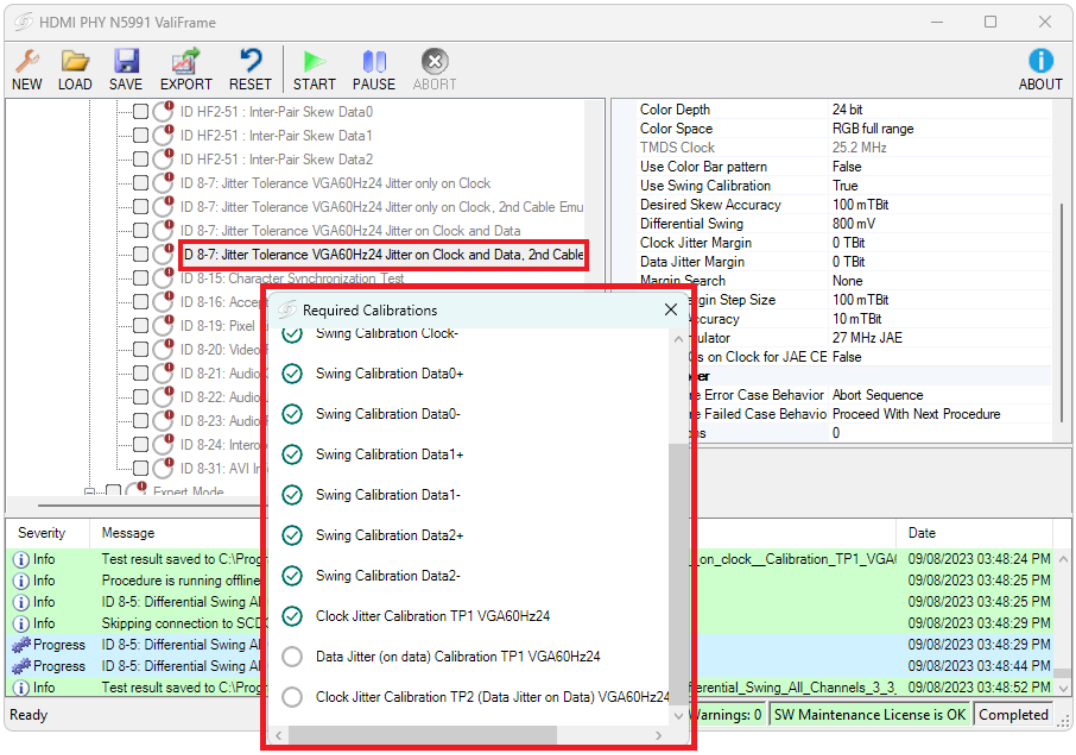


Figure 13 Example list of required calibrations

The icon next to the name of a calibration procedure in the list indicates whether the calibration has been run successfully (green), is incomplete (yellow), failed (red) or has not yet been run (gray).

Results

Run-Time Data Display

Most procedures generate data output. While the procedure is running, the data is displayed in a results window, which opens automatically for each individual procedure.

Any results windows that are open during the procedure runs are closed automatically once the specific procedure is finished. As long as the N5991 Software is running, each result file can be reopened by double-clicking the respective procedure. However, the individual files are lost when the N5991 main window is closed, unless you save the individual files or a collection of them.

Exporting Results

For your convenience, all individual results are summarized in an HTML document at the end of the test run (see Figure 14 on page 38). All calibration and test data worksheets can be saved in a workbook by clicking the **Export** button on the toolbar of the HDMI PHY N5991 ValiFrame main window. Keysight recommends performing this action at least at the end of each HDMI PHY N5991 ValiFrame procedure run to avoid any data loss. If the calibration and test procedures are conducted several times during the same HDMI PHY N5991 ValiFrame run, the resulting worksheets are combined in a workbook. If a test procedure is conducted without prior execution of calibration procedures in the same test run, only the test results will be saved to the workbook.

NOTE

As a safety feature, all calibration and test results are saved by default to the N5991 “Tmp” directory (C:\ProgramData\BitifEye\ValiframeK1\Tmp). The sub-folder “Results\HdmiPhy Station” contains the HTML files of the final results measured at each calibration and test procedure.

In addition to the calibration data HTML files, calibration data files are generated. These files are saved by default to the N5991 calibrations folder ‘C:\ ProgramData\BitifEye\ValiframeK1\HdmiPhy\Calibrations’. If these calibrations are run again, the data file is overwritten. To save the calibration data files at each configuration, the files must be copied from this folder and saved manually in a different folder before the calibrations are rerun.

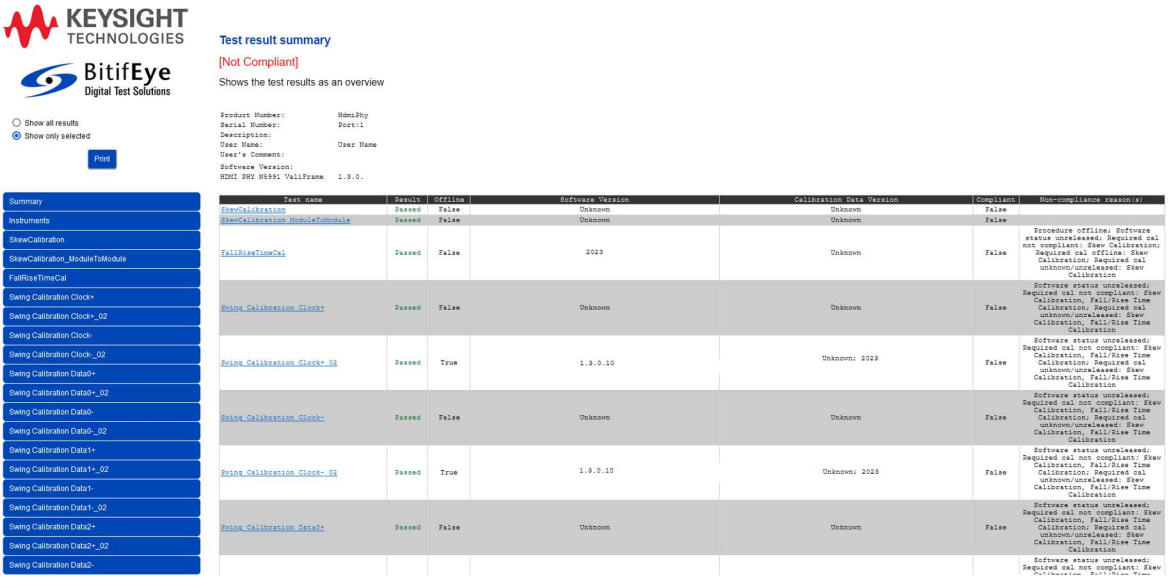


Figure 14 Example summary page (just the top) of an HDMI PHY N5991 ValiFrame workbook

HDMI Parameters

The HDMI parameters are of three types:

- Sequencer Parameters
- Common Parameters
- Procedure Parameters

Sequencer Parameters

The sequencer parameters control the flow of the test sequencer only, not the behavior of individual procedures. One of them, Repetitions, is available for all procedures and groups in the procedure tree. The others are only available for procedures. Like all other parameters, the sequencer parameters are shown in the right half of the ValiFrame user interface and you may manually change them, as illustrated in Figure 15.

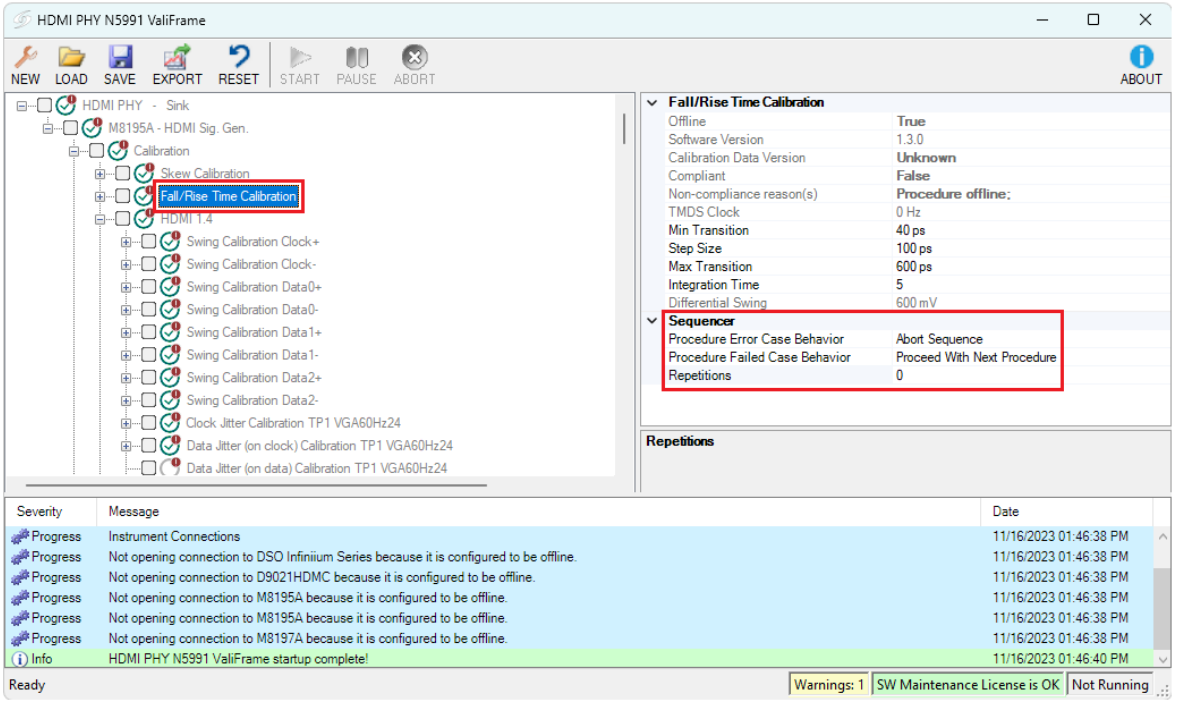


Figure 15 HDMI sequencer parameters

All sequencer parameters are listed in alphabetical order in Table 8 on page 239.

Common Parameters

The common parameters are used for several related calibration or test procedures. They are shown on the right side of the ValiFrame user interface when the selected entry of the procedure tree on the left is a group instead of an individual procedure.

The HDMI Receiver Test Software has some group parameters (in addition to “Repetitions”) on the top-level entry of the HDMI procedure tree. These are common for all Valiframe HDMI PHY calibration and receiver test procedures.

All of the common parameters are listed in Table 9 on page 240 in the order they appear in the user interface.

Procedure Parameters

The Procedure Parameters are all such parameters that are not part of any of the previously described categories. They are shown on the right side of the ValiFrame user interface when the selected entry of the procedure tree on the left is an individual procedure. Their purpose is to modify the behavior of that single procedure. Procedures often have parameters with the same name, but pre-configured settings always apply to the selected procedure, while their meaning may be slightly different.

The procedure parameters are listed alphabetically in

- Table 10 on page 241 (parameters used in all procedures)
- Table 11 on page 242 (parameters for sink calibrations)
- Table 12 on page 246 (parameters for cable calibrations)
- Table 13 on page 250 (parameters for sink tests)
- Table 14 on page 259 (parameters for cable tests)

4 HDMI Sink Calibrations

Before any sink or cable test procedure can be run, the HDMI PHY test system must be calibrated. The procedures used for a sink DUT are described in this chapter.

Overview

The purpose of the calibration procedures is to calibrate the TDMS and FRL signal generator levels and timings.

ValiFrame automatically determines the required calibration procedures according to the parameters set in the Configure Product dialog, including

- Product Type (sink or cable)
- Test Mode (compliance or expert)
- TMDS or FRL
- Supported Video Modes
- Color Depth
- Color Space
- Cable Type

The results of each calibration are stored in the 'Calibration' folder of ValiFrame, so that they can be used for another calibration or test, as required.

The order of the procedures in the procedure tree is driven mainly by the calibration dependencies.

For calibrations, in general, the following calibrations are prerequisite:

- The appropriate skew calibration.
- All the calibrations listed above it in the same branch of the procedure tree.

They are not listed explicitly for each calibration in this User Guide. However, they can be found directly in the application (see Required Calibration Data on page 36 of this User Guide).

Note that ValiFrame attempts to reduce the calibration effort by coalescing similar data rates into one calibration, when no significant deviation in the results is expected.

DC and single-ended levels are always determined with respect to the termination voltage.

Calibrations for Both Sinks and Cables

Skew Calibration

Purpose and Method

This calibration is used to de-skew the setup. Because of the differences in length between Clock, Data0, Data1 and Data2, the output signals are not aligned on the same base. Additionally, this calibration performs the module alignment of the two M8195A modules using the M8197A synchronization module.

The length differences are measured in several steps and finally saved in a calibration table. With additional steps, the software measures the module-to-module skew for specific sample frequencies and saves this in a calibration table as well. For each test, this data table is used to de-skew the signals.

Connection Diagram

During the test, the software prompts you to change the outputs connected to the oscilloscope. Initially, M8195A module 1 outputs (Clock and Data0) must be connected. Thereafter, these must be replaced with M8195A module 2 outputs (Data1 and Data2). Finally, to calibrate the module-to-module skew, you must connect both modules 1 and 2 to the oscilloscope. See Figure 16, Figure 17 and Figure 18.

Figure 16 Example connection diagram for Sink Skew Calibration (connection 1)

Figure 17 Example connection diagram for Sink Skew Calibration (connection 2)

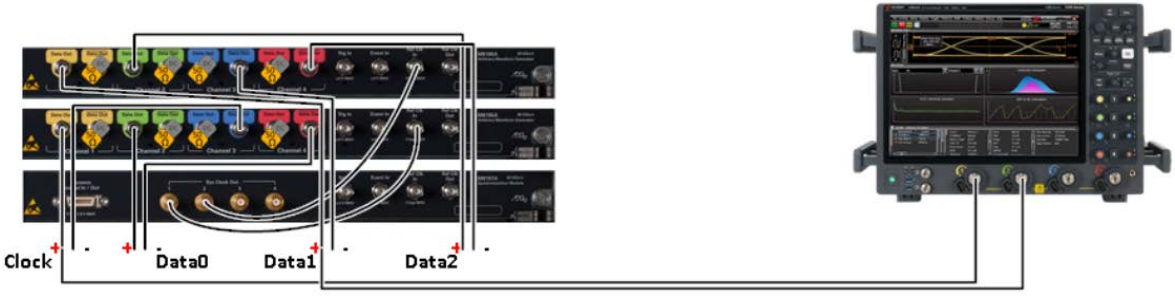


Figure 18 Example connection diagram for Sink Skew Calibration (connection 3)

Result Description

The example result in Figure 19 shows the calibration data used to de-skew the setup.

The second page of results gives the module-to-module skew for various frequencies set on the AWG (Figure 20).

Skew Calibration

[Not Compliant]

Skew Calibration

----General----	
Offline	True
Software Version	1.3.0
Compliant	False
Non-compliance reason(s)	Procedure offline; Software status unre
Step size of sample frequency	250 MHz
User Name	Unknown User
----M8195A - HDMI Sig. Gen.----	
DVI Mode	False
Fill up blanking periods with Null packets	False
Keep the signals after test?	False
Skip Pattern generation	True
----SCDC Controller----	
SCDC supports Character Error Detections	False
Skip Link Training	False
Start delay between SCDC controller and TMDS signal	100 ms
----Dso----	
Use internal probe head termination voltage	True

Result	Identifier	Skew Value [ns]
pass	AWG1.CH1+ to AWG1.Ch2+	0.002
pass	AWG1.CH1+ to AWG1.Ch3-	0.003
pass	AWG1.CH1+ to AWG1.Ch4-	0.002
pass	AWG2.CH1+ to AWG2.Ch2+	0.003
pass	AWG2.CH1+ to AWG2.Ch3-	0.004
pass	AWG2.CH1+ to AWG2.Ch4-	0.005

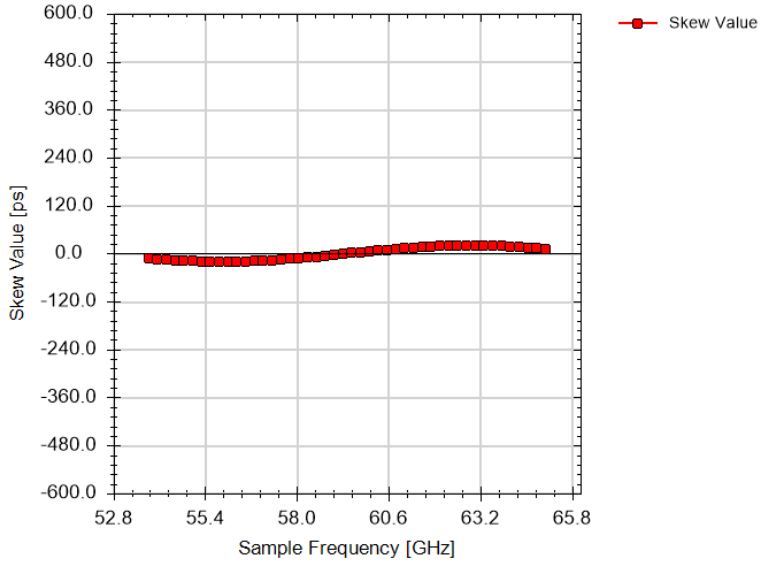
Figure 19 Example result for Skew Calibration

- Result: (Pass/Fail) Test is considered as passed if the measured skew is below the maximum limits.
- Identifier: The skew is measured between these M8195A outputs.
- Skew Value [ns]: Measured skew value for each output

SkewCalibration_ModuleToModule

[Not Compliant]

Calibrates the module to module skew



----General----	
Offline	True
Software Version	1.3.0
Compliant	False
Non-compliance reason(s)	Procedure offline; Software st
Step size of sample frequency	250 MHz
User Name	Unknown User
----M8195A - HDMI Sig. Gen.----	
DVI Mode	False
Fill up blanking periods with Null packets	False
Keep the signals after test?	False
Skip Pattern generation	True
----SCDC Controller----	
SCDC supports Character Error Detections	False
Skip Link Training	False
Start delay between SCDC controller and TMDS signal	100 ms
----Dso----	
Use internal probe head termination voltage	True

Result	Sample Frequency [GHz]	Skew Value [ps]
pass	53.760	-12.0
pass	54.010	-13.7
pass	54.260	-15.2
pass	54.510	-16.6
pass	54.760	-17.7
pass	55.010	-18.6
pass	55.260	-19.3
pass	55.510	-19.8
pass	55.760	-20.0
pass	56.010	-19.9
pass	56.260	-19.7
pass	56.510	-19.1
pass	56.760	-18.4
pass	57.010	-17.4
pass	57.260	-16.2
pass	57.510	-14.8
pass	57.760	-13.2
pass	58.010	-11.4
pass	58.260	-9.6
pass	58.510	-7.5
pass	58.760	-5.4

Figure 20 Example result for Skew Calibration (module-to-module). Just the top of the table

- Result: (Pass/Fail) Test is considered as passed if the measured skew is below the maximum limits.
- Sample Frequency: The M8195A sample frequency that has been set.
- Skew Value: Measured skew value between the M8195A modules for each sample frequency.

Fall/Rise Time Calibration

Purpose and Method

Transition times can be created on an M8195A by manipulating waveforms instead of using hardware TTCs. Test fixtures and cables affect the transition times. To compensate for this, the fall and rise times are calibrated by generating a clock signal and measuring the rise time with a DSO.

For the calibration, a valid clock signal of the lowest video mode is generated with different transition times. For each step, the DSO measures the rise time of the signal and averages the measured transition time over multiple measurements.

Connection Diagram

See Figure 21.

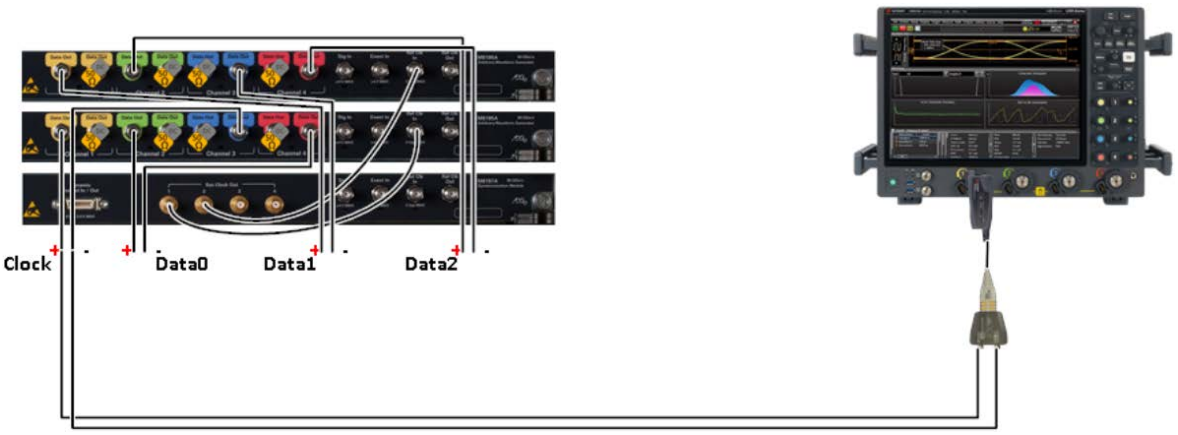


Figure 21 Example connection diagram for Fall/Rise Time Calibration – M8195A setup

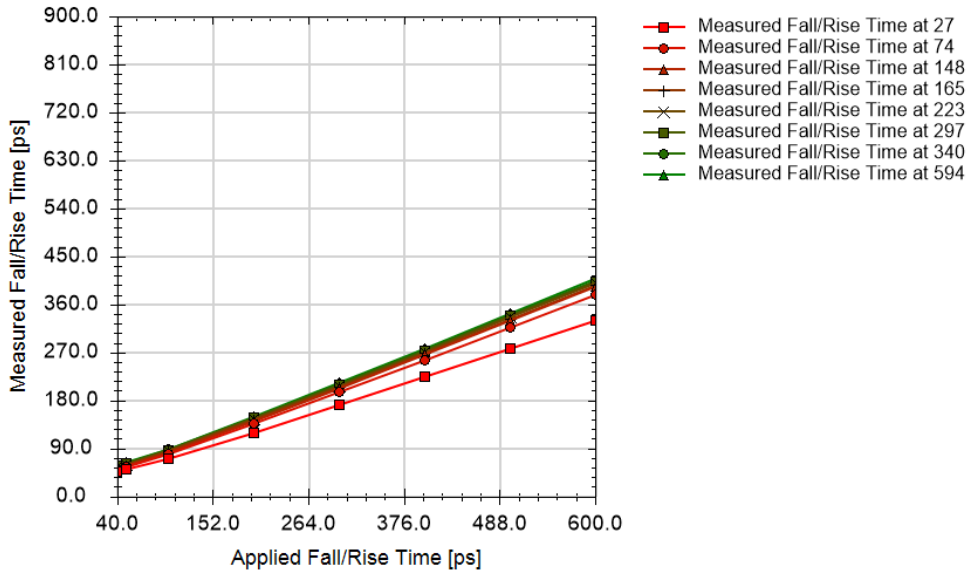
NOTE This connection diagram is specifically for the N5444A/N28XXA probe head. If a different probe head is selected in the Configure DUT dialog, the connection diagram will be slightly different.

Result Description

FallRiseTimeCal

[Not Compliant]

Calibrates the transition time



----General----	
Offline	True
Software Version	1.3.0.9_RC
Calibration Data Version	Unknown
Compliant	False
Non-compliance reason(s)	Procedure offline; Software status unreleased; Required cal not compliant: Skew Calibration; Required cal offline: Skew Calibration; Required cal unknown/unreleased: Skew Calibration
Video Mode	64: 1920x1080p @ 100 Hz
Color Depth	24 bit
Color Space	RGB full range
Use Color Bar pattern	False
Min Transition	40 ps
Step Size	100 ps
Max Transition	600 ps
Integration Time	5
User Name	Unknown User
----M8195A - HDMI Sig. Gen.----	
DVI Mode	False
Fill up blanking periods with Null packets	False
Keep the signals after test?	False
Skip Pattern generation	True

```
----SCDC Controller----
SCDC supports Character Error Detections              False
Skip Link Training                                    False
Start delay between SCDC controller and TMDS signal   100 ms
----Dso----
Use internal probe head termination voltage           True
```

Set Fall/Rise Time [ps]	Measured Fall/Rise Time at 27 [ps]	Measured Fall/Rise Time at 74 [ps]	Measured Fall/Rise Time at 148 [ps]	Measured Fall/Rise Time at 165 [ps]	Measured Fall/Rise Time at 223 [ps]	Measured Fall/Rise Time at 297 [ps]	Measured Fall/Rise Time at 340 [ps]	Measured Fall/Rise Time at 594 [ps]
600.0	331	379	393	396	400	403	405	408
500.0	277	317	330	332	335	338	340	343
400.0	224	256	266	268	271	274	275	278
300.0	171	195	203	205	207	209	211	213
200.0	119	136	141	143	145	146	148	150
100.0	70	79	82	84	85	87	88	89
50.0	50	55	57	58	59	61	62	63
40.0	47	51	53	54	55	56	57	58

Figure 22 Example result for Fall/Rise Time Calibration

- Result: (Pass/Fail) Test is considered as passed if transition times are calibrated successfully.
- Set Fall/Rise Time [ps]: The applied transition time for this step.
- Measured Fall/Rise Time at xx MHz [ps]: Measured transition time for this step at a specific data rate.

Sink Calibrations – HDMI 1.4

Swing Calibration

Availability

- HDMI 1.4
- Clock+, Clock-, Data0+, Data0-, Data1+, Data1-, Data2+, Data2-

Purpose and Method

The test fixtures and cables attenuate the data or clock signals. To compensate for this, the differential signal levels are calibrated by connecting an HDMI fixture to the HDMI setup and measuring the differential swing with a DSO.

For the calibration, a software PRBS signal is generated at different swing voltage levels. For each step, the DSO measures the histogram to find the most frequently attained value of the differential swing. This calibration is done for each channel of the signal generator

Connection Diagram

Figure 23 shows the connection diagram for the Swing Clock+ calibration. The differential probe head must be connected to the TPA-R output of the specific channel to be calibrated.

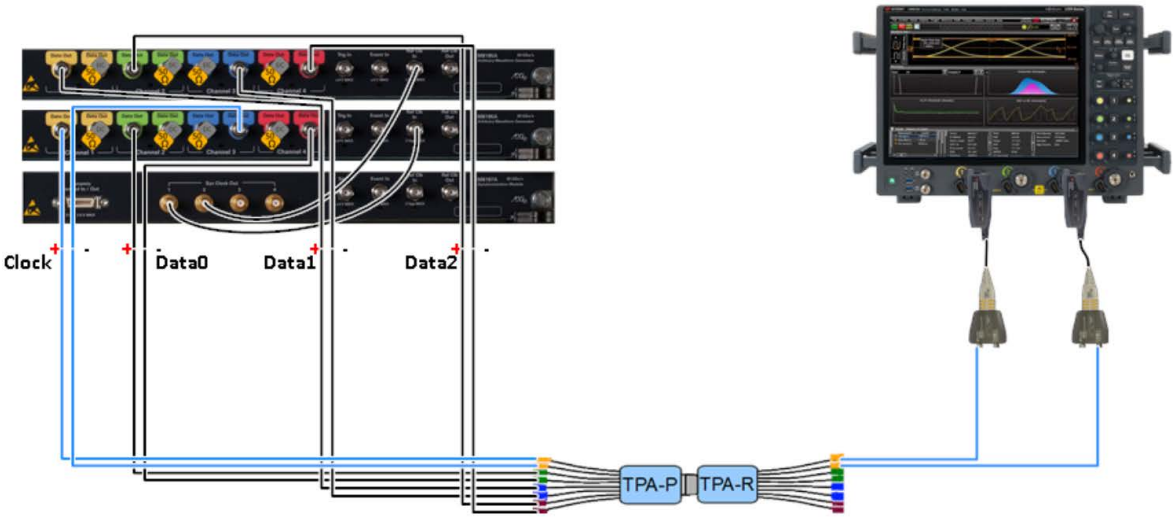


Figure 23 Example connection diagram for Sink Swing Calibration – M8195A setup

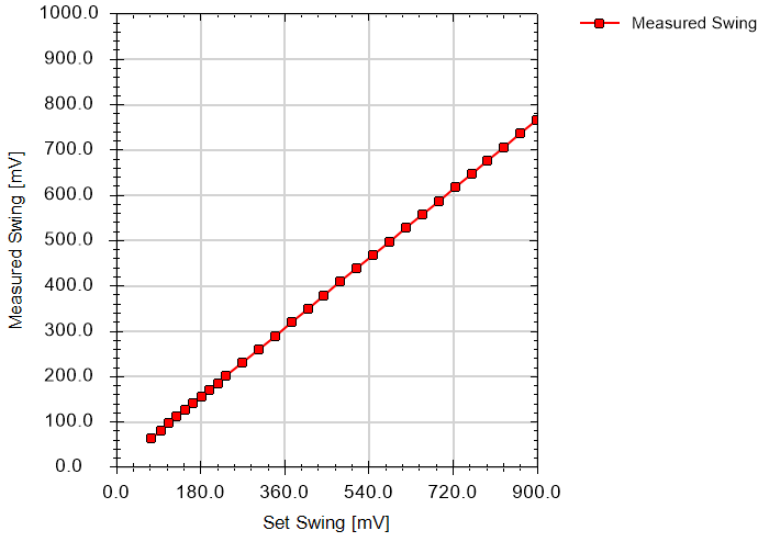
NOTE This connection diagram is specifically for the N5444A/N28XXA probe head. If a different probe head is selected in the Configure DUT dialog, the connection diagram will be slightly different.

Result Description

Ck+ 64: 1920x1080p @ 100 Hz

[Not Compliant]

Calibrates the Generator Swing



----General----	
Offline	True
Software Version	1.3.0
Calibration Data Version	Unknown; '1.3.0
Compliant	False
Non-compliance reason(s)	Procedure offline; Software st Calibration, Fall/Rise Time Ca Time Calibration; Required cal Calibration
Video Mode	64: 1920x1080p @ 100 Hz
Color Depth	24 bit
Color Space	RGB full range
Min Swing Value	35 mV
Max Swing Value	900 mV
Step Size	35 mV
DSO Channel used for Calibration	CHANnel1
DSO Channel used for Termination	CHANnel3
User Name	Unknown User
----M8195A - HDMI Sig. Gen.----	
DVI Mode	False
Fill up blanking periods with Null packets	False
Keep the signals after test?	False
Skip Pattern generation	True

```
----SCDC Controller----
SCDC supports Character Error Detections              False
Skip Link Training                                    False
Start delay between SCDC controller and TMDS signal   100 ms
----Dso----
Use internal probe head termination voltage           True
```

Result	Set Swing [mV]	Measured Swing [mV]
pass	900	765
pass	865	735
pass	830	706
pass	795	676
pass	760	646
pass	725	616
pass	690	587
pass	655	557
pass	620	527
pass	585	497
pass	550	468
pass	515	438
pass	480	408
pass	445	378
pass	410	349
pass	375	319
pass	340	289
pass	305	259
pass	270	230
pass	235	200
pass	217	185
pass	200	170
pass	182	155
pass	165	140
pass	147	125
pass	130	110
pass	112	96
pass	95	81
pass	75	64

Figure 24 Example result for Swing Calibration Clock+

- Result: (Pass/Fail) Test is considered as passed if the calibration step succeeds.
- Set Swing: The applied differential swing voltage for this step.
- Measured Swing: The measured differential swing voltage for this step.

Clock Jitter Calibration

Purpose and Method

This procedure calibrates the clock jitter amplitude by measuring jitter with a DSO.

The calibration is divided into several parts:

- Clock Jitter Calibration TP1
- Clock Jitter Calibration TP2
- Clock Jitter Calibration TP2 (Data Jitter on Data)
- Clock Jitter Calibration TP2, 2nd Cable Emulator
- Clock Jitter Calibration TP2 (Data Jitter on Data), 2nd Cable Emulator

NOTE **The various parts of the calibration listed above may not be direct neighbors in the procedure tree. Data Jitter may be calibrated in between.**

Clock jitter is sinusoidal jitter injected into the HDMI Clock signal. Four different sinusoidal jitter frequencies are calibrated: 500 kHz, 1 MHz, 7 MHz and 10 MHz.

For this calibration, a valid HDMI video signal is generated at different frequencies and amplitudes. The jitter is calculated from the signal waveform. For each step, the histogram peak-to-peak width of the jitter is measured by the oscilloscope.

Since the data rate directly affects the jitter, this calibration must be conducted for each required data rate.

For the test point TP2, the signal is modified by including cable emulators. The cable emulator is included in the waveform calculation. This is accomplished by applying the reference S-parameter characteristics of the specific cable emulator to the signal waveform generated by the M8195A. The cable emulators are dependent on the applied data rate and as required in the HDMI CTS.

Connection Diagram

Refer to Figure 25.

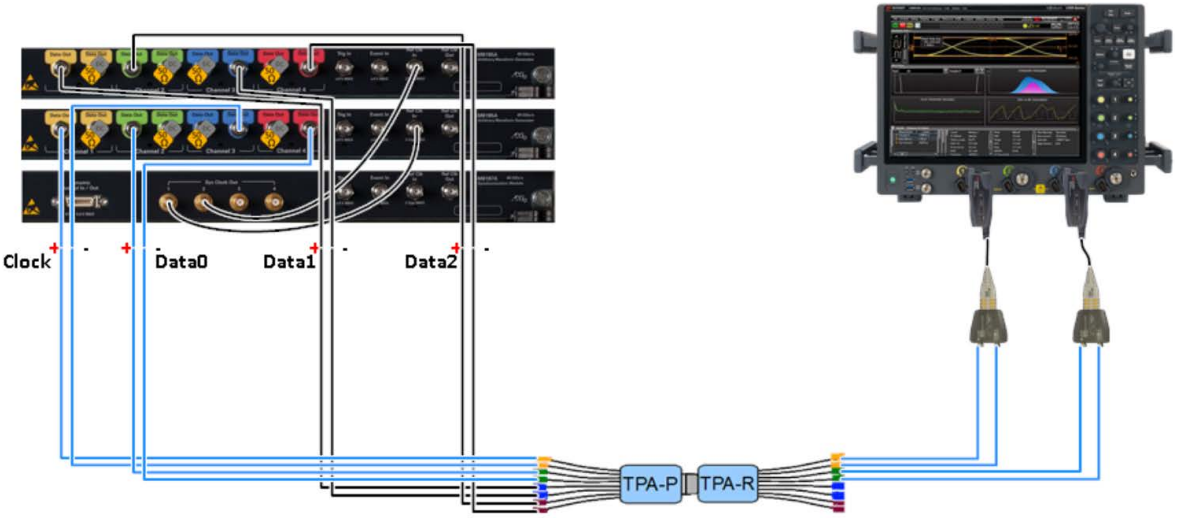


Figure 25 Example connection diagram for Sink Jitter Calibration

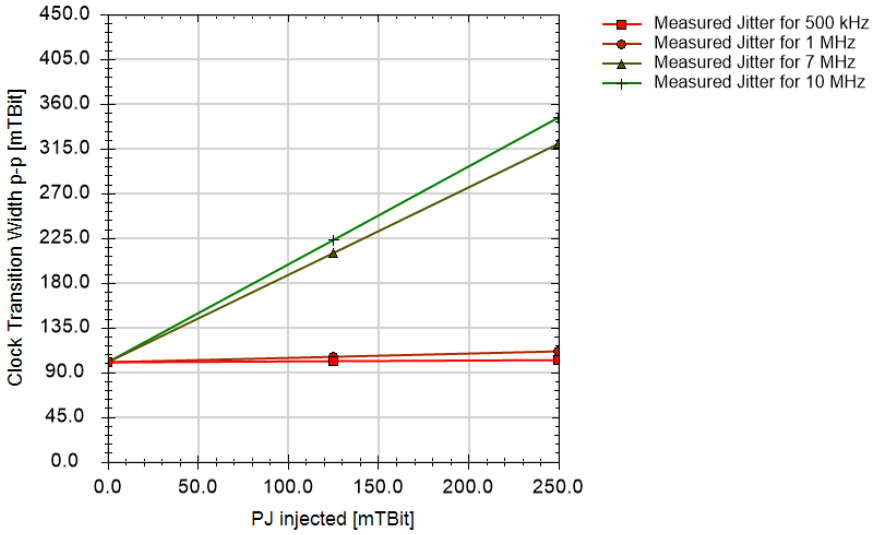
NOTE This connection diagram is specifically for the N5444A/N28XXA probe head. If a different probe head is selected in the Configure DUT dialog, the connection diagram will be slightly different.

Result Description

ClkJCalTP1_VIC01_60Hz_24

[Not Compliant]

Jitter Calibration PJ Injected vs. Histogram p-p



----General----	
Offline	True
Software Version	1.3.0
Calibration Data Version	Unknown; '1.3.0
Compliant	False
Non-compliance reason(s)	Procedure offline; Software status unreleas Calibration Clock-, Swing Calibration Data0 Clock+, Swing Calibration Clock-, Swing Cal Calibration, Swing Calibration Clock+, Swin
Video Mode	01: 640x480p @ 60 Hz
Color Depth	24 bit
Color Space	RGB full range
Use Color Bar pattern	False
Min Jitter	0 TBit
Max Jitter	250 mTBit
Jitter Step Size	125 mTBit
Differential Swing	800 mV
User Name	Unknown User
----M8195A - HDMI Sig. Gen.----	
DVI Mode	False
Fill up blanking periods with Null packets	False
Keep the signals after test?	False
Skip Pattern generation	True

```
----SCDC Controller----
SCDC supports Character Error Detections              False
Skip Link Training                                    False
Start delay between SCDC controller and TMDS signal   100 ms
----Dsc----
Use internal probe head termination voltage           True
```

Result	Jitter Injected [mTBit]	Measured Jitter for 500 kHz [mTBit]	Measured Jitter for 1 MHz [mTBit]	Measured Jitter for 7 MHz [mTBit]	Measured Jitter for 10 MHz [mTBit]
pass	0	100	100	100	100
pass	125	101	105	210	223
pass	250	103	111	320	347

Figure 26 Example result for Clock Jitter Calibration at TP1

- Result: (Pass/Fail) Test is considered as passed if the calibration step succeeds.
- Jitter Injected [mTBit]: The applied clock jitter amplitude for this step.
- Measured Jitter for 500 kHz [mTBit]: The measured 500 kHz clock jitter amplitude for this step.
- Measured Jitter for x MHz [mTBit]: The measured x MHz clock jitter amplitude for this step.

Data Jitter Calibration

Purpose and Method

This procedure calibrates the data jitter amplitude by measuring jitter with a DSO.

As defined in the HDMI CTS, there are two different data jitter injection techniques; data jitter is applied either by injecting it into the TMDS clock signal or by injecting it into the TMDS data lines. Therefore the calibration is divided into two parts:

- Data Jitter (on clock) Calibration
- Data Jitter (on data) Calibration

Like the clock jitter, the data jitter is sinusoidal jitter, which is calibrated for a frequency of 500 kHz with a clock jitter frequency of 10 MHz and also for a frequency of 1 MHz with a clock jitter frequency of 7 MHz.

For the calibration, a valid HDMI video signal is generated. The clock jitter values are applied according to the Clock Jitter Calibration TP1 and then as much data jitter is added as is required to achieve the worst case condition. The worst case condition is considered to be achieved if the eye almost touches the eye mask but does not violate it.

Since the data rate directly affects jitter, this calibration has to be conducted for each required data rate.

Connection Diagram

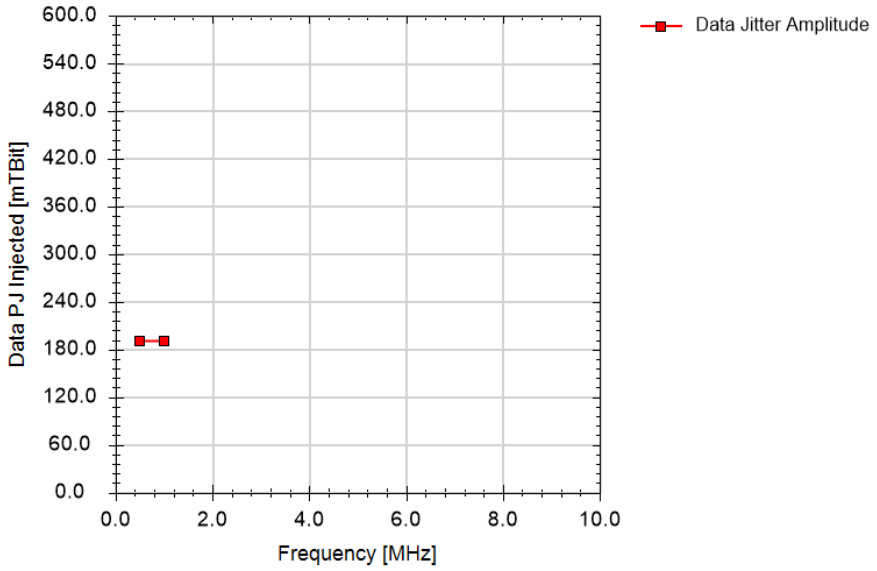
The connection setup for the Data Jitter Calibration is the same as for the Clock Jitter Calibration. See Figure 25 on page 56.

Result Description

Data Jitter Calibration

[Not Compliant]

Jitter Calibration PJ Injected vs. TJ Measured for VGA60Hz24 D_jitter on Clock



----General----	
Offline	True
Software Version	1.3.0
Calibration Data Version	Unknown; '1.3.0
Compliant	False
Non-compliance reason(s)	Procedure offline; Software status u Calibration Data0+, Swing Calibratic Swing Calibration Clock-, Swing Cali Time Calibration, Swing Calibration
Video Mode	01: 640x480p @ 60 Hz
Color Depth	24 bit
Color Space	RGB full range
Use Color Bar pattern	False
Min Jitter	0 TBit
Max Jitter	400 mTBit
Jitter Step Size	50 mTBit
Differential Swing	800 mV
Perform full D9021HDMC mask test for each calibration step	False
User Name	Unknown User
----M8195A - HDMI Sig. Gen.----	
DVI Mode	False
Fill up blanking periods with Null packets	False
Keep the signals after test?	False
Skip Pattern generation	True

```
----SCDC Controller----
SCDC supports Character Error Detections                    False
Skip Link Training                                          False
Start delay between SCDC controller and TMDS signal         100 ms
----Dso----
Use internal probe head termination voltage                 True
```

Result	Jitter Injected [MHz]	Data Jitter Amplitude [mTBit]	Clock Jitter Frequency [MHz]	Clock Jitter Amplitude [mTBit]
pass	0.500	190.000	10.000	149.9
pass	1.000	190.000	7.000	161.2

Figure 27 Example result for Data Jitter Calibration

- Result: (Pass/Fail) Test is considered as passed if the calibration step succeeds.
- Jitter Injected [MHz]: The applied data jitter frequency for this step.
- Data Jitter Amplitude [mTBit]: The measured data jitter amplitude for this step.
- Clock Jitter Frequency [MHz]: The clock jitter frequency for this step.
- Clock Jitter Amplitude [mTBit]: The measured clock jitter amplitude for this step.

Sink Calibrations – HDMI 2.1 TMDS

HF Swing Calibration

Availability

- HDMI 2.1 TMDS
- Clock+, Clock-, Data0+, Data0-, Data1+, Data1-, Data2+, Data2-

Purpose and Method

The test fixtures and cables attenuate the data or clock signals. To compensate for this, the differential signal levels are calibrated by connecting an HDMI fixture to the HDMI setup and measuring the differential swing with a DSO.

For the calibration, a software PRBS signal is generated at different swing voltage levels. For each step, the DSO measures the histogram to find the most frequently attained value of the differential swing. This calibration is done for each channel of the signal generator.

Connection Diagram

Figure 28 shows the connection diagram for the Swing Clock+ calibration. The differential probe head must be connected to the TPA-R output of the specific channel to be calibrated.

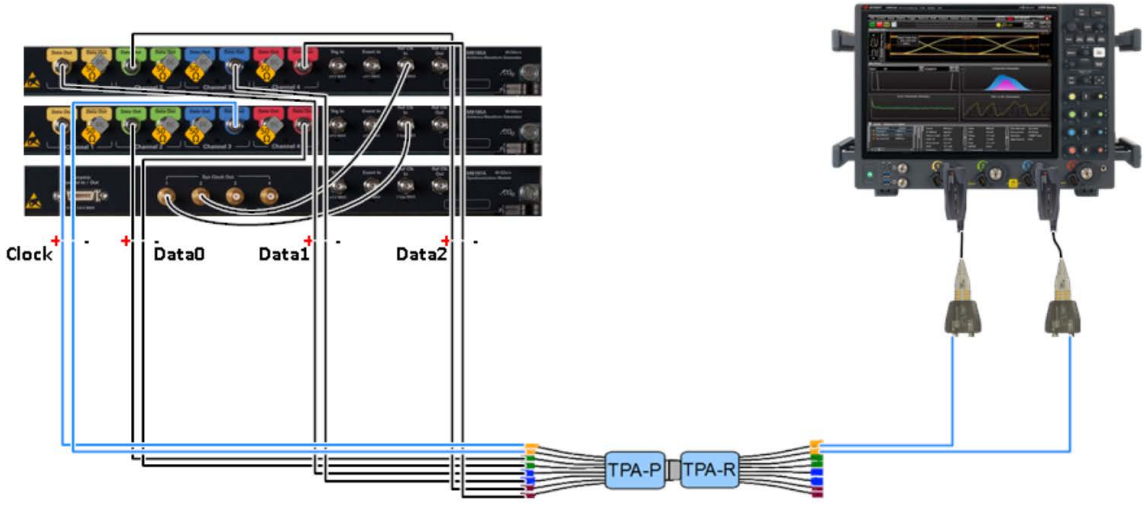


Figure 28 Example connection diagram for HF Swing Calibration

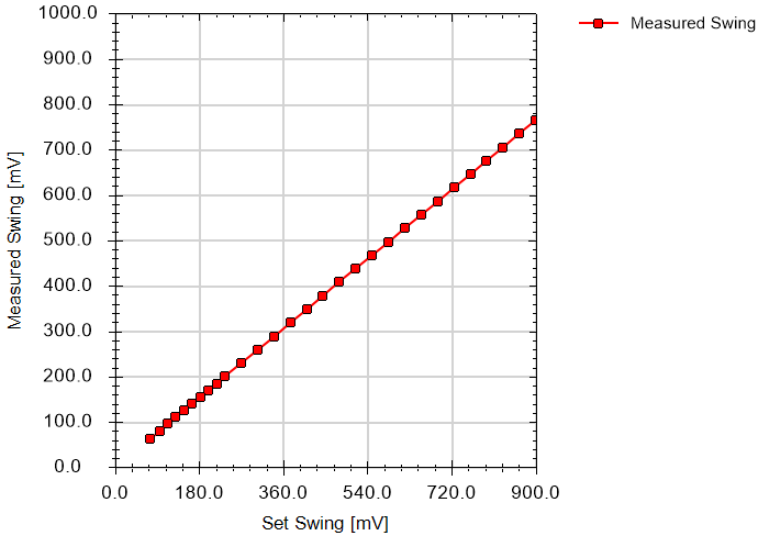
NOTE This connection diagram is specifically for the N5444A/N28XXA probe head. If a different probe head is selected in the Configure DUT dialog, the connection diagram will be slightly different.

Result Description

Ck+ 96: 3840x2160p @ 50 Hz

[Not Compliant]

Calibrates the Generator Swing



----General----	
Offline	True
Software Version	1.3.0
Calibration Data Version	Unknown; '1.3.0
Compliant	False
Non-compliance reason(s)	Procedure offline; Software st offline: Skew Calibration, Fal
Video Mode	96: 3840x2160p @ 50 Hz
Color Depth	24 bit
Color Space	RGB full range
Min Swing Value	35 mV
Max Swing Value	900 mV
Step Size	35 mV
DSO Channel used for Calibration	CHANnel1
DSO Channel used for Termination	CHANnel3
User Name	Unknown User

----M8195A - HDMI Sig. Gen.----	
DVI Mode	False
Fill up blanking periods with Null packets	False
Keep the signals after test?	False
Skip Pattern generation	True
----SCDC Controller----	
SCDC supports Character Error Detections	False
Skip Link Training	False
Start delay between SCDC controller and TMDS signal	100 ms
----Dso----	
Use internal probe head termination voltage	True

Result	Set Swing [mV]	Measured Swing [mV]
pass	900	765
pass	865	735
pass	830	706
pass	795	676
pass	760	646
pass	725	616
pass	690	587
pass	655	557
pass	620	527
pass	585	497
pass	550	468
pass	515	438
pass	480	408
pass	445	378
pass	410	349
pass	375	319
pass	340	289
pass	305	259
pass	270	230
pass	235	200
pass	217	185
pass	200	170
pass	182	155
pass	165	140
pass	147	125
pass	130	110
pass	112	96
pass	95	81
pass	75	64

Figure 29 Example result for HF Swing Calibration

- Result: (Pass/Fail) Test is considered as passed if the calibration step succeeds.
- Set Swing [mV]: The applied differential swing voltage for this step.
- Measured Swing [mV]: The measured differential swing voltage for this step.

HF Clock Jitter Calibration

Availability

- HDMI 2.1 TMDS
- TP2

Purpose and Method

This procedure calibrates the clock jitter amplitude for TMDS Character Rates ranging from 340 to 600 Mcsc.

Clock jitter is sinusoidal jitter injected into the HDMI Clock signal. Four different sinusoidal jitter frequencies are calibrated: 500 kHz, 1 MHz, 7 MHz and 10 MHz.

For this calibration, a valid HDMI video signal is generated at different jitter frequencies and amplitudes. The jitter is calculated in the signal waveform. For each step, the histogram peak-to-peak width of the jitter is measured by the oscilloscope.

This calibration must be conducted for the highest testing video mode selected. It is available when HDMI 2.1 testing is supported.

Connection Diagram

See Figure 30 and Figure 31 on page 66.

NOTE

In this calibration it is important to terminate all unused outputs with 50 Ω into 3.3 V. That is why the connection diagrams show the additional probe heads. Nevertheless, any 50 Ω in 3.3 V termination is valid and those additional probe heads will not be necessary.

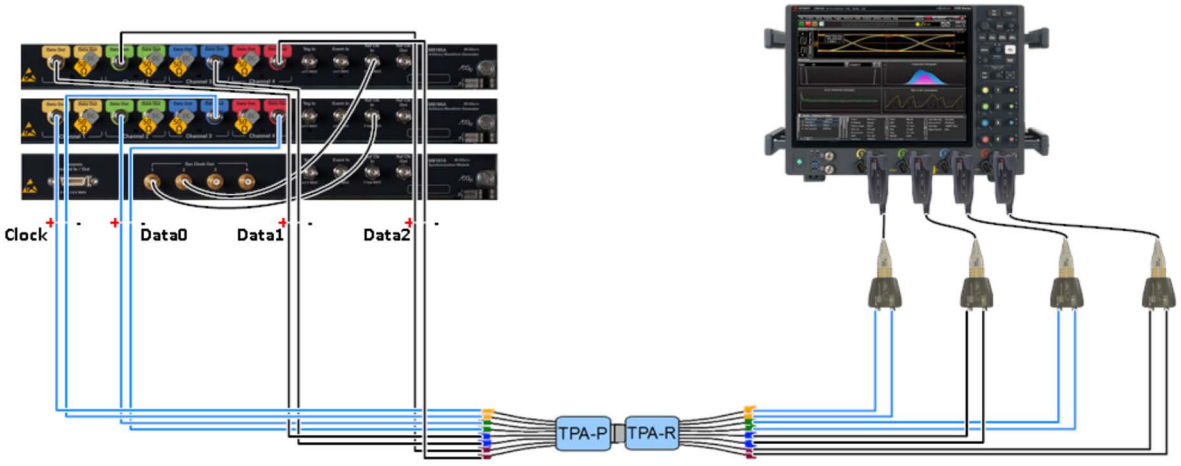


Figure 30 Example connection diagram for HF Clock Jitter Calibration (terminated with probes)

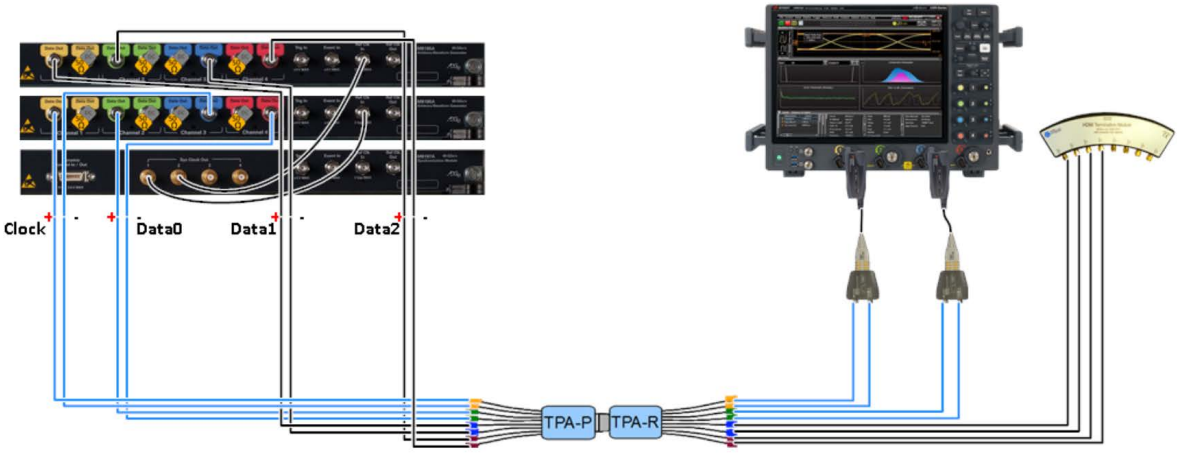


Figure 31 Example connection diagram for HF Clock Jitter Calibration (terminated with fixture)

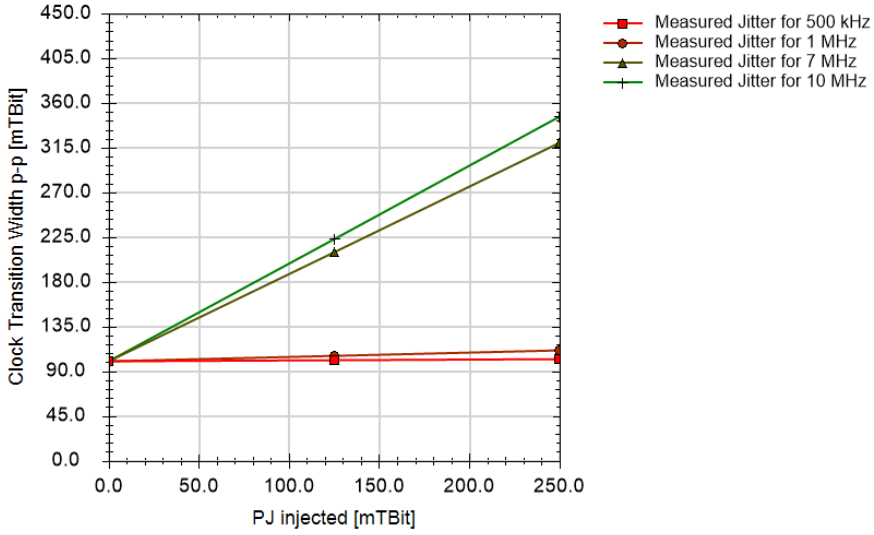
NOTE These connection diagrams are specifically for the N5444A/N28XXA probe head. If a different probe head is selected in the Configure DUT dialog, the connection diagram will be slightly different.

Result Description

ClkJCalTP2HF_VIC96_50Hz_24

[Not Compliant]

Jitter Calibration PJ Injected vs. Histogram p-p



----General----	
Offline	True
Software Version	1.3.0
Calibration Data Version	Unknown; '1.3.0
Compliant	False
Non-compliance reason(s)	Procedure offline; Software status unreleas HF Swing Calibration Data0+, HF Swing Calib Clock-, HF Swing Calibration Data0+, HF Swi Swing Calibration Clock-, HF Swing Calibrat
Video Mode	96: 3840x2160p @ 50 Hz
Color Depth	24 bit
Color Space	RGB full range
Use Color Bar pattern	False
Min Jitter	0 TBit
Max Jitter	250 mTBit
Jitter Step Size	125 mTBit
Differential Swing	800 mV
Cable Emulator	HDMI 2 0 NO SKEW
TMDS data to clock ratio 1:40	True
Use scrambled video signal	True
User Name	Unknown User
----M8195A - HDMI Sig. Gen.----	
DVI Mode	False
Fill up blanking periods with Null packets	False
Keep the signals after test?	False
Skip Pattern generation	True

----SCDC Controller----	
SCDC supports Character Error Detections	False
Skip Link Training	False
Start delay between SCDC controller and TMDS signal	100 ms
----Dso----	
Use internal probe head termination voltage	True

Result	Jitter Injected [mTBit]	Measured Jitter for 500 kHz [mTBit]	Measured Jitter for 1 MHz [mTBit]	Measured Jitter for 7 MHz [mTBit]	Measured Jitter for 10 MHz [mTBit]
pass	0	100	100	100	100
pass	125	101	105	210	223
pass	250	103	111	320	347

Figure 32 Example result for HF Clock Jitter Calibration

- Result: (Pass/Fail) Test is considered as passed if the calibration step succeeds.
- Jitter Injected [mTBit]: The applied clock jitter amplitude for this step.
- Measured Jitter for 500 kHz [mTBit]: The measured 500 kHz clock jitter amplitude for this step.
- Measured Jitter for x MHz [mTBit]: The measured x MHz clock jitter amplitude for this step.

HF Data Jitter Calibration

Availability

- HDMI 2.1 TMDS
- TP2
- Skew on complement (-), skew on normal (+)

Purpose and Method

This procedure calibrates the data jitter amplitude for TMDS Character Rates ranging from 340 to 600 Mcsc.

The data jitter is a sinusoidal jitter, which is calibrated first for a frequency of 500 kHz with a clock jitter frequency of 10 MHz and then for a frequency of 1 MHz with a clock jitter frequency of 7 MHz.

For the calibration, a valid HDMI video signal is generated. The clock jitter values are applied according to the HF clock jitter calibration and then the data jitter is added as much as required to achieve the worst case condition. The worst case condition is considered to be achieved if the eye almost touches the eye mask but does not violate it.

Moreover, the worst cable model requires addition of an intra-pair skew of 112 ps, first to all TMDS Data negative and then to all TMDS Data positive. To achieve this, the calibration is divided into two parts: skew on normal and skew on complement. This calibration has to be conducted for the highest testing video mode selected.

Connection Diagram

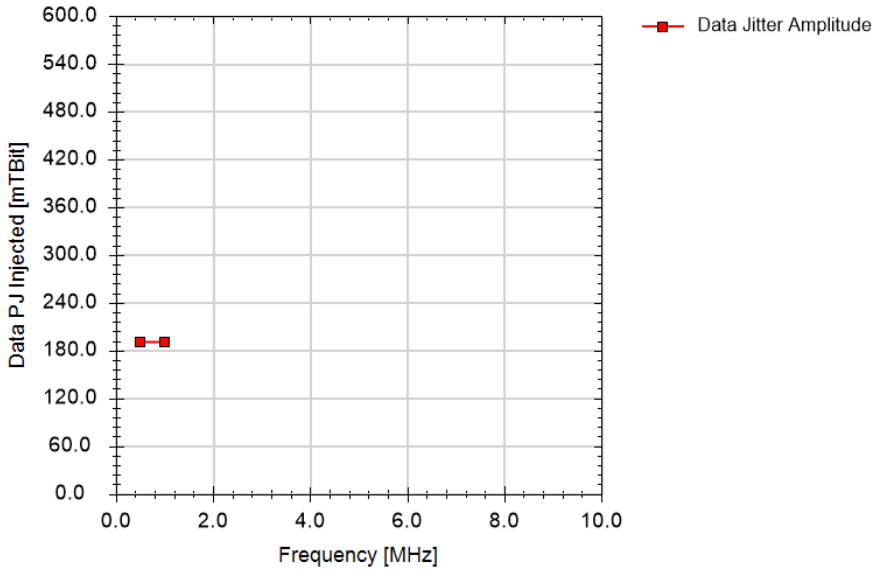
The connection setup for the Data Jitter TP2 calibration is the same as for the HF Clock Jitter calibrations. Refer to Figure 30 and Figure 31 on page 66.

Result Description

Data Jitter Calibration

[Not Compliant]

Jitter Calibration PJ Injected vs. TJ Measured for 3840x2160p50Hz24 D_jitter on Clock



----General----	
Offline	True
Software Version	1.3.0
Calibration Data Version	Unknown; '1.3.0
Compliant	False
Non-compliance reason(s)	Procedure offline; Software status u Data0+, HF Swing Calibration Clock-, Calibration, HF Swing Calibration Cl 3840x2160p50Hz24; Required cal unkno Clock-, HF Swing Calibration Data0-,
Video Mode	96: 3840x2160p @ 50 Hz
Color Depth	24 bit
Color Space	RGB full range
Use Color Bar pattern	False
Min Jitter	0 TBit
Max Jitter	400 mTBit
Jitter Step Size	50 mTBit
Differential Swing	800 mV
Perform full D9021HDMC mask test for each calibration step	False
Cable Emulator	HDMI 2 0 NO SKEW
TMDS data to clock ratio 1:40	True
Use scrambled video signal	True
User Name	Unknown User

----M8195A - HDMI Sig. Gen.----	
DVI Mode	False
Fill up blanking periods with Null packets	False
Keep the signals after test?	False
Skip Pattern generation	True
----SCDC Controller----	
SCDC supports Character Error Detections	False
Skip Link Training	False
Start delay between SCDC controller and TMDS signal	100 ms
----Dso----	
Use internal probe head termination voltage	True

Result	Jitter Injected [MHz]	Data Jitter Amplitude [mTBit]	Clock Jitter Frequency [MHz]	Clock Jitter Amplitude [mTBit]
pass	0.500	190.000	10.000	200.6
pass	1.000	190.000	7.000	218.0

Figure 33 Example result for HF Data Jitter Calibration

- Result: (Pass/Fail) The test is considered as passed if the calibration step succeeds.
- Jitter Injected [MHz]: The applied data jitter frequency for this step.
- Data Jitter Amplitude [mTBit]: The measured data jitter amplitude for this step.
- Clock Jitter Frequency [MHz]: The clock jitter frequency for this step.
- Clock Jitter Amplitude [mTBit]: The measured clock jitter amplitude for this step.

Sink Calibrations – HDMI 2.1 FRL

FRL Swing Calibration

Availability

- HDMI 2.1 FRL
- Lane0+, Lane0-, Lane1+, Lane1-, Lane2+, Lane2-, Lane3+, Lane3-

Purpose and Method

The test fixtures and cables attenuate the FRL signal. To compensate for this, the differential signal levels are calibrated by connecting an HDMI fixture to the HDMI setup and measuring the differential swing with a DSO.

For the calibration, a software generates an FRL pattern at different swing voltage levels. For each step, the DSO measures the histogram to find the most frequently attained value of the differential swing.

This calibration is done for each channel of the signal generator at the minimum supported data rate and the maximum supported data rate.

Connection Diagram

Figure 34 shows the connection diagram for the Swing Lane0+ calibration. The differential probe head must be connected to the TPA-R output of the specific channel to be calibrated.

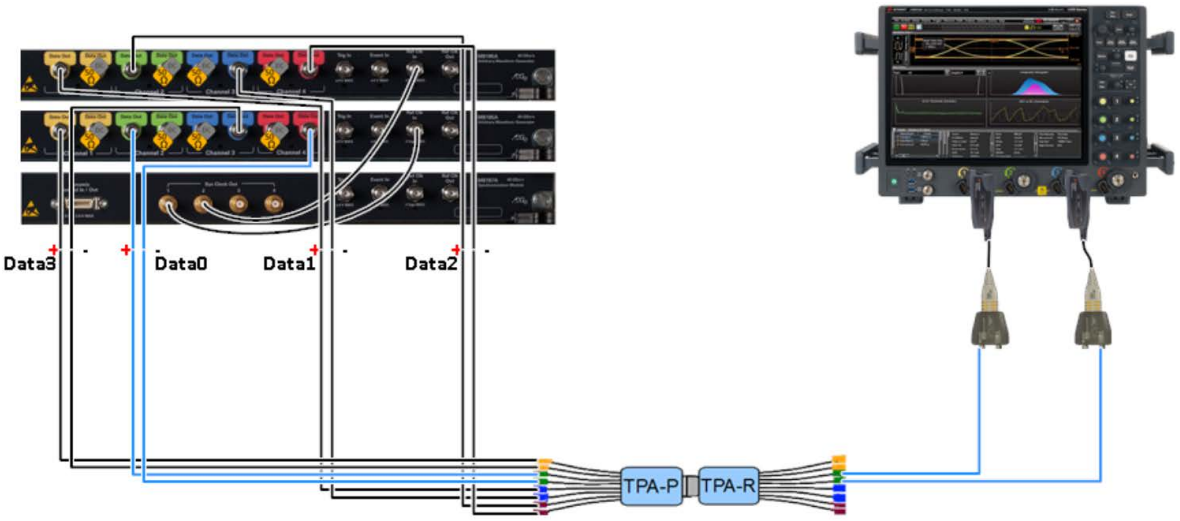


Figure 34 Example connection diagram for FRL Sink Swing Calibration, Lane0, M8195A setup

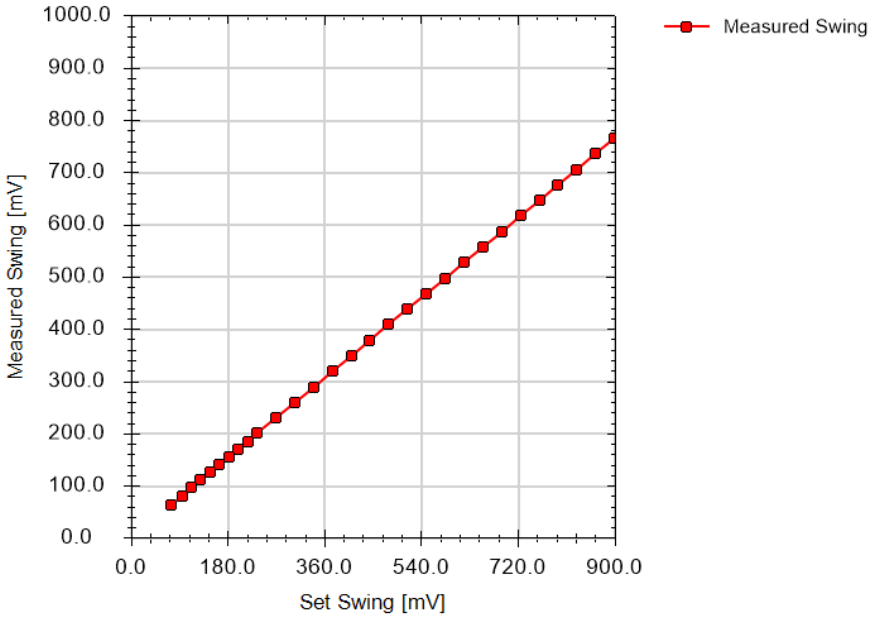
NOTE This connection diagram is specifically for the N5444A/N28XXA probe head. If a different probe head is selected in the Configure DUT dialog, the connection diagram will be slightly different.

Result Description

L0+ 3 GBit/s ThreeLane

[Not Compliant]

Calibrates the Generator Swing



----General----	
Offline	True
Software Version	1.3.0
Compliant	False
Non-compliance reason(s)	Procedure offline; Software status unreleas
Video Mode	FRL0 (3 Lanes) : RXSB33PAT @ 3 GBit/s
Min Swing Value	35 mV
Max Swing Value	900 mV
Step Size	35 mV
DSO Channel used for Calibration	CHANnel1
DSO Channel used for Termination	CHANnel3
User Name	Unknown User
----M8195A - HDMI Sig. Gen.----	
DVI Mode	False
Fill up blanking periods with Null packets	False
Keep the signals after test?	False
Skip Pattern generation	True

```
----SCDC Controller----
SCDC supports Character Error Detections              False
Skip Link Training                                    False
Start delay between SCDC controller and TMDS signal   100 ms
----Dso----
Use internal probe head termination voltage           True
```

Result	Set Swing [mV]	Measured Swing [mV]
pass	900	765
pass	865	735
pass	830	706
pass	795	676
pass	760	646
pass	725	616
pass	690	587
pass	655	557
pass	620	527
pass	585	497
pass	550	468
pass	515	438
pass	480	408
pass	445	378
pass	410	349
pass	375	319
pass	340	289
pass	305	259
pass	270	230
pass	235	200
pass	217	185
pass	200	170
pass	182	155
pass	165	140
pass	147	125
pass	130	110
pass	112	96
pass	95	81
pass	75	64

Figure 35 Example result for FRL Swing Lane0+ Calibration

- Result: (Pass/Fail) Test is considered as passed if the calibration step succeeds.
- Set Swing [mV]: The applied differential swing voltage for this step.
- Measured Swing [mV]: The measured differential swing voltage for this step.

Random Jitter Calibration

Availability

- HDMI 2.1 FRL
- Lane0, Lane1, Lane2

Purpose and Method

Random jitter is added to simulate the effects of thermal noise. Due to system intrinsic jitter, the effective jitter level is different from the value set in the data generator, so the jitter amplitude has to be calibrated. The test automation starts with a small RJ amplitude and increases that value in several steps over a defined range. For each step, the procedure measures the actual random jitter. The measurement is done on a real-time oscilloscope using the RJ/DJ-separation software EZJIT.

This calibration must be done separately for each lane, and at both the minimum supported data rate and the maximum supported data rate.

Connection Diagram

For this calibration, the unused lanes must be terminated.

If the terminations are done with scope probes, the connection diagram is as shown in Figure 36. In this case no re-connections are need to calibrate different lanes.

If the terminations are done with a termination fixture, the connection diagram is as shown in Figure 37 for Lane0. For other lanes, the differential probe head must be connected to the TPA-R output of the specific lane to be calibrated.

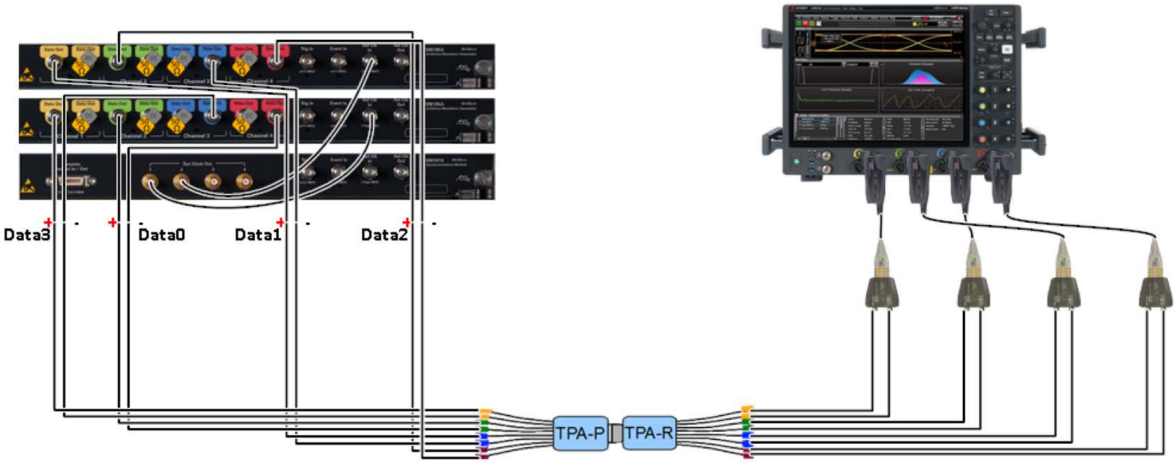


Figure 36 Example connection diagram for FRL Sink Random Jitter Calibration (terminated with scope probes)

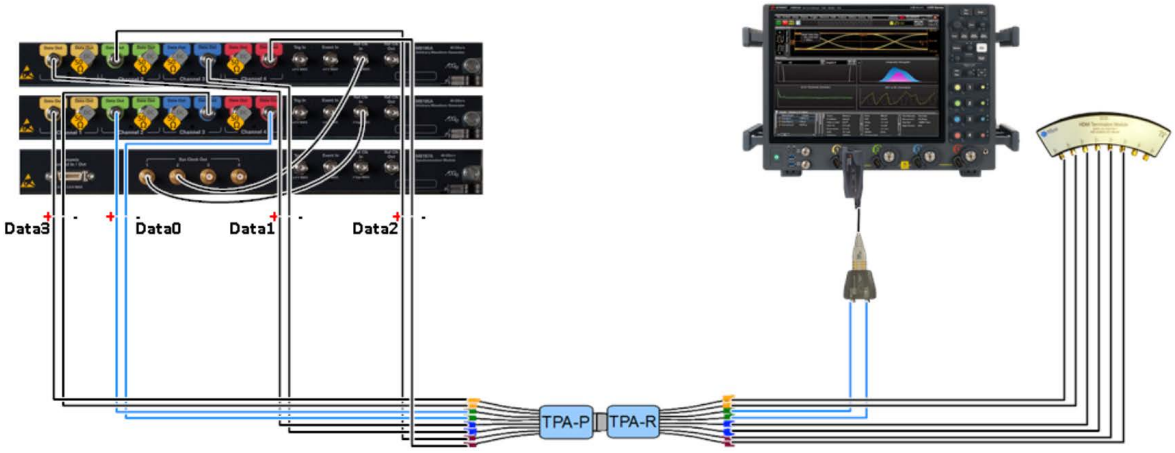


Figure 37 Example connection diagram for FRL Sink Random Jitter Calibration (terminated with fixture)

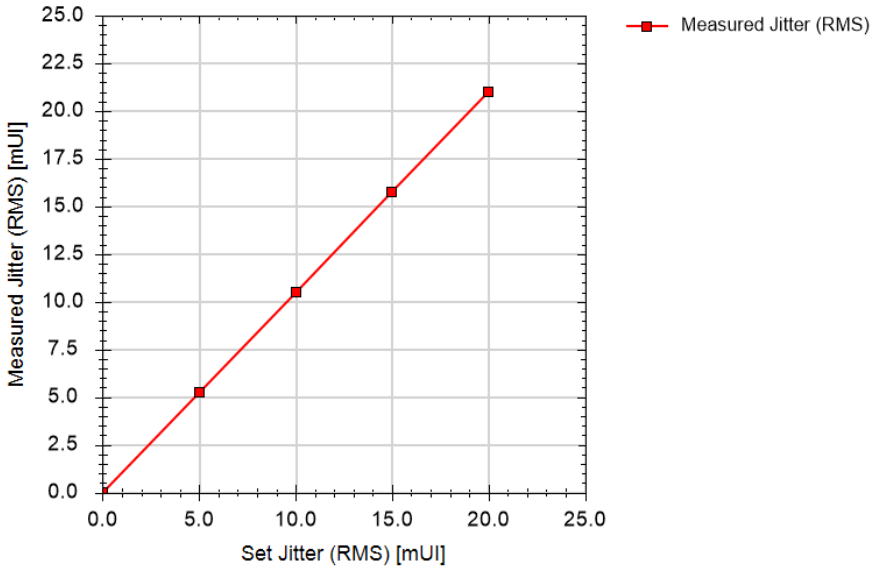
NOTE These connection diagrams are specifically for the N5444A/N28XXA probe head. If a different probe head is selected in the Configure DUT dialog, the connection diagram will be slightly different.

Result Description

Random Jitter Cal 3Gbps L0

[Not Compliant]

This procedure calibrates the random jitter RMS amplitude.



----General----	
Offline	True
Software Version	1.3.0
Calibration Data Version	Unknown
Compliant	False
Non-compliance reason(s)	Procedure offline; Software status unreleas Lane1+_FrlLinkRate_3Gbps_ThreeLane, FRL Swi Calibration, FRL Swing Calibration Lane0+_F Lane1-_FrlLinkRate_3Gbps_ThreeLane, FRL Swi Lane0+_FrlLinkRate_3Gbps_ThreeLane, FRL Swi Lane2+_FrlLinkRate_3Gbps_ThreeLane, FRL Swi
Video Mode	FRL0 (3 Lanes) : RXSB33PAT @ 3 GBit/s
Differential Swing	1 V
User Name	Unknown User
----M8195A - HDMI Sig. Gen.----	
DVI Mode	False
Fill up blanking periods with Null packets	False
Keep the signals after test?	False
Skip Pattern generation	True

```
----SCDC Controller----
SCDC supports Character Error Detections              False
Skip Link Training                                    False
Start delay between SCDC controller and TMDS signal   100 ms
----Dso----
Use internal probe head termination voltage           True
```

Set Jitter (RMS) [mUI]	Measured Jitter (RMS) [mUI]
0	0.0
5	5.3
10	10.5
15	15.8
20	21.0

Figure 38 Example result for FRL Random Jitter Calibration

- Set Jitter (RMS) [mUI]: The applied random jitter for this step.
- Measured Jitter (RMS) [mUI]: The measured random jitter amplitude for this step.

Eye Width Calibration

Availability

- HDMI 2.1 FRL
- Lane0, Lane1, Lane2, Lane3

Purpose and Method

This procedure calibrates the eye width by applying different values of PCB Loss Factor.

The test automation sets the initial PCB Loss Factor in the AWG by embedding the corresponding cable model and increases that value in linear steps. At each step, the eye width is measured on a real-time oscilloscope using a horizontal histogram.

The calibration finishes when the total jitter reaches the target jitter or when the generator limit is reached.

The Eye Width Calibration requires a minimum of 1 point below the Target Jitter and 1 point above. The greater the jitter, the smaller the eye.

If the Eye Width Calibration fails, please adjust the value of 'Start PCB Loss Factor' to meet the condition.

This calibration must be done separately for each lane, and at both the minimum supported data rate and the maximum supported data rate.

Connection Diagram

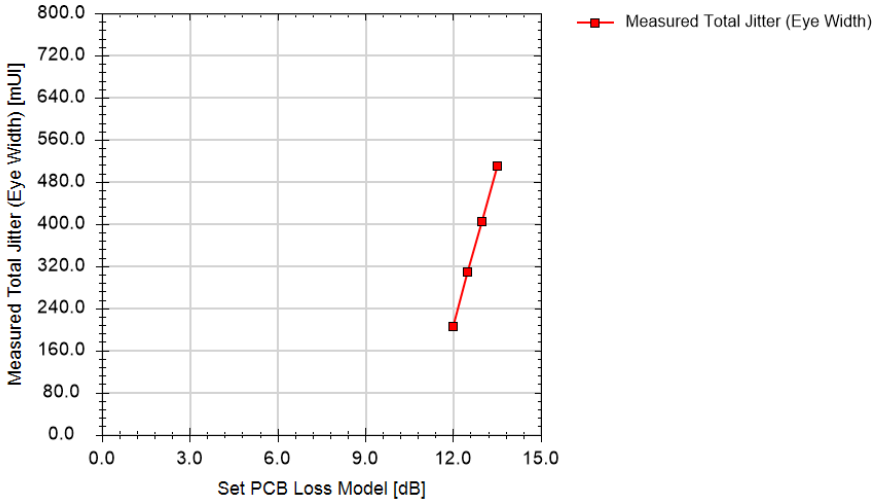
Refer to Figure 36 and Figure 37 on page 77.

Result Description

Eye Width Cal 3Gbps L0

[Not Compliant]

This calibrates the eye width



----General----	
Offline	True
Software Version	1.3.0
Calibration Data Version	Unknown; '1.3.0
Compliant	False
Non-compliance reason(s)	Procedure offline; Software status unreleas Lane2+_FrlLinkRate_3Gbps_ThreeLane, FRL Swi GBit/s ThreeLane L2, Random Jitter Calibrat Lane1+_FrlLinkRate_3Gbps_ThreeLane, FRL Swi Lane2-_FrlLinkRate_3Gbps_ThreeLane, Random Swing Calibration Lane0+_FrlLinkRate_3Gbps_ Calibration Lane1-_FrlLinkRate_3Gbps_ThreeL ThreeLane L1
Video Mode	FRL0 (3 Lanes) : RXSB33PAT @ 3 GBit/s
Cable Emulator	HDMI 2 1 WCM3
Enable Crosstalk	True
Measurement Cycles	4
Start PCB Loss Factor	12 dB
Target Jitter Lane0	500 mUI
Target Jitter Lane1	500 mUI
Target Jitter Lane2	500 mUI
Differential Swing	500 mV
User Name	Unknown User
----M8195A - HDMI Sig. Gen.----	
DVI Mode	False
Fill up blanking periods with Null packets	False
Keep the signals after test?	False
Skip Pattern generation	True

```
----SCDC Controller----
SCDC supports Character Error Detections              False
Skip Link Training                                    False
Start delay between SCDC controller and TMDS signal   100 ms
----Dso----
Use internal probe head termination voltage           True
```

Set PCB Loss Model [dB]	Measured Total Jitter (Eye Width) [mUI]
12.0	205
12.5	308
13.0	404
13.5	509

Figure 39 Example result for FRL Eye Width Calibration

- Set PCB Loss Model [dB]: The applied PCB Loss Model for this step.
- Measured Total Jitter (Eye Width) [mUI]: The measured total jitter amplitude for this step.

Eye Height Calibration

Availability

- HDMI 2.1 FRL
- Lane0, Lane1, Lane2, Lane3

Purpose and Method

This procedure calibrates the eye height by applying different values of differential voltage.

The test automation sets the initial differential voltage in the AWG and decreases that value in linear steps. At each step, the eye height is measured on a real-time oscilloscope using a horizontal histogram.

The calibration ends when the eye height is less than the Target Height.

The Eye Height Calibration requires a minimum of 1 point above the Target Height and 1 point below. The smaller the differential voltage, the smaller the eye.

If the Eye Height Calibration fails, please adjust the value of 'First Differential Voltage' to meet the condition.

This calibration must be done separately for each lane, and at both the minimum supported data rate and the maximum supported data rate.

Connection Diagram

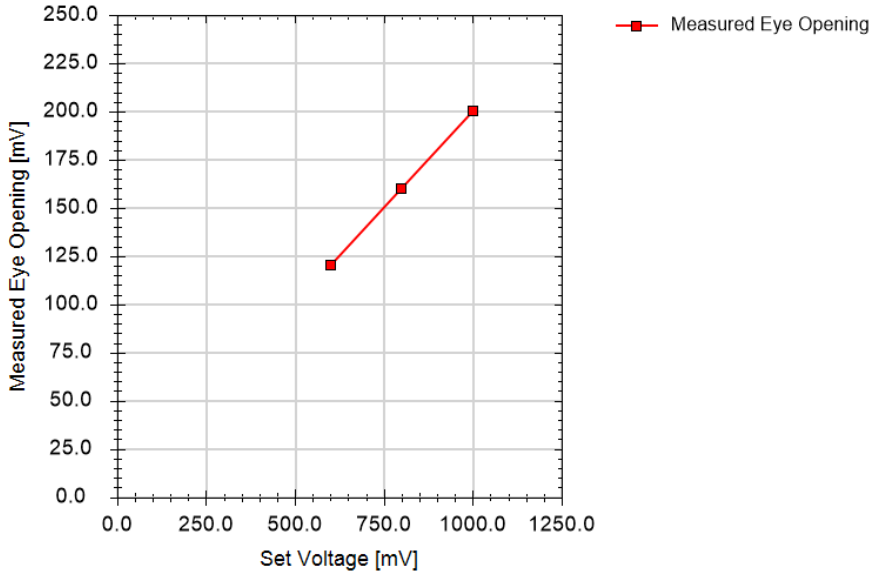
Refer to Figure 36 and Figure 37 on page 77.

Result Description

Eye Height Cal 3Gbps L0

[Not Compliant]

This calibrates the eye height



----General----	
Offline	True
Software Version	1.3.0.9_RC
Calibration Data Version	Unknown; '1.3.0.9_RC
Compliant	False
Non-compliance reason(s)	Procedure offline; Software status unreleas Lane2+_FrlLinkRate_3Gbps_ThreeLane, FRL Swi GBit/s ThreeLane L2, Random Jitter Calibrat Lane1+_FrlLinkRate_3Gbps_ThreeLane, FRL Swi Lane2-_FrlLinkRate_3Gbps_ThreeLane, Random Swing Calibration Lane0+_FrlLinkRate_3Gbps_ Calibration Lane1-_FrlLinkRate_3Gbps_ThreeL ThreeLane L1
Video Mode	FRL0 (3 Lanes) : RXSB33PAT @ 3 GBit/s
Cable Emulator	HDMI 2 1 WCM3
Enable Crosstalk	True
Measurement Cycles	4
Target Height Lane0	150 mV
Target Height Lane1	150 mV
Target Height Lane2	150 mV

First Differential Voltage	1 V
Target Jitter Lane0	500 mUI
Target Jitter Lane1	500 mUI
Target Jitter Lane2	500 mUI
Applied Voltage Step	-200 mV
User Name	Unknown User
----M8195A - HDMI Sig. Gen.----	
DVI Mode	False
Fill up blanking periods with Null packets	False
Keep the signals after test?	False
Skip Pattern generation	True
----SCDC Controller----	
SCDC supports Character Error Detections	False
Skip Link Training	False
Start delay between SCDC controller and TMDS signal	100 ms
----Dso----	
Use internal probe head termination voltage	True

Set Voltage [mV]	Measured Eye Opening [mV]
1000	200
800	160
600	120

Figure 40 Example result for FRL Eye Height Calibration

- Set Voltage [mV]: The applied voltage amplitude for this step.
- Measured Eye Opening [mV]: The measured eye opening for this step.

5 HDMI Cable Calibrations

Before any sink or cable test procedure can be run, the HDMI PHY test system must be calibrated. The procedures used for a cable DUT are described in this chapter.

Overview

The purpose of the calibration procedures is to calibrate the TDMS and FRL signal generator levels and timings.

ValiFrame automatically determines the required calibration procedures according to the parameters set in the Configure Product dialog, including

- Product Type (sink or cable)
- Test Mode (compliance or expert)
- TMDS or FRL
- Supported Video Modes
- Color Depth
- Color Space
- Cable Type

The results of each calibration are stored in the 'Calibration' folder of ValiFrame, so that they can be used for another calibration or test, as required.

The order of the procedures in the procedure tree is driven mainly by the calibration dependencies.

For calibrations, in general, the following calibrations are prerequisite:

- The appropriate skew calibration.
- All the calibrations listed above it in the same branch of the procedure tree.

They are not listed explicitly for each calibration in this User Guide. However, they can be found directly in the application (see Required Calibration Data on page 36 of this User Guide).

Note that ValiFrame attempts to reduce the calibration effort by coalescing similar data rates into one calibration, when no significant deviation in the results is expected.

DC and single-ended levels are always determined with respect to the termination voltage.

Calibrations for Both Sinks and Cables

Skew Calibration

For a description of this calibration, see Skew Calibration on page 43.

Fall/Rise Time Calibration

For a description of this calibration, see Fall/Rise Time Calibration on page 48.

This calibration is not available for Category 3 (FRL) cables.

Cable Calibrations – HDMI 1.4

Swing Calibration

Availability

- HDMI 1.4
- Cable type: Category 1 (Home), Category 2 (Home)
- Clock+, Clock-, Data0+, Data0-, Data1+, Data1-, Data2+, Data2-

Description

For a description of this calibration, see Swing Calibration on page 51.

Data Jitter (on Clock) Calibration

Availability

- HDMI 1.4
- Cable type: Category 1 (Home), Category 2 (Home)
- TP1

Purpose and Method

This procedure calibrates the data jitter amplitude by measuring jitter with a DSO.

For Cable DUTs, data jitter is applied by injecting it into the TMDS clock signal. The data jitter is sinusoidal jitter that is calibrated for a frequency of 500 kHz with a clock jitter frequency of 10 MHz.

For the calibration, a valid HDMI video signal is generated. The clock jitter values are applied and then as much data jitter is added as is required to achieve the worst case condition. The worst case condition is considered to be achieved if the eye almost touches the eye mask but does not violate it.

Since the data rate directly affects jitter, this calibration has to be conducted for each required data rate.

Connection Diagram

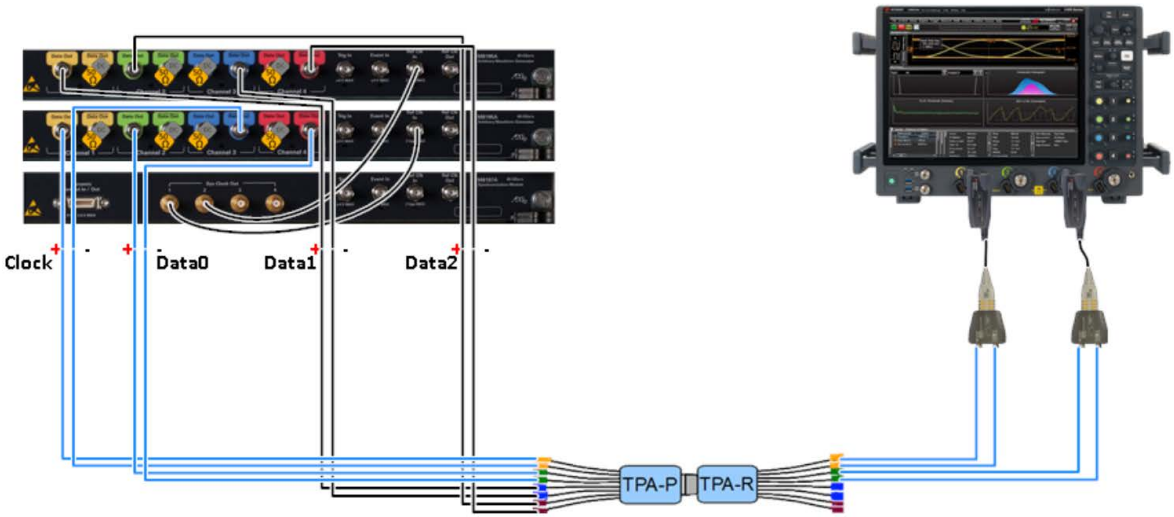


Figure 41 Example connection diagram for Cable Data Jitter Calibration – M8195A setup

Result Description

Data Jitter Calibration

[Not Compliant]

Jitter Calibration PJ Injected vs. TJ Measured for 1280x1024p111Hz24 D_jitter on Clock

----General----	
Offline	True
Software Version	1.3.0
Calibration Data Version	Unknown; '1.3.0
Compliant	False
Non-compliance reason(s)	Procedure offline; Software status u Required cal not compliant: Skew Cal Fall/Rise Time Calibration; Required Skew Calibration, Fall/Rise Time Cal Required cal unknown/unreleased: Ske Fall/Rise Time Calibration
Video Mode	138: 1280x1024p @ 111 Hz
Color Depth	24 bit
Color Space	RGB limited range
Use Color Bar pattern	False
Min Jitter	0 TBit
Max Jitter	400 mTBit
Jitter Step Size	50 mTBit

Differential Swing	800 mV
Perform full D9021HDMC mask test for each calibration step	False
User Name	Unknown User
Cable Equalizer	5m Cable Equalizer
----M8195A - HDMI Sig. Gen.----	
Fill up blanking periods with Null packets	False
Keep the signals after test?	False
Skip Pattern generation	True
----Dso----	
Use internal probe head termination voltage	True

Result	Frequency [MHz]	Data PJ Injected [mTBit]
pass	0.5	190.0

Figure 42 Example result for Data Jitter Calibration

- Result: (Pass/Fail) The procedure is considered as passed if the calibration step succeeds.
- Frequency [MHz]: Frequency of the injected sinusoidal jitter. This is the jitter frequency that will be used in tests.
- Data PJ Injected [mTBit]: The amplitude of the periodic jitter injected into the data.

Cable Calibrations – HDMI 2.1 TMDS

HF Swing Calibration

Availability

- HDMI 2.1 TMDS
- Cable type: Category 1 (Home), Category 2 (Home)
- Clock+, Clock-, Data0+, Data0-, Data1+, Data1-, Data2+, Data2-

Description

For a description of this calibration, see Swing Calibration on page 51.

Data Jitter (on Clock) Calibration 6G

Availability

- HDMI 2.1 TMDS
- Cable type: Category 1 (Home), Category 2 (Home)

Description

For a description of this calibration, see Data Jitter (on Clock) Calibration on page 91.

Cable Calibrations – HDMI 2.1 FRL

FRL Cable Swing Calibration

Availability

- HDMI 2.1 FRL
- Cable type: Category 3 (FRL)
- Lane0+, Lane0-, Lane1+, Lane1-, Lane2+, Lane2-, Lane3+, Lane3-

Purpose and Method

The cabling attenuates the FRL signal. To compensate for this, the differential signal levels are calibrated by measuring the differential swing with a DSO.

For the calibration, the software sends FRL patterns at different swing voltage levels. For each step, the DSO measures the histogram to find the most frequent value of the differential swing. This calibration is done for each channel of the signal generator.

In Compliance mode, this calibration is available for all data rates. In Expert mode, it is available for the highest supported data rate.

Connection Diagram

Figure 43 shows the connection diagram for the Swing Lane0+ calibration. The differential probe head must be connected to the data output of the specific lane to be calibrated.

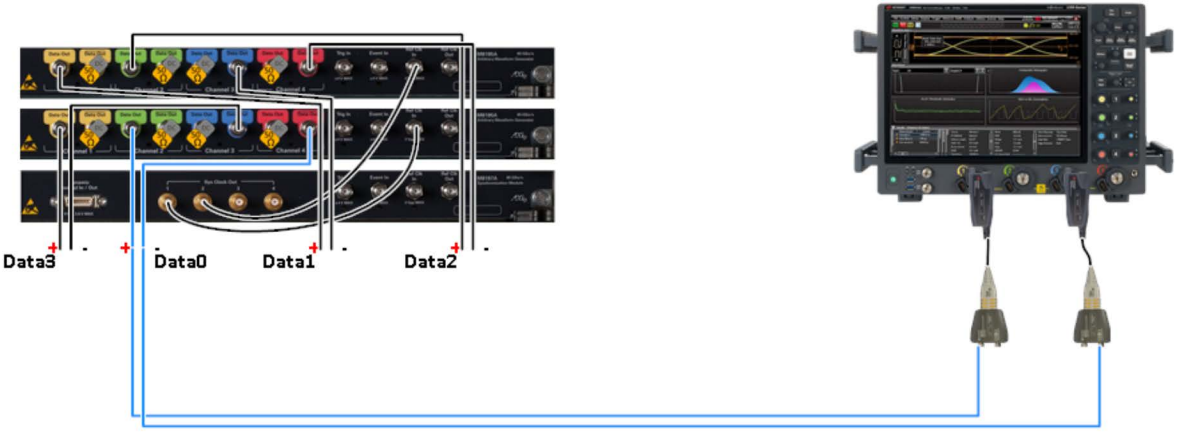


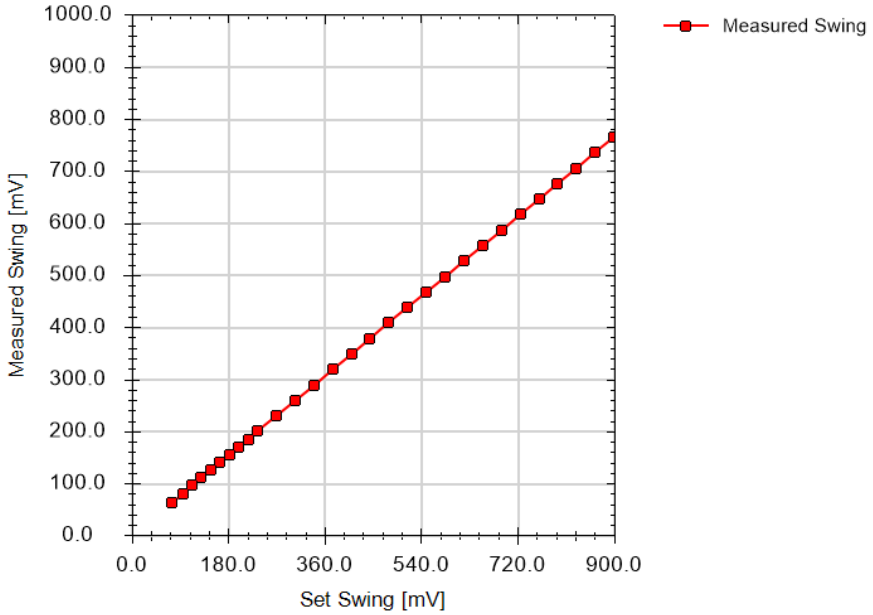
Figure 43 Example connection diagram for FRL Cable Swing Calibration

Result Description

L0+ 3 GBit/s ThreeLane

[Not Compliant]

Calibrates the Generator Swing



----General----	
Offline	True
Software Version	1.3.0
Compliant	False
Non-compliance reason(s)	Procedure offline; Software status unreleased
Video Mode	FRL0 (3 Lanes) : RXSB33PAT @ 3 GBit/s
Min Swing Value	35 mV
Max Swing Value	900 mV
Step Size	35 mV
DSO Channel used for Calibration	CHANnel1
DSO Channel used for Termination	CHANnel3
User Name	Unknown User
Cable Equalizer	5m Cable Equalizer
----M8195A - HDMI Sig. Gen.----	
Fill up blanking periods with Null packets	False
Keep the signals after test?	False
Skip Pattern generation	True
----Dso----	
Use internal probe head termination voltage	True

Result	Set Swing [mV]	Measured Swing [mV]
pass	900	765
pass	865	735
pass	830	706
pass	795	676
pass	760	646
pass	725	616
pass	690	587
pass	655	557
pass	620	527
pass	585	497
pass	550	468
pass	515	438
pass	480	408
pass	445	378
pass	410	349
pass	375	319
pass	340	289
pass	305	259
pass	270	230
pass	235	200
pass	217	185
pass	200	170
pass	182	155
pass	165	140
pass	147	125
pass	130	110
pass	112	96
pass	95	81
pass	75	64

Figure 44 Example result for FRL Cable Swing Calibration

- Result: (Pass/Fail) The procedure is considered as passed if the calibration step succeeds.
- Set Swing [mV]: The applied differential swing voltage.
- Measured Swing [mV]: The measured differential swing voltage.

Random Jitter Calibration

Availability

- HDMI 2.1 FRL
- Cable type: Category 3 (FRL)
- Highest supported data rate

Purpose and Method

The FRL Random Jitter Calibration for a cable DUT is similar to the FRL Random Jitter Calibration on page 76 for a sink DUT. However, the connection diagram is different because the TPA-R is embedded for FRL Cable calibrations (see below).

This calibration is available for the highest supported data rate.

Connection Diagram

See Figure 45 and Figure 46.

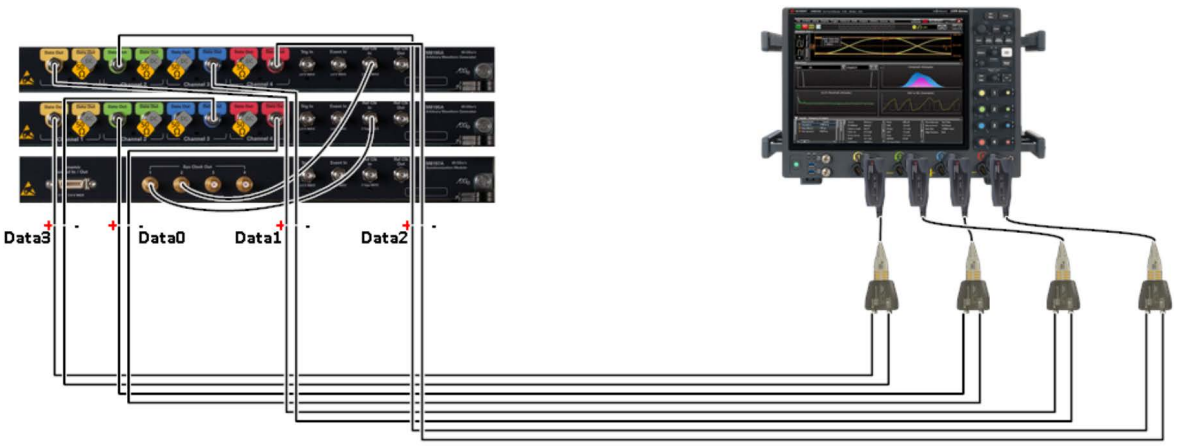


Figure 45 Example connection diagram for FRL Cable Random Jitter Calibration (terminated with scope probes)

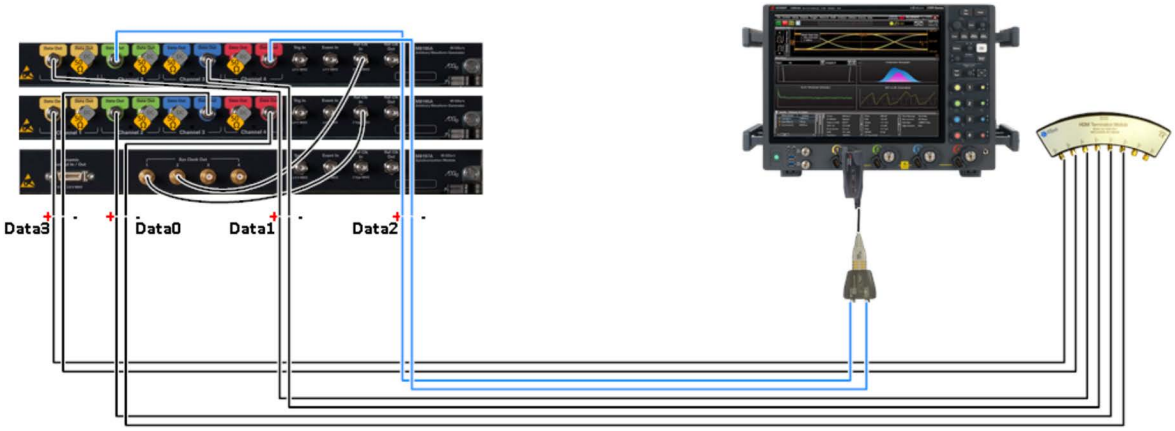


Figure 46 Example connection diagram for FRL Cable Random Jitter Calibration (terminated with a fixture)

Eye Width Calibration

Availability

- HDMI 2.1 FRL
- Cable type: Category 3 (FRL)
- Highest supported data rate

Purpose and Method

The FRL Eye Width Calibration for a cable DUT is similar to the FRL Eye Width Calibration on page 80 for a sink DUT. However, the connection diagram is different because the TPA-R is embedded for FRL cable calibrations (see below).

This calibration is available for the highest supported data rate.

Connection Diagram

See Figure 45 on page 99 and Figure 46 on page 100.

Eye Height Calibration

Availability

- HDMI 2.1 FRL
- Cable type: Category 3 (FRL)
- Highest supported data rate

Purpose and Method

The FRL Eye Height Calibration for a cable DUT is similar to the FRL Eye Height Calibration on page 83 for a sink DUT. However, the connection diagram is different because the TPA-R is embedded for FRL Cable calibrations (see below).

This calibration is available for the highest supported data rate.

Connection Diagram

See Figure 45 on page 99 and Figure 46 on page 100.

FRL Cable Mode Conversion Swing Calibration

Availability

- HDMI 2.1 FRL
- Cable type: Category 3 (FRL), Active Cable
- Compliance mode only
- Data rate: 10 GBit/s
- Lane0+, Lane0-, Lane1+, Lane1-, Lane2+, Lane2-, Lane3+, Lane3-

Purpose and Method

This calibrates the swing voltage for the mode conversion of each FRL lane. The procedure is similar to the FRL Swing Calibration on page 72.

This calibration is available only if you check “Active Cable” in the Configure Product dialog, only in Compliance mode and only for 10 GBit/s.

Connection Diagram

Figure 43 on page 96 shows the connection diagram for the FRL Cable Mode Conversion Swing Lane0+ calibration. The differential probe head must be connected to the data output of the specific lane to be calibrated.

Mode Conversion Calibration

Availability

- HDMI 2.1 FRL
- Cable type: Category 3 (FRL), Active Cable
- Compliance mode only
- Data rate: 10 GBit/s

Purpose and Method

The purpose of this calibration is to measure the differential mode voltage input and the common mode voltage input of all FRL lanes at 6 GHz. These values are necessary for the test HFR7-23 Mode Conversion on page 231.

The calibration is divided into two steps. In the first step, the Vdm_input and Vcm_input of lane 3 and lane 0 are measured using a real-time oscilloscope. In the second step, after the cables have been re-connected, those parameters are measured for lane 2 and lane 4.

This calibration is available only if you check “Active Cable” in the Configure Product dialog, only in Compliance mode and only for 10 GBit/s.

Connection Diagram

For this calibration, the unused lanes must be terminated. The connection diagram is as shown in Figure 47.

Figure 47 Example connection diagram for Mode Conversion Calibration (Lanes 3 & 0)

Result Description

Calculated Vdm_input and Vcm_input for all FRL lanes

[Not Compliant]

Calculated Vdm_input and Vcm_input for all FRL lanes

----General----	
Offline	True
Software Version	1.3.0
Calibration Data Version	Unknown
Compliant	False
Non-compliance reason(s)	Procedure offline; Software status unr FRL Cable Mode Conversion Swing Calibr Calibration Lane3-; Required cal offli Calibration Lane1-, FRL Cable Mode Con unknown/unreleased: Skew Calibration, Cable Mode Conversion Swing Calibratio
Cable Emulator	None
Enable Crosstalk	False
User Name	Unknown User
----M8195A - HDMI Sig. Gen.----	
Fill up blanking periods with Null packets	False
Keep the signals after test?	False
Skip Pattern generation	True
----Dso----	
Use internal probe head termination voltage	True

Vdm_Input_Lane 3 [mV]	Vdm_Input_Lane 0 [mV]	Vcm_Input_Lane 3 [mV]	Vcm_Input_Lane 0 [mV]	Vdm_Input_Lane 1 [mV]	Vdm_Input_Lane 2 [mV]	Vcm_Input_Lane 1 [mV]	Vcm_Input_Lane 2 [mV]
35.000	45.000	15.000	16.000	35.000	45.000	15.000	16.000

Figure 48 Example result for Mode Conversion Calibration

- Vdm_Input_Lane X [mV]: The differential mode voltage input measured at lane X.
- Vcm_Input_Lane X [mV]: The common mode voltage input measured at lane X.

6 FRL Waveform Calculation

The procedures described in this chapter calculate FRL waveforms that are required in particular Sink Tests (HFR2-2 to HFR2-5).

Calculate FRL Waveforms

Availability

- Product Type: Sink
- Test Mode: Compliance Mode
- DUT Setting: FRL

Purpose and Method

This procedure calculates and saves the FRL waveforms that are required for the Sink Tests HFR2-2 to HFR2-4.

The procedure consists of four essential steps:

1 Calculate the base FRL waveforms.

2 Calculate the FRL waveforms with WCM and crosstalk.

3 Calculate the FRL waveforms with WCM and crosstalk along with positive data rate deviation.

4 Calculate the FRL waveforms with WCM and crosstalk along with negative data rate deviation.

Connection Diagram

Not required.

Calculate HFR2-5 FRL Waveforms

Purpose and Method

This procedure calculates and saves the FRL waveforms that are required for the Sink Test HFR2-5 Jitter Tolerance on page 167.

The procedure is performed in several steps. In the first step, the base FRL waveforms are calculated. In the next few steps, the FRL waveforms (with sinusoidal jitter injected) are calculated. The set of sinusoidal jitter amplitudes and frequencies for each step is defined in *Table 6-28 "Sink Jitter Tolerance Requirement"* and *Table 6-29 "Sinusoidal Jitter Frequency and Jitter Amplitude for Sink Jitter Tolerance Test"* of the HDMI 2.1 specification.

Connection Diagram

Not required.

7 HDMI Receiver Tests for Sinks

Once the HDMI PHY Test Station has been calibrated, receiver test procedures can be run. The tests for sink DUTs described at the beginning of this chapter are required for compliance. The additional tests in expert mode (last two sections listed above) are intended for custom characterization and debugging of sink DUTs.

Overview

ValiFrame automatically determines the required sink tests from the combination of the supported video modes, color modes and 3D modes as specified in the Configure Product dialog. The method of compliance testing depends on whether the signal is TMDS (HDMI 1.4 and HDMI 2.1 TMDS) or FRL (HDMI 2.1 FRL).

TMDS Signals

For TMDS signals, sink electrical compliance testing is conducted by applying a stressed signal and observing the video output for errors.

There are different test cases:

- differential swing voltage tolerance
- intra-pair skew tolerance
- inter-pair skew tolerance (only HDMI 2.1 TMDS)
- jitter tolerance
- video timing tests (only HDMI 2.1 TMDS)
- pixel decoding tests (only HDMI 2.1 TMDS)

Additionally, the ValiFrame solution provides certain further tests, which can be used for sink DUT characterization. These additional tests are found in the application under the node “Expert Mode” and are described in the section Additional Sink Tests in Expert Mode beginning on page 170 in this User Guide.

Every test consists of multiple test steps, each with different stressed parameters and/or parameter levels. As soon as the TMDS generator is programmed, you are prompted to observe the video for pixel errors (see Figure 49).

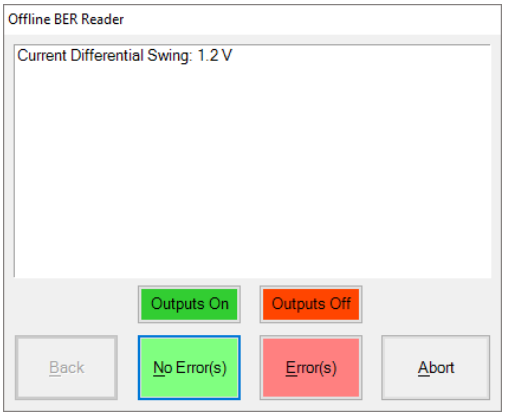


Figure 49 Offline BER Reader dialog

FRL Signals

HDMI FRL sink electrical compliance testing is conducted by applying a stressed signal, performing the loopback training and automatically reading errors with the SCDC Controller.

There are different test cases:

- differential swing voltage tolerance
- intra-pair skew tolerance
- inter-pair skew tolerance
- minimum link rate
- jitter tolerance

FRL tests must be conducted for the highest and the lowest supported data rates.

Additionally, the ValiFrame solution provides certain further tests, which can be used for sink DUT characterization. For FRL signals these additional tests are found in the application under the node “HDMI 2.1” under the node “Expert Mode” and are described in the section Additional HDMI 2.1 FRL Signal Sink Tests in Expert Mode beginning on page 206 in this User Guide.

Prerequisite Calibrations

Prerequisite calibrations are not listed explicitly for each test in this User Guide. However, they can be found directly in the application (see Required Calibration Data on page 36 of this User Guide).

HDMI ValiFrame Parameters

The parameters used in a test are no longer listed with the procedure descriptions in this User Guide. Instead they can be found in Chapter 9 beginning on page 237.

The following parameters that are used in Sink tests require a longer explanation and so are included here.

Voltage Offset Factor, Voltage Swing Factor

The HDMI levels are defined relative to the high level, which is nominally at $V_{NominalOffset}$ = 3.3 V. The instrument defines levels that are relative to the center of the signal. To calculate the instrument offset, use the formula

$$V_{OffsetInstrument} = V_{OffsetFactor} * V_{OffsetHDMI} - V_{SwingFactor} * (V_{diff}/2) - V_{NominalOffset}$$

These factors allow another definition to be set for the offset in HDMI. It is imperative that the AC-coupled source be enabled to set the factors $V_{OffsetFactor}$ =1 and $V_{SwingFactor}$ = 0.

Use Slider Dialog

In Expert mode, you may use a slider to set differential swing voltage levels (see Figure 50). If set to 'True', the slider dialog is displayed and if set to 'False', only such voltage levels are tested that are required by the HDMI CTS.

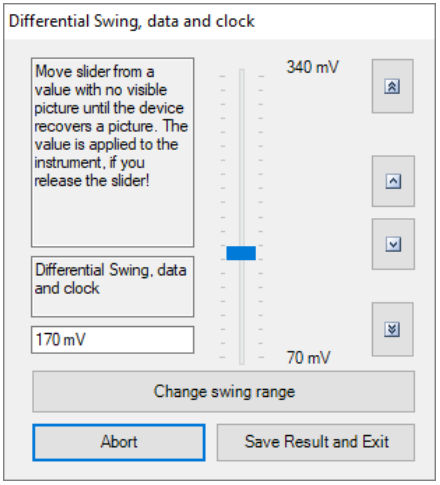


Figure 50 Slider dialog for Differential Swing in Expert Mode

HDMI 1.4 TMDS Signal

ID 8-5 Differential Swing

Availability

- HDMI 1.4
- Compliance Mode, Expert Mode
- All Channels
- V_{ICM} = 2.9 V, 3.0 V, 3.3 V

Purpose and Method

This procedure tests for compliance according to HDMI CTS Version 1.4b, Section 8.3 “Sink – Electrical”, Test ID 8-5: “TMDS – Min/Max Differential Swing Tolerance”.

A video signal at the highest supported data rate is generated with calibrated voltage levels and with no jitter applied. Depending on data rate, this procedure is done with a V_{ICM} of 2.9 V, 3.0 V or 3.3 V.

The differential swing voltage level is decreased from 170 mV until the DUT fails to support the signal without errors. With a V_{ICM} of 3.3 V, the differential swing is set to 1.2 V. When the sink displays the video image without pixel errors for each step and the minimum voltage level is lower than or equal to 150 mV, the test is passed; else, the test is failed.

Connection Diagram

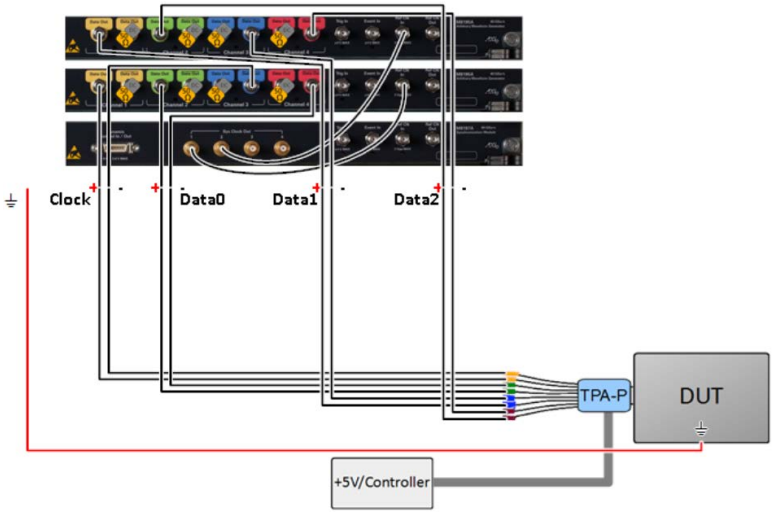


Figure 51 Example connection diagram for Sink tests

CAUTION Ensure that you connect the AXI Frame ground to the DUT ground before connecting the TPA to the DUT (in case the TV does not contain a GND pin). Otherwise there is a risk of permanently damaging the AWG.

Result Description

ID 8-5 D.Swing All_3.3 on All

[Not Compliant]

----General----	
Offline	True
Software Version	1.3.0
Calibration Data Version	Unknown; '1.3.0
Compliant	False
Non-compliance reason(s)	Procedure offline; Software st Calibration Clock-, Swing Cali Data1+, Swing Calibration Data Clock+, Swing Calibration Data
Video Mode	64: 1920x1080p @ 100 Hz
Color Depth	24 bit
Color Space	RGB full range
Use Color Bar pattern	False

Start Differential Swing	170 mV
Minimum Differential Swing	70 mV
Differential Swing Step Size	10 mV
Voltage Offset	3.3 V
TMDS data to clock ratio 1:40	False
Use scrambled video signal	False
User Name	Unknown User
----M8195A - HDMI Sig. Gen.----	
DVI Mode	False
Fill up blanking periods with Null packets	False
Keep the signals after test?	False
Skip Pattern generation	True
----SCDC Controller----	
SCDC supports Character Error Detections	False
Skip Link Training	False
Start delay between SCDC controller and TMDS signal	100 ms
----Dso----	
Use internal probe head termination voltage	True

Result	Channel	Min Passed Diff. Swing [mV]	Min Spec Diff. Swing [mV]	Max Swing Test [V]
pass	All	120	150	1.200

Figure 52 Example result for Test ID 8-5: Differential Swing

- Result: (Pass/Fail) Pass indicates that the DUT passed this test step successfully.
- Channel: The TMDS line where the voltage level is applied.
- Min Passed Diff. Swing [mV]: The minimum differential swing when the DUT passed.
- Min Spec Diff. Swing [mV]: The required minimum differential swing voltage level (optionally defined through user-specification instead of CTS).
- Max Swing Test [V]: The maximum applied differential swing voltage level.

ID 8-6 Intra-Pair Skew

Availability

- HDMI 1.4
- Compliance Mode, Expert Mode
- Data0, Data1, Data2, Clock Channel

Purpose and Method

This procedure tests for compliance according to HDMI CTS Version 1.4b, Section 8.3 “Sink – Electrical”, Test ID 8-6: “TMDS – Intra-Pair Skew”. Any Sink-supported video signal with the highest supported data rate is generated with single-ended swing of 500 mV.

For each of the TMDS clock and data pairs, the intra-pair skew is increased from a value less than or equal to 0.1 TBit up to 0.6 TBit or until errors are displayed in the Sink DUT output. This process is performed once each in the positive and in the negative skew directions. If errors are seen on the DUT, the skew is reduced until the Sink DUT returns an error-free output.

The test is considered as passed when the Sink displays the video image without pixel errors for intra-pair skew level as required by the HDMI CTS; otherwise, the test is considered to be failed.

Connection Diagram

Refer to Figure 51 on page 116.

Result Description

ID 8-6: Intra-Pair Skew Data0

[Not Compliant]

----General----	
Offline	True
Software Version	1.3.0
Calibration Data Version	Unknown; '1.3.0
Compliant	False
Non-compliance reason(s)	Procedure offline; Software st Fall/Rise Time Calibration
Video Mode	02: 720x480p @ 60 Hz
Color Depth	24 bit
Color Space	RGB full range
Use Color Bar pattern	False
TMDS data to clock ratio 1:40	False
Use scrambled video signal	False
Minimum Skew	-600 mTBit
Maximum Skew	600 mTBit
Skew Step Size	100 mTBit
User Name	Unknown User
----M8195A - HDMI Sig. Gen.----	
DVI Mode	False
Fill up blanking periods with Null packets	False
Keep the signals after test?	False
Skip Pattern generation	True
----SCDC Controller----	
SCDC supports Character Error Detections	False
Skip Link Training	False
Start delay between SCDC controller and TMDS signal	100 ms
----Dso----	
Use internal probe head termination voltage	True

Result	Channel	Max Passed Skew [mTBit]	Min Failed Skew [mTBit]	Max Recovery Skew [mTBit]	Spec. Skew [mTBit]
pass	Data0+	600	N/A	N/A	400
pass	Data0-	-600	N/A	N/A	400

Figure 53 Example result for Test ID 8-6: Intra-Pair Skew

- Result: (Pass/Fail) Pass indicates that the DUT passed this test step successfully.
- Channel: The TMDS line where the intra-pair skew is applied.
- Max Passed Skew [mTBit]: The maximum passed value of skew for which the DUT shows no errors in the output.
- Min Failed Skew [mTBit]: The minimum value of skew for which the DUT shows errors in the output.

- Max Recovery Skew [mTBit]: The maximum value of skew for which the DUT recovered to having no errors in the output errors after errors were seen in the output.
- Spec. Skew [mTBit]: Required minimum skew as defined in the CTS (optionally user-defined spec.).

ID 8-7 Jitter Tolerance

Availability

- HDMI 1.4
- Compliance Mode, Expert Mode

Purpose and Method

The purpose of this procedure is confirm that the maximum allowed value of TMDS clock jitter is supported by the Sink DUT. The test is divided into four parts:

- Jitter only on Clock
- Jitter only on Clock, with a 2nd Cable Emulator
- Jitter on Clock and Data
- Jitter on Clock and Data, with a 2nd Cable Emulator

These procedures test for compliance according to HDMI CTS Version 1.4b, Section 8.3 “Sink – Electrical”, Test ID 8-7: “TMDS – Jitter Tolerance”. Depending on the supported video modes, the pixel clock rates 27 MHz, 74.25 MHz, 148.5 MHz, 222.75 MHz, 297 MHz and optionally, if not already covered, the highest rate supported by the DUT, are tested.

For this procedure, a valid HDMI video signal is generated. Two cases are tested:

- Clock jitter = 10 MHz; Data jitter = 500 kHz
- Clock jitter = 7 MHz; Data jitter = 1 MHz

At each step the software performs a sweep of the clock-to-data skew from 0 TBit to 1 TBit. The test is considered as passed when the Sink displays a video image without any pixel errors for skew levels as required by the HDMI CTS; otherwise, the test is considered as failed.

Connection Diagram

Refer to Figure 51 on page 116.

Result Description

ID 8-7 WVGA60Hz24

[Not Compliant]

Test 8-7, Jitter Tolerance VGA60Hz24 Jitter only on Clock

----General----	
Offline	True
Software Version	1.3.0
Calibration Data Version	Unknown; '1.3.0
Compliant	False
Non-compliance reason(s)	Procedure offline; Software st Calibration TP1 VGA60Hz24, Dat offline: Skew Calibration, Fal VGA60Hz24, Clock Jitter Calibr Calibration Clock+, Swing Calil Calibration Data1+, Swing Calil
Video Mode	01: 640x480p @ 60 Hz
Color Depth	24 bit
Color Space	RGB full range
Use Color Bar pattern	False
Desired Skew Accuracy	100 mTBit
Differential Swing	800 mV
Clock Jitter Margin	0 TBit
Data Jitter Margin	0 TBit
Margin Search	None
Initial Margin Step Size	100 mTBit
Margin Accuracy	10 mTBit
Cable Emulator	Cat 1 and 2
User Name	Unknown User
----M8195A - HDMI Sig. Gen.----	
DVI Mode	False
Fill up blanking periods with Null packets	False
Keep the signals after test?	False
Skip Pattern generation	True
----SCDC Controller----	
SCDC supports Character Error Detections	False
Skip Link Training	False
Start delay between SCDC controller and TMDS signal	100 ms
----Dso----	
Use internal probe head termination voltage	True

Result	Clock Jitter Amplitude [TBit]	Clock Jitter Frequency [MHz]	Data Jitter Amplitude [TBit]	Data Jitter Frequency [MHz]	Failed Skew	Tested Data Jitter Margin [TBit]	Tested Clock Jitter Margin [TBit]
pass	0.203	10.0	0.190	0.5	N/A	0.000	0.000
pass	0.227	7.0	0.190	1.0	N/A	0.000	0.000

Figure 54 Example result for Test ID 8-7: Jitter Tolerance

- Result: (Pass/Fail) Pass indicates that the DUT passed this test step successfully.

- Clock Jitter Amplitude [TBit]: Initial clock jitter amplitude (without added data jitter).
- Clock Jitter Frequency [MHz]: The clock jitter frequency that is applied.
- Data Jitter Amplitude [TBit]: Calibrated data jitter amplitude that is added to the clock lane.
- Data Jitter Frequency [MHz]: The data jitter frequency that is applied to the clock lane.
- Failed Skew: Skew value where DUT failed.
- Tested Data Jitter Margin [TBit]: Margin of the data jitter relative to the specification limit.
- Tested Clock Jitter Margin [TBit]: Margin of the clock jitter relative to the specification limit.

HDMI 2.1 TMDS Signal

ID HF2-1 Differential Swing

Availability

- HDMI 2.1 TMDS
- Compliance Mode, Expert Mode
- All Channels
- Minimum swing, Maximum swing

Purpose and Method

This procedure tests for compliance according to HDMI Sink CTS Version 2.1i, Section 5.1.1.1 “Sink TMDS Electrical 6G Tests”, HF2-1: “Sink TMDS Electrical – 6G – Min/Max Differential Swing Tolerance” and “HF2-1 Keysight MOI v1.0c”.

A video signal at the highest supported data rate is generated with calibrated voltage levels and with no jitter applied. This procedure is performed for minimum and maximum swing levels.

For minimum swing, the differential swing voltage is fixed at150 mV and the V_{ICM} is set to 3.1 V. Then, the V_{ICM} is changed to 3.3 V.

For maximum swing, the differential swing voltage is fixed at 1200 mV and the V_{ICM} is set to 2.6 V. Then, the V_{ICM} is changed to 3.3 V.

The test is considered as passed when, for each step, the Sink displays the video image without pixel errors; else, the test is considered as failed.

In Expert mode, the procedure can be used for the characterization of the DUT by changing the “Start Differential Swing” value and the step size. In this case, the differential swing voltage level is decreased from the start value until the DUT fails to support the signal without errors.

This test must be conducted for the highest supported data rate above 340 Mcsc.

Connection Diagram

Refer to Figure 51 on page 116.

Result Description

ID HF2-1 min D.Swing All on All

[Not Compliant]

----General----	
Offline	True
Software Version	1.3.0
Calibration Data Version	Unknown; '1.3.0
Compliant	False
Non-compliance reason(s)	Procedure offline; Software st Swing Calibration Clock-, HF S Swing Calibration Data1+, HF S Calibration, HF Swing Calibrat Data2-
Video Mode	96: 3840x2160p @ 50 Hz
Color Depth	24 bit
Color Space	RGB full range
Use Color Bar pattern	False
TMDS data to clock ratio 1:40	True
Use scrambled video signal	True
Start Differential Swing	170 mV
Minimum Differential Swing	100 mV
Differential Swing Step Size	10 mV
Voltage Offset	3.1 V
User Name	Unknown User
----M8195A - HDMI Sig. Gen.----	
DVI Mode	False
Fill up blanking periods with Null packets	False
Keep the signals after test?	False
Skip Pattern generation	True
----SCDC Controller----	
SCDC supports Character Error Detections	False
Skip Link Training	False
Start delay between SCDC controller and TMDS signal	100 ms
----Dso----	
Use internal probe head termination voltage	True

Result	Vicm	Passed Diff. Swing [mV]	Spec Diff. Swing [mV]
pass	V_icm1 (3.1V)	100	150
pass	V_icm2 (3.3V)	100	150

Figure 55 Example result for Test ID HF2-1: Differential Swing

- Result: (Pass/Fail) Test is considered as passed if the DUT displays the video image without pixel errors.
- Vicm: The common mode input voltage level applied.
- Passed Diff. Swing [mV]: The minimum differential swing when the DUT passed.
- Spec Diff. Swing: The required differential swing voltage level (optionally defined through user-spec instead of CTS).

ID HF2-2 Intra-Pair Skew

Availability

- HDMI 2.1 TMDS
- Compliance Mode, Expert Mode
- Data0, Data1, Data2, Clock

Purpose and Method

This procedure tests for compliance according to HDMI Sink CTS Version 2.1i, Section 5.1.1.1 “Sink TMDS Electrical 6G Tests”, HF2-2: “Sink TMDS Electrical – 6G – Intra-Pair Skew” and “HF2-2 Keysight MOI v1.0c”.

For each of the TMDS clock and data pairs, the intra-pair skew is set to the worst case value, that is (112 ps + skew amount), as required in the MOI (which depends on the data rate). The skew must be applied once on the TMDS positive line and once on the TMDS negative line. Therefore, the procedure must be run twice for each signal path.

The DUT is tested first for V_{ICM} = 2.8 V and then for V_{ICM} = 3.3 V.

The test is considered as passed when the Sink displays the video image without pixel errors for the intra-pair skew level required by the HDMI CTS; otherwise, the test is considered as failed.

This test must be conducted for the highest supported data rate above 340 Mcsc.

Connection Diagram

Refer to Figure 51 on page 116.

Result Description

ID HF2-2 3840x2160p50Hz24 Data0

[Not Compliant]

----General----	
Offline	True
Software Version	1.3.0
Calibration Data Version	Unknown; '1.3.0
Compliant	False
Non-compliance reason(s)	Procedure offline; Software st. Swing Calibration Clock-, HF S Swing Calibration Data1+, HF S Calibration, HF Swing Calibrat. Data2-
Video Mode	96: 3840x2160p @ 50 Hz
Color Depth	24 bit
Color Space	RGB full range
Use Color Bar pattern	False
Voltage offset, Vicm1	2.8 V
Voltage offset, Vicm2	3.3 V
TMDS data to clock ratio 1:40	True
Use scrambled video signal	True
Skew	695 mTBit
Skew in ps	117 ps
Cable Emulator	HDMI 2 0 NO SKEW
User Name	Unknown User
----M8195A - HDMI Sig. Gen.----	
DVI Mode	False
Fill up blanking periods with Null packets	False
Keep the signals after test?	False
Skip Pattern generation	True
----SCDC Controller----	
SCDC supports Character Error Detections	False
Skip Link Training	False
Start delay between SCDC controller and TMDS signal	100 ms
----Dso----	
Use internal probe head termination voltage	True

Result	Channel	Passed Skew [mTBit]	Failed Skew [mTBit]	Spec. Skew [mTBit]	Vicm [V]
pass	Data0	695	N/A	695	2.8
pass	Data0	-695	N/A	-695	2.8
pass	Data0	695	N/A	695	3.3
pass	Data0	-695	N/A	-695	3.3

Figure 56 Example result for Test ID HF2-2: Intra-Pair Skew

- Result: (Pass/Fail) Pass indicates that the DUT passed this test step successfully.
- Channel: The TMDS line where the intra-pair skew is applied.

- Passed Skew [mTBit]: The maximum value of skew that has passed for which the DUT shows no errors in the output.
- Failed Skew [mTBit]: The minimum value of skew for which the DUT shows errors in the output.
- Spec. Skew [mTBit]: Required minimum skew as defined in the CTS.
- Vicm [V]: Common mode input voltage level.

ID HF2-51 Inter-Pair Screw

Availability

- HDMI 2.1 TMDS
- Compliance Mode, Expert Mode
- Data0, Data1, Data2
- V_{ICM} = 2.8 V, 3.3 V

Purpose and Method

The test ID HF2-51: “Sink TMDS Electrical – Inter-Pair Skew” was introduced in revision 2.1g of the GCTS.

This test confirms that the maximum allowed inter-pair skew between two TMDS data lanes, as defined by the CTS, is supported by the sink DUT.

The DUT is tested first for V_{ICM} = 2.8 V and then for V_{ICM} = 3.3 V.

The test is considered as passed if the Sink displays the video image without pixel errors for the inter-pair skew level required by the HDMI CTS; otherwise, the test is considered as failed.

This test must be conducted at the highest TMDS character rate supported by the DUT.

Connection Diagram

Refer to Figure 51 on page 116.

Result Description

ID HF2-51 3840x2160p50Hz24 Data0

[Not Compliant]

----General----	
Offline	True
Software Version	1.3.0
Calibration Data Version	Unknown; '1.3.0
Compliant	False
Non-compliance reason(s)	Procedure offline; Software st Swing Calibration Clock-, HF S Swing Calibration Data1+, HF S Calibration, HF Swing Calibrat Data2-; Non-Default values: 'T
Video Mode	96: 3840x2160p @ 50 Hz
Color Depth	24 bit
Color Space	RGB full range
Use Color Bar pattern	False

Voltage offset, Vicm1	2.8 V
Voltage offset, Vicm2	3.3 V
TMDS data to clock ratio 1:40	True
Use scrambled video signal	True
Skew	12.573 TBit
Skew in ps	2117 ps
User Name	Unknown User
----M8195A - HDMI Sig. Gen.----	
DVI Mode	False
Fill up blanking periods with Null packets	False
Keep the signals after test?	False
Skip Pattern generation	True
----SCDC Controller----	
SCDC supports Character Error Detections	False
Skip Link Training	False
Start delay between SCDC controller and TMDS signal	100 ms
----Dso----	
Use internal probe head termination voltage	True

Result	Channel	Spec. Skew [mTBit]	Vicm [V]
pass	Data0	12573	2.8
pass	Data0	12573	3.3

Figure 57 Example result for Test ID HF2-51: Inter-Pair Skew

- Result: (Pass/Fail) Pass indicates that the DUT passed this test step successfully.
- Channel: The TMDS line where the inter-pair skew is measured.
- Spec. Skew [mTBit]: Required minimum skew as defined in the CTS.
- Vicm [V]: Common mode input voltage level.

ID HF2-3 Jitter Tolerance

Availability

- HDMI 2.1 TMDS
- Compliance Mode, Expert Mode

Purpose and Method

This procedure tests for compliance according to HDMI Sink CTS Version 2.1i, Chapter 5.1.1.1 “Sink TMDS Electrical 6G Tests”, HF2-3: “Sink TMDS Electrical – 6G – Jitter Tolerance” and “HF2-3 Keysight MOI v1.0c”. Here, the software tests for the highest supported data rate above 340 Mcsc.

For this procedure, a valid HDMI video signal is generated. The differential swing is set to 800 mV. Data jitter and Clock jitter are applied to the TMDS clock signal. Two jitter frequency pairs are tested:

- Clock jitter = 10 MHz; Data jitter = 500 kHz
- Clock jitter = 7 MHz; Data jitter = 1 MHz

For each jitter pair, two distinct common mode offsets (2.9 V and 3.3 V) are tested. Additionally, the worst cable model is applied using a software emulator.

The test is run with 112 ps intra-pair skew delay on each TMDS Data line, once on all TMDS Data positive lines and once on all TMDS Data negative lines.

The test is considered as passed if the DUT adequately supports the transmitted image; else, the test is failed.

Connection Diagram

Refer to Figure 51 on page 116.

Result Description

ID HF2-3 3840x2160p50Hz24 (skew on +)

[Not Compliant]

Test HF2-3, Jitter Tolerance 3840x2160p50Hz24

----General----	
Offline	True
Software Version	1.3.0
Calibration Data Version	Unknown; '1.3.0
Compliant	False
Non-compliance reason(s)	Procedure offline; Software status unreleased Clock Jitter Calibration TP2 3840x2160p50Hz24 cal offline: Skew Calibration, Fall/Rise Time Calibration TP2 skew on normal (+) 3840x2160p Calibration, HF Swing Calibration Clock+, HF 3840x2160p50Hz24, HF Swing Calibration Data1+
Video Mode	96: 3840x2160p @ 50 Hz
Color Depth	24 bit
Color Space	RGB full range
Use Color Bar pattern	False
Differential Swing	800 mV
Clock Jitter Margin	0 TBit
Data Jitter Margin	0 TBit
Margin Search	None
Initial Margin Step Size	100 mTBit
Margin Accuracy	10 mTBit
Min Voltage Offset	2.9 V
Max Voltage Offset	3.3 V
TMDS data to clock ratio 1:40	True
Cable Emulator	HDMI 2 0 NO SKEW
Use scrambled video signal	True
User Name	Unknown User
----M8195A - HDMI Sig. Gen.----	
DVI Mode	False
Fill up blanking periods with Null packets	False
Keep the signals after test?	False
Skip Pattern generation	True
----SCDC Controller----	
SCDC supports Character Error Detections	False
Skip Link Training	False
Start delay between SCDC controller and TMDS signal	100 ms
----Dso----	
Use internal probe head termination voltage	True

Result	Clock Jitter Amplitude [TBit]	Clock Jitter Frequency [MHz]	Data Jitter Amplitude [TBit]	Data Jitter Frequency [MHz]	Tested Data Jitter Margin [TBit]	Tested Clock Jitter Margin [TBit]	Common Mode Voltage Offset [V]
pass	0.201	10.0	0.190	0.5	0.000	0.000	2.9
pass	0.201	10.0	0.190	0.5	0.000	0.000	3.3
pass	0.218	7.0	0.190	1.0	0.000	0.000	2.9
pass	0.218	7.0	0.190	1.0	0.000	0.000	3.3

Figure 58 Example result for Test ID HF2-3: Jitter Tolerance

- Result: (Pass/Fail) Pass indicates that the DUT passed this test step successfully.
- Clock Jitter Amplitude [TBit]: The clock jitter amplitude that is applied.
- Clock Jitter Frequency [MHz]: The clock jitter frequency that is applied.
- Data Jitter Amplitude [TBit]: The data jitter amplitude applied.
- Data Jitter Frequency [MHz]: The data jitter frequency applied.
- Tested Data Jitter Margin [TBit]: Margin of the data jitter relative to the specification limit.
- Tested Clock Jitter Margin: Margin of the clock jitter relative to the specification limit.
- Common Mode Voltage Offset [V]: V_{icm}.

ID HF2-6 Video Timing 2160p 24bit

Availability

- HDMI 2.1 TMDS
- Compliance Mode, Expert Mode

Purpose and Method

This procedure tests for compliance according to HDMI Sink CTS Version 2.1, Section 5.1.4.1 “Sink Video Timing 6G Tests”, HF2-6: “Sink Video Timing - 6G - 2160p 24-bit Color Depth” and “HF2-6 Keysight MOI v1.0c”.

This procedure tests for a limited set of video formats (only 2160p), which are supported by the DUT and have a data rate above 340 Mcsc.

Each supported video format is run with a color depth of 24 bit. A valid HDMI video signal is generated and for each tested video format, the pixel clock frequency is deviated to minimum and maximum as described in the CTS (typically, ±0.5%).

The test is considered as passed if the DUT adequately supports the transmitted image; else, the test is considered as failed.

Connection Diagram

Refer to Figure 51 on page 116.

Result Description

ID HF2-6: Video Timing 2160p 24bit

[Not Compliant]

----General----	
Offline	True
Software Version	1.3.0
Calibration Data Version	Unknown; '1.3.0
Compliant	False
Non-compliance reason(s)	Procedure offline; Software st Fall/Rise Time Calibration
TMDS data to clock ratio 1:40	True
User Name	Unknown User
----M8195A - HDMI Sig. Gen.----	
DVI Mode	False
Fill up blanking periods with Null packets	False
Keep the signals after test?	False
Skip Pattern generation	True
----SCDC Controller----	
SCDC supports Character Error Detections	False
Skip Link Training	False
Start delay between SCDC controller and TMDS signal	100 ms
----Dso----	
Use internal probe head termination voltage	True

Result	Video Mode
pass	96: 3840x2160p @ 50 Hz _24_bit RGB_full_range (max frequency 5
pass	96: 3840x2160p @ 50 Hz _24_bit RGB_full_range (min frequency 4
pass	97: 3840x2160p @ 60 Hz _24_bit RGB_full_range (max frequency 6
pass	97: 3840x2160p @ 60 Hz _24_bit RGB_full_range (min frequency 5
pass	97: 3840x2160p @ 59.94 Hz _24_bit RGB_full_range (max frequency
pass	97: 3840x2160p @ 59.94 Hz _24_bit RGB_full_range (min frequency
pass	101: 4096x2160p @ 50 Hz _24_bit RGB_full_range (max frequency 5
pass	101: 4096x2160p @ 50 Hz _24_bit RGB_full_range (min frequency 4
pass	102: 4096x2160p @ 60 Hz _24_bit RGB_full_range (max frequency
pass	102: 4096x2160p @ 60 Hz _24_bit RGB_full_range (min frequency 5
pass	102: 4096x2160p @ 59.94 Hz _24_bit RGB_full_range (max frequency
pass	102: 4096x2160p @ 59.94 Hz _24_bit RGB_full_range (min frequency
pass	Test Result

Figure 59 Example result for Test ID HF2-6: Video Timing 2160p

- Result: (Pass/Fail) Pass indicates that the DUT passed this test step successfully.
- Video Mode: The tested video mode. The final entry, “Test Result”, is for the entire test.

ID HF2-7 Video Timing 2160p Deep Color

Availability

- HDMI 2.1 TMDS
- Compliance Mode, Expert Mode
- Color Depth 30 bit, 36 bit, 48 bit
- Data rate between 340 and 600 Mcsc

Purpose and Method

This procedure tests for compliance according to HDMI Sink CTS Version 2.1i, Section 5.1.4.1 “Sink Video Timing 6G Tests”, HF2-7: “Sink Video Timing – 6G – 2160p Deep Color” and “HF2-7 Keysight MOI v1.0c”.

This procedure tests for a limited set of video formats (only 2160p), which are supported by the DUT and have a data rate above 340 Mcsc.

The test is run at each supported color depth other than 24 bit. A valid HDMI video signal is generated and for each tested video format and color depth, the pixel clock frequency is deviated to minimum and maximum as described in the CTS (typically, ±0.5%).

The test is considered as passed if the DUT adequately supports the transmitted image; else, the test is considered as failed.

Connection Diagram

Refer to Figure 51 on page 116.

Result Description

ID HF2-7: Deep Color

[Not Compliant]

----General----	
Offline	True
Software Version	2023
Calibration Data Version	Unknown; '1.3.0
Compliant	False
Non-compliance reason(s)	Procedure offline; Software st Fall/Rise Time Calibration
gCTS Revision	2.1h
MOI Revision	v1c
TMDS data to clock ratio 1:40	True
User Name	Unknown User

----M8195A - HDMI Sig. Gen.----	
DVI Mode	False
Fill up blanking periods with Null packets	False
Keep the signals after test?	False
Skip Pattern generation	True
----SCDC Controller----	
SCDC supports Character Error Detections	False
Skip Link Training	False
Start delay between SCDC controller and TMDS signal	100 ms
----Dso----	
Use internal probe head termination voltage	True

Result	Video Mode
pass	63: 1920x1080p @ 120 Hz _36_bit RGB_full_range (max frequency 120.6 Hz)
pass	63: 1920x1080p @ 120 Hz _36_bit RGB_full_range (min frequency 119.4 Hz)
pass	63: 1920x1080p @ 119.88 Hz _36_bit RGB_full_range (max frequency 120.6 Hz)
pass	63: 1920x1080p @ 119.88 Hz _36_bit RGB_full_range (min frequency 119.4 Hz)
pass	64: 1920x1080p @ 100 Hz _36_bit RGB_full_range (max frequency 100.5 Hz)
pass	64: 1920x1080p @ 100 Hz _36_bit RGB_full_range (min frequency 99.5 Hz)
pass	93: 3840x2160p @ 24 Hz _36_bit RGB_full_range (max frequency 24.12 Hz)
pass	93: 3840x2160p @ 24 Hz _36_bit RGB_full_range (min frequency 23.86 Hz)
pass	93: 3840x2160p @ 23.98 Hz _36_bit RGB_full_range (max frequency 24.12 Hz)
pass	93: 3840x2160p @ 23.98 Hz _36_bit RGB_full_range (min frequency 23.86 Hz)
pass	94: 3840x2160p @ 25 Hz _36_bit RGB_full_range (max frequency 25.12 Hz)
pass	94: 3840x2160p @ 25 Hz _36_bit RGB_full_range (min frequency 24.88 Hz)
pass	95: 3840x2160p @ 30 Hz _36_bit RGB_full_range (max frequency 30.15 Hz)
pass	95: 3840x2160p @ 30 Hz _36_bit RGB_full_range (min frequency 29.82 Hz)
pass	95: 3840x2160p @ 29.97 Hz _36_bit RGB_full_range (max frequency 30.15 Hz)
pass	95: 3840x2160p @ 29.97 Hz _36_bit RGB_full_range (min frequency 29.82 Hz)
pass	98: 4096x2160p @ 24 Hz _36_bit RGB_full_range (max frequency 24.12 Hz)
pass	98: 4096x2160p @ 24 Hz _36_bit RGB_full_range (min frequency 23.86 Hz)
pass	98: 4096x2160p @ 23.98 Hz _36_bit RGB_full_range (max frequency 24.12 Hz)
pass	98: 4096x2160p @ 23.98 Hz _36_bit RGB_full_range (min frequency 23.86 Hz)
pass	99: 4096x2160p @ 25 Hz _36_bit RGB_full_range (max frequency 25.12 Hz)
pass	99: 4096x2160p @ 25 Hz _36_bit RGB_full_range (min frequency 24.88 Hz)
pass	100: 4096x2160p @ 30 Hz _36_bit RGB_full_range (max frequency 30.15 Hz)
pass	100: 4096x2160p @ 30 Hz _36_bit RGB_full_range (min frequency 29.82 Hz)
pass	100: 4096x2160p @ 29.97 Hz _36_bit RGB_full_range (max frequency 30.15 Hz)
pass	100: 4096x2160p @ 29.97 Hz _36_bit RGB_full_range (min frequency 29.82 Hz)
pass	Test Result

Figure 60 Example result for Test ID HF2-7: Video Timing 2061p Deep Color

- Result: (Pass/Fail) Pass indicates that the DUT passed this test step successfully.
- Video Mode: Tested Video mode. The final entry, “Test Result”, is for the entire test.

ID HF2-8 Video Timing 2160p 3D

Availability

- HDMI 2.1 TMDS
- Compliance Mode, Expert Mode

Purpose and Method

This procedure tests for compliance according to HDMI Sink CTS Version 2.1i, Section 5.1.4.1 “Sink Video Timing 6G Tests”, HF2-8: “Sink Video Timing – 6G – 2160p 3D” and the “HF2.8 Keysight MOI v1.0c”.

This procedure tests for a limited set of video formats (only 2160p) and 3D modes, which are supported by the DUT and have a data rate above 340 Mcsc.

Each supported video format is run with a color depth of 24 bit. A valid HDMI video signal is generated and for each tested video format, the pixel clock frequency is deviated to minimum and maximum as described in the CTS (typically, ±0.5%).

The test is considered as passed if the DUT adequately supports the transmitted image; else, the test is considered as failed.

Connection Diagram

Refer to Figure 51 on page 116.

Result Description

ID HF2-8: Video Timing 2160p 3D

[Not Compliant]

----General----	
Offline	True
Software Version	1.3.0
Calibration Data Version	Unknown; '1.3.0
Compliant	False
Non-compliance reason(s)	Procedure offline; Software st Fall/Rise Time Calibration
TMDS data to clock ratio 1:40	True
User Name	Unknown User
----M8195A - HDMI Sig. Gen.----	
DVI Mode	False
Fill up blanking periods with Null packets	False
Keep the signals after test?	False
Skip Pattern generation	True
----SCDC Controller----	
SCDC supports Character Error Detections	False
Skip Link Training	False
Start delay between SCDC controller and TMDS signal	100 ms
----Dso----	
Use internal probe head termination voltage	True

Result	Video Mode
pass	93: 3840x2160p @ 24 Hz _24_bit RGB_limited_range FramePacking (max frequency 24.12 Hz)
pass	93: 3840x2160p @ 24 Hz _24_bit RGB_limited_range FramePacking (min frequency 23.86 Hz)
pass	93: 3840x2160p @ 23.98 Hz _24_bit RGB_limited_range FramePacking (max frequency 24.12 Hz)
pass	93: 3840x2160p @ 23.98 Hz _24_bit RGB_limited_range FramePacking (min frequency 23.86 Hz)
pass	94: 3840x2160p @ 25 Hz _24_bit RGB_limited_range FramePacking (max frequency 25.12 Hz)
pass	94: 3840x2160p @ 25 Hz _24_bit RGB_limited_range FramePacking (min frequency 24.88 Hz)
pass	95: 3840x2160p @ 30 Hz _24_bit RGB_limited_range FramePacking (max frequency 30.15 Hz)
pass	95: 3840x2160p @ 30 Hz _24_bit RGB_limited_range FramePacking (min frequency 29.82 Hz)
pass	95: 3840x2160p @ 29.97 Hz _24_bit RGB_limited_range FramePacking (max frequency 30.15 Hz)
pass	95: 3840x2160p @ 29.97 Hz _24_bit RGB_limited_range FramePacking (min frequency 29.82 Hz)
pass	98: 4096x2160p @ 24 Hz _24_bit RGB_limited_range FramePacking (max frequency 24.12 Hz)
pass	98: 4096x2160p @ 24 Hz _24_bit RGB_limited_range FramePacking (min frequency 23.86 Hz)
pass	98: 4096x2160p @ 23.98 Hz _24_bit RGB_limited_range FramePacking (max frequency 24.12 Hz)
pass	98: 4096x2160p @ 23.98 Hz _24_bit RGB_limited_range FramePacking (min frequency 23.86 Hz)
pass	99: 4096x2160p @ 25 Hz _24_bit RGB_limited_range FramePacking (max frequency 25.12 Hz)

pass	99: 4096x2160p @ 25 Hz _24_bit RGB_limited_range FramePacking (min frequency 24.88 Hz)
pass	100: 4096x2160p @ 30 Hz _24_bit RGB_limited_range FramePacking (max frequency 30.15 Hz)
pass	100: 4096x2160p @ 30 Hz _24_bit RGB_limited_range FramePacking (min frequency 29.82 Hz)
pass	100: 4096x2160p @ 29.97 Hz _24_bit RGB_limited_range FramePacking (max frequency 30.15 Hz)
pass	100: 4096x2160p @ 29.97 Hz _24_bit RGB_limited_range FramePacking (min frequency 29.82 Hz)
pass	Test Result

Figure 61 Example result for Test ID HF2-8: Video Timing 2160p 3D

- Result: (Pass/Fail) Pass indicates that the DUT passed this test step successfully.
- Video Mode: The tested video mode. The final entry, “Test Result”, is for the entire test.

ID HF2-23 Pixel Decoding YCbCr 4:2:0

Availability

- HDMI 2.1 TMDS
- Compliance Mode, Expert Mode
- Color Depth 24 bit
- Color Space YCbCr 4:2:0 (four varieties available)

Purpose and Method

This procedure tests for compliance according to HDMI Sink CTS Version 2.1i, Section 5.1.3.1 “Sink YC_BC_R 4:2:0 Pixel Decoding Tests”, HF2-23: “Sink Pixel Decoding - YC_BC_R 4:2:0” and “HF2-23 Keysight MOI v1.0c”.

This procedure tests whether a DUT appropriately supports YC_BC_R 4:2:0 pixel encoding and signaling.

For each supported YC_BC_R pixel encoded video format, which is supported by the DUT as shown in its EDID, the video signal is generated and transmitted. Each video format is tested at two pixel clock frequencies: –0.5% (or –0.6% when the frame-rate is 60 Hz) and +0.5%.

The test is considered as passed if the DUT adequately shows the image at each pixel clock frequency and for each video format; else, the test is considered as failed.This test covers 24-bit color depth only.

Connection Diagram

Refer to Figure 51 on page 116.

Result Description

ID HF2-23: Pixel Decoding YCbCr 4:2:0

[Not Compliant]

----General----	
Offline	True
Software Version	2023
Calibration Data Version	Unknown; '1.3.0
Compliant	False
Non-compliance reason(s)	Procedure offline; Software st Fall/Rise Time Calibration
gCTS Revision	2.1h
MOI Revision	v1c
Use seperated YCbCr 4:2:0 test images	False
User Name	Unknown User

----M8195A - HDMI Sig. Gen.----	
DVI Mode	False
Fill up blanking periods with Null packets	False
Keep the signals after test?	False
Skip Pattern generation	True
----SCDC Controller----	
SCDC supports Character Error Detections	False
Skip Link Training	False
Start delay between SCDC controller and TMDS signal	100 ms
----Dso----	
Use internal probe head termination voltage	True

Result	Video Mode
pass	96: 3840x2160p @ 50 Hz YCbCr420_709_limited_range _24_bit (max frequency 50.25 Hz)
pass	96: 3840x2160p @ 50 Hz YCbCr420_709_limited_range _24_bit (min frequency 49.75 Hz)
pass	97: 3840x2160p @ 60 Hz YCbCr420_709_limited_range _24_bit (max frequency 60.3 Hz)
pass	97: 3840x2160p @ 60 Hz YCbCr420_709_limited_range _24_bit (min frequency 59.64 Hz)
pass	97: 3840x2160p @ 59.94 Hz YCbCr420_709_limited_range _24_bit (max frequency 59.29 Hz)
pass	97: 3840x2160p @ 59.94 Hz YCbCr420_709_limited_range _24_bit (min frequency 58.7 Hz)
pass	101: 4096x2160p @ 50 Hz YCbCr420_709_limited_range _24_bit (max frequency 50.25 Hz)
pass	101: 4096x2160p @ 50 Hz YCbCr420_709_limited_range _24_bit (min frequency 49.75 Hz)
pass	102: 4096x2160p @ 60 Hz YCbCr420_709_limited_range _24_bit (max frequency 60.3 Hz)
pass	102: 4096x2160p @ 60 Hz YCbCr420_709_limited_range _24_bit (min frequency 59.64 Hz)
pass	102: 4096x2160p @ 59.94 Hz YCbCr420_709_limited_range _24_bit (max frequency 59.29 Hz)
pass	102: 4096x2160p @ 59.94 Hz YCbCr420_709_limited_range _24_bit (min frequency 58.7 Hz)
pass	106: 3840x2160p @ 50 Hz YCbCr420_709_limited_range _24_bit (max frequency 50.25 Hz)
pass	106: 3840x2160p @ 50 Hz YCbCr420_709_limited_range _24_bit (min frequency 49.75 Hz)
pass	107: 3840x2160p @ 60 Hz YCbCr420_709_limited_range _24_bit (max frequency 60.3 Hz)
pass	107: 3840x2160p @ 60 Hz YCbCr420_709_limited_range _24_bit (min frequency 59.64 Hz)
pass	107: 3840x2160p @ 59.94 Hz YCbCr420_709_limited_range _24_bit (max frequency 59.29 Hz)
pass	107: 3840x2160p @ 59.94 Hz YCbCr420_709_limited_range _24_bit (min frequency 58.7 Hz)
pass	Test Result

Figure 62 Example result for Test ID HF2-23: Pixel Decoding YC_BC_R

- Result: (Pass/Fail) Pass indicates that the DUT passed this test step successfully.
- Video Mode: The tested video mode. The final entry, “Test Result”, is for the entire test.

ID HF2-24 Pixel Decoding YCbCr 4:2:0 Deep Color

Availability

- HDMI 2.1 TMDS
- Compliance Mode, Expert Mode
- Color Depth 30 bit, 36 bit, 48 bit
- Color Space YCbCr 4:2:0 (four varieties available)

Purpose and Method

This procedure tests for compliance according to HDMI Sink CTS Version 2.1i, Section 5.1.3.2 “Sink YC_BC_R 4:2:0 Pixel Deep Color Decoding Tests”, HF2-24: “Sink Pixel Decoding - YC_BC_R Deep Color” and “HF2-24 Keysight MOI v1.0c”.

This procedure tests if a DUT appropriately supports YC_BC_R pixel encoding and signaling with deep color content.

For each supported YC_BC_R pixel encoded video format that is supported by the DUT as shown in its EDID, the video signal is generated at each supported color depth.

The test is considered as passed if the DUT adequately shows the image for each tested video format; else, the test is considered as failed.

This test covers only 30-bit, 36-bit, and 48-bit color depth.

Connection Diagram

Refer to Figure 51 on page 116.

Result Description

ID HF2-24: Pixel Decoding YCbCr 4:2:0 Deep Color

[Not Compliant]

----General----	
Offline	True
Software Version	2023
Calibration Data Version	Unknown; '1.3.0
Compliant	False
Non-compliance reason(s)	Procedure offline; Software st Fall/Rise Time Calibration
gCTS Revision	2.1h
MOI Revision	vlc
Use seperated YCbCr 4:2:0 test images	False
User Name	Unknown User
----M8195A - HDMI Sig. Gen.----	
DVI Mode	False
Fill up blanking periods with Null packets	False
Keep the signals after test?	False
Skip Pattern generation	True
----SCDC Controller----	
SCDC supports Character Error Detections	False
Skip Link Training	False
Start delay between SCDC controller and TMDS signal	100 ms
----Dso----	
Use internal probe head termination voltage	True

Result	Video Mode
pass	96: 3840x2160p @ 50 Hz YCbCr420_709_limited_range _36_bit
pass	97: 3840x2160p @ 60 Hz YCbCr420_709_limited_range _36_bit
pass	97: 3840x2160p @ 59.94 Hz YCbCr420_709_limited_range _36_bit
pass	101: 4096x2160p @ 50 Hz YCbCr420_709_limited_range _36_bit
pass	102: 4096x2160p @ 60 Hz YCbCr420_709_limited_range _36_bit
pass	102: 4096x2160p @ 59.94 Hz YCbCr420_709_limited_range _36_bit
pass	106: 3840x2160p @ 50 Hz YCbCr420_709_limited_range _36_bit
pass	107: 3840x2160p @ 60 Hz YCbCr420_709_limited_range _36_bit
pass	107: 3840x2160p @ 59.94 Hz YCbCr420_709_limited_range _36_bit
pass	Test Result

Figure 63 Example result for Test ID HF2-24: Pixel Decoding YCbCr 4:2:0 Deep Color

- Result: (Pass/Fail) Pass indicates that the DUT passed this test step successfully.
- Video Mode: The tested video mode. The final entry, “Test Result”, is for the entire test.

ID HF2-25 Sink Video Timing—21:9 (64:27)

Availability

- HDMI 2.1 TMDS
- Compliance Mode, Expert Mode

Purpose and Method

This procedure tests for compliance according to HDMI Sink CTS Version 2.1i, Section 5.1.4.2 “Sink Video Timing 21:9 (64:27) Video Formats Tests”, HF2-25: “Sink Video Timing – 21:9 (64:27)” and “HF2-25 Keysight MOI v1.0c”.

This procedure tests for a limited set of video formats, which have an aspect ratio of 21:9 (64:27), supported by the DUT.

Each supported video format is run with a color depth of 24 bit. A valid HDMI video signal is generated and for each tested video format, the pixel clock frequency is deviated to minimum and maximum as described in the CTS (typically, ±0.5%).

The test is considered as passed if the DUT adequately supports the transmitted image and the picture is geometrically correct with respect to the aspect ratio; else, the test is considered as failed. This test covers 24-bit color depth only.

Connection Diagram

Refer to Figure 51 on page 116.

Result Description

ID HF2-25: Sink Video Timing – 21:9 (64:27)

[Not Compliant]

----General----	
Offline	True
Software Version	1.3.0
Calibration Data Version	Unknown; '1.3.0
Compliant	False
Non-compliance reason(s)	Procedure offline; Software st. Fall/Rise Time Calibration
Test image	ColorBar
User Name	Unknown User
----M8195A - HDMI Sig. Gen.----	
DVI Mode	False
Fill up blanking periods with Null packets	False
Keep the signals after test?	False
Skip Pattern generation	True
----SCDC Controller----	
SCDC supports Character Error Detections	False
Skip Link Training	False
Start delay between SCDC controller and TMDS signal	100 ms
----Dso----	
Use internal probe head termination voltage	True

Result	Video Mode
pass	60: 1280x720p @ 24 Hz _24_bit RGB_full_range (max frequency 24.12 Hz)
pass	60: 1280x720p @ 24 Hz _24_bit RGB_full_range (min frequency 23.86 Hz)
pass	65: 1280x720p @ 24 Hz _24_bit RGB_full_range (max frequency 24.12 Hz)
pass	65: 1280x720p @ 24 Hz _24_bit RGB_full_range (min frequency 23.86 Hz)
pass	61: 1280x720p @ 25 Hz _24_bit RGB_full_range (max frequency 25.12 Hz)
pass	61: 1280x720p @ 25 Hz _24_bit RGB_full_range (min frequency 24.88 Hz)
pass	66: 1280x720p @ 25 Hz _24_bit RGB_full_range (max frequency 25.12 Hz)
pass	66: 1280x720p @ 25 Hz _24_bit RGB_full_range (min frequency 24.88 Hz)
pass	62: 1280x720p @ 30 Hz _24_bit RGB_full_range (max frequency 30.15 Hz)
pass	62: 1280x720p @ 30 Hz _24_bit RGB_full_range (min frequency 29.82 Hz)
pass	67: 1280x720p @ 30 Hz _24_bit RGB_full_range (max frequency 30.15 Hz)
pass	67: 1280x720p @ 30 Hz _24_bit RGB_full_range (min frequency 29.82 Hz)
pass	19: 1280x720p @ 50 Hz _24_bit RGB_full_range (max frequency 50.25 Hz)
pass	19: 1280x720p @ 50 Hz _24_bit RGB_full_range (min frequency 49.75 Hz)
pass	68: 1280x720p @ 50 Hz _24_bit RGB_full_range (max frequency 50.25 Hz)
pass	68: 1280x720p @ 50 Hz _24_bit RGB_full_range (min frequency 49.75 Hz)
pass	04: 1280x720p @ 60 Hz _24_bit RGB_full_range (max frequency 60.3 Hz)
pass	04: 1280x720p @ 60 Hz _24_bit RGB_full_range (min frequency 59.64 Hz)
pass	69: 1280x720p @ 60 Hz _24_bit RGB_full_range (max frequency 60.3 Hz)
pass	69: 1280x720p @ 60 Hz _24_bit RGB_full_range (min frequency 59.64 Hz)
pass	41: 1280x720p @ 100 Hz _24_bit RGB_full_range (max frequency 100.5 Hz)
pass	41: 1280x720p @ 100 Hz _24_bit RGB_full_range (min frequency 99.5 Hz)
pass	70: 1280x720p @ 100 Hz _24_bit RGB_full_range (max frequency 100.5 Hz)
pass	70: 1280x720p @ 100 Hz _24_bit RGB_full_range (min frequency 99.5 Hz)

...

pass	105: 3840x2160p @ 30 Hz _24_bit RGB_full_range (max frequency 30.15 Hz)
pass	105: 3840x2160p @ 30 Hz _24_bit RGB_full_range (min frequency 29.82 Hz)
pass	96: 3840x2160p @ 50 Hz _24_bit RGB_full_range (max frequency 50.25 Hz)
pass	96: 3840x2160p @ 50 Hz _24_bit RGB_full_range (min frequency 49.75 Hz)
pass	106: 3840x2160p @ 50 Hz _24_bit RGB_full_range (max frequency 50.25 Hz)
pass	106: 3840x2160p @ 50 Hz _24_bit RGB_full_range (min frequency 49.75 Hz)
pass	97: 3840x2160p @ 60 Hz _24_bit RGB_full_range (max frequency 60.3 Hz)
pass	97: 3840x2160p @ 60 Hz _24_bit RGB_full_range (min frequency 59.64 Hz)
pass	107: 3840x2160p @ 60 Hz _24_bit RGB_full_range (max frequency 60.3 Hz)
pass	107: 3840x2160p @ 60 Hz _24_bit RGB_full_range (min frequency 59.64 Hz)
pass	Test Result

Figure 64 Example result for Test ID HF2-25: Sink Video Timing – 21:9 (64:27)

- Result: (Pass/Fail) Pass indicates that the DUT passed this test step successfully.
- Video Mode: The tested video mode. The final entry, “Test Result”, is for the entire test.

ID HF2-36 Video Timing Non-2160p 24bit

Availability

- HDMI 2.1 TMDS
- Compliance Mode, Expert Mode

Purpose and Method

This procedure tests for compliance according to HDMI Sink CTS Version 2.1i, Section 5.1.4.1 “Sink Video Timing 6 Tests”, HF2-6: “Sink Video Timing – 6G – Non-2160p 24-bit Color Depth” and “HF2-36 Keysight MOI v1.0c”.

This procedure tests for a limited set of video formats (only non-2160p formats), which are supported by the DUT and have a data rate above 340 Mcsc.

Each supported video format is run with a color depth of 24 bit. A valid HDMI video signal is generated and for each tested video format, the pixel clock frequency is deviated to minimum and maximum as described in the CTS (typically, ±0.5%).

The test is considered as passed if the DUT adequately supports the transmitted image; else, the test is considered as failed.

Connection Diagram

Refer to Figure 51 on page 116.

Result Description

ID HF2-36: Video Timing non 2160p 24bit

[Not Compliant]

----General----	
Offline	True
Software Version	1.3.0
Calibration Data Version	Unknown; '1.3.0
Compliant	False
Non-compliance reason(s)	Procedure offline; Software st Fall/Rise Time Calibration
TMDS data to clock ratio 1:40	True
User Name	Unknown User
----M8195A - HDMI Sig. Gen.----	
DVI Mode	False
Fill up blanking periods with Null packets	False
Keep the signals after test?	False
Skip Pattern generation	True
----SCDC Controller----	
SCDC supports Character Error Detections	False
Skip Link Training	False
Start delay between SCDC controller and TMDS signal	100 ms
----Dso----	
Use internal probe head termination voltage	True

Result	Video Mode
pass	91: 2560x1080p @ 100 Hz _24_bit RGB_full_range (max frequency 100.5 Hz)
pass	91: 2560x1080p @ 100 Hz _24_bit RGB_full_range (min frequency 99.5 Hz)
pass	92: 2560x1080p @ 120 Hz _24_bit RGB_full_range (max frequency 120.6 Hz)
pass	92: 2560x1080p @ 120 Hz _24_bit RGB_full_range (min frequency 119.4 Hz)
pass	92: 2560x1080p @ 119.88 Hz _24_bit RGB_full_range (max frequency 120.6 Hz)
pass	92: 2560x1080p @ 119.88 Hz _24_bit RGB_full_range (min frequency 119.4 Hz)
pass	Test Result

Figure 65 Example result for Test ID HF2-36: Video Timing non-2160p 24 bit

- Result: (Pass/Fail) Pass indicates that the DUT passed this test step successfully.
- Video Mode: The tested video mode. The final entry, “Test Result”, is for the entire test.

ID HF2-37 Video Timing Non-2160p Deep Color

Availability

- HDMI 2.1 TMDS
- Compliance Mode, Expert Mode
- Color Depth 30 bit, 36 bit, 48 bit
- Data rate between 340 and 600 Mcsc

Purpose and Method

This procedure tests for compliance according to HDMI Sink CTS Version 2.1i, Section 5.1.4.1 “Sink Video Timing 6G Tests”, HF2-37: “Sink Video Timing – 6G – Non-2160p Deep Color” and “HF2-37 Keysight MOI v1.0c”.

This procedure tests for a limited set of video formats (other than 2160p), which are supported by the DUT and have a data rate above 340 Mcsc.

The test is run at each supported color depth other than 24 bit. A valid HDMI video signal is generated and for each tested video format and color depth, the pixel clock frequency is deviated to minimum and maximum as described in the CTS (typically, ±0.5%).

The test is considered as passed if the DUT adequately supports the transmitted image; else, the test is considered as failed.

Connection Diagram

Refer to Figure 51 on page 116.

Result Description

ID HF2-37: Video Timing non 2160p Deep Color

[Not Compliant]

----General----	
Offline	True
Software Version	2023
Calibration Data Version	Unknown; '1.3.0
Compliant	False
Non-compliance reason(s)	Procedure offline; Software st Fall/Rise Time Calibration
gCTS Revision	2.1h
MOI Revision	v1c
TMDS data to clock ratio 1:40	True
User Name	Unknown User
----M8195A - HDMI Sig. Gen.----	
DVI Mode	False
Fill up blanking periods with Null packets	False
Keep the signals after test?	False
Skip Pattern generation	True
----SCDC Controller----	
SCDC supports Character Error Detections	False
Skip Link Training	False
Start delay between SCDC controller and TMDS signal	100 ms
----Dso----	
Use internal probe head termination voltage	True

Result	Video Mode
pass	132: 1920x1080p @ 92 Hz _36_bit RGB_full_range (max frequency 92.46 Hz)
pass	132: 1920x1080p @ 92 Hz _36_bit RGB_full_range (min frequency 91.54 Hz)
pass	Test Result

Figure 66 Example result for Test ID HF2-37: Video Timing non-2160p Deep Color

- Result: (Pass/Fail) Pass indicates that the DUT passed this test step successfully.
- Video Mode: Tested Video mode. The final entry, “Test Result”, is for the entire test.

ID HF2-38 Video Timing Non-2160p 3D

Availability

- HDMI 2.1 TMDS
- Compliance Mode, Expert Mode

Purpose and Method

This procedure tests for compliance according to HDMI Sink CTS Version 2.1i, Section 5.1.4.1 “Sink Video Timing Tests”, HF2-38: “Sink Video Timing - 6G - Non-2160p 3D” and “HF2-38 Keysight MOI v1.0c”.

This procedure tests for a limited set of video formats (only non-2160p formats) and 3D modes, which are supported by the DUT and have a data rate above 340 Mcsc.

Each supported video format is run with a color depth of 24 bit. A valid HDMI video signal is generated and for each tested video format, the pixel clock frequency is deviated to minimum and maximum as described in the CTS (typically, ±0.5%).

The test is considered as passed if the DUT adequately supports the transmitted image; else, the test is considered as failed.

Connection Diagram

Refer to Figure 51 on page 116.

Result Description

ID HF2-38: Video Timing non 2160p 3D

[Not Compliant]

----General----	
Offline	True
Software Version	1.3.0
Calibration Data Version	Unknown; '1.3.0
Compliant	False
Non-compliance reason(s)	Procedure offline; Software st Fall/Rise Time Calibration
TMDS data to clock ratio 1:40	True
User Name	Unknown User
----M8195A - HDMI Sig. Gen.----	
DVI Mode	False
Fill up blanking periods with Null packets	False
Keep the signals after test?	False
Skip Pattern generation	True
----SCDC Controller----	
SCDC supports Character Error Detections	False
Skip Link Training	False
Start delay between SCDC controller and TMDS signal	100 ms
----Dso----	
Use internal probe head termination voltage	True

Result	Video Mode
pass	63: 1920x1080p @ 120 Hz _24_bit RGB_limited_range FramePacking (max frequency 120.6 Hz)
pass	63: 1920x1080p @ 120 Hz _24_bit RGB_limited_range FramePacking (min frequency 119.4 Hz)
pass	63: 1920x1080p @ 119.88 Hz _24_bit RGB_limited_range FramePacking (max frequency 120.6 Hz)
pass	63: 1920x1080p @ 119.88 Hz _24_bit RGB_limited_range FramePacking (min frequency 119.4 Hz)
pass	64: 1920x1080p @ 100 Hz _24_bit RGB_limited_range FramePacking (max frequency 100.5 Hz)
pass	64: 1920x1080p @ 100 Hz _24_bit RGB_limited_range FramePacking (min frequency 99.5 Hz)
pass	77: 1920x1080p @ 100 Hz _24_bit RGB_limited_range FramePacking (max frequency 100.5 Hz)
pass	77: 1920x1080p @ 100 Hz _24_bit RGB_limited_range FramePacking (min frequency 99.5 Hz)
pass	78: 1920x1080p @ 120 Hz _24_bit RGB_limited_range FramePacking (max frequency 120.6 Hz)
pass	78: 1920x1080p @ 120 Hz _24_bit RGB_limited_range FramePacking (min frequency 119.4 Hz)
pass	78: 1920x1080p @ 119.88 Hz _24_bit RGB_limited_range FramePacking (max frequency 120.6 Hz)
pass	78: 1920x1080p @ 119.88 Hz _24_bit RGB_limited_range FramePacking (min frequency 119.4 Hz)
pass	85: 1680x720p @ 120 Hz _24_bit RGB_limited_range FramePacking (max frequency 120.6 Hz)
pass	85: 1680x720p @ 120 Hz _24_bit RGB_limited_range FramePacking (min frequency 119.4 Hz)
pass	89: 2560x1080p @ 50 Hz _24_bit RGB_limited_range FramePacking (max frequency 50.25 Hz)
pass	89: 2560x1080p @ 50 Hz _24_bit RGB_limited_range FramePacking (min frequency 49.75 Hz)
pass	90: 2560x1080p @ 60 Hz _24_bit RGB_limited_range FramePacking (max frequency 60.3 Hz)
pass	90: 2560x1080p @ 60 Hz _24_bit RGB_limited_range FramePacking (min frequency 59.7 Hz)
pass	Test Result

Figure 67 Example result for Test ID HF2-38: Video Format Timing Non-2160p 3D

- Result: (Pass/Fail) Pass indicates that the DUT passed this test step successfully.
- Video Mode: The tested video mode. The final entry, “Test Result”, is for the entire test.

HDMI 2.1 FRL Signal

HFR2-1 Differential Swing Tolerance

Availability

- HDMI 2.1 FRL
- Compliance Mode, Expert Mode
- Minimum supported FRL data rate, Maximum supported FRL data rate

Purpose and Method

This procedure tests for compliance according to HDMI Sink CTS Version 2.1i, Section 5.2.1.1 “Sink FRL Electrical Tests”, HFR2-1: “Sink FRL Electrical - Min/Max Differential Swing Tolerance” and “HFR2-1 Keysight MOI v1.0d”.

An FRL Gap character pattern (that is, RXSB33PAT, as defined in the CTS) is generated with calibrated voltage levels and without any jitter applied. This procedure can be performed to find the minimum and maximum swing values.

NOTE **The minimum swing procedure is available in Expert Mode only and can be found under Expert Mode > HDMI 2.1 > Differential SwingTolerance in the procedure tree.**

For maximum swing, the differential swing voltage is fixed at 1200 mV. The V_{ICM} is set to 3.135 V.

At each step, link training is performed between the Sink DUT and the FRL Signal Generator for the selected FRL rate. If the link training passes, the FRL test patterns are applied and the software performs the BER test. The test is considered as passed if there are no errors; else, the test is considered as failed.

This test must be conducted for the highest and lowest supported data rates.

Connection Diagram

Refer to Figure 51 on page 116.

Result Description

HFR2-1 3Gbps Max Differential Swing Tolerance

[Not Compliant]

----General----	
Offline	True
Software Version	1.3.0
Calibration Data Version	Unknown
Compliant	False
Non-compliance reason(s)	Procedure offline; Software statu Lane2+_FrlLinkRate_3Gbps_ThreeLan Calibration Lane0+_FrlLinkRate_3G Calibration Lane1-_FrlLinkRate_3G Lane1+_FrlLinkRate_3Gbps_ThreeLan Lane2-_FrlLinkRate_3Gbps_ThreeLan
Video Mode	FRL0 (3 Lanes) : RXSB33PAT @ 3 GB
Start Differential Swing	1.2 V
Minimum Differential Swing	1.2 V
Differential Swing Step Size	10 mV
Voltage Offset	3.3 V
Starting Pattern on Lane 0	LTP5 - LFSR0 4096 FRL Characters
Starting Pattern on Lane 1	LTP6 - LFSR1 4096 FRL Characters
Starting Pattern on Lane 2	LTP7 - LFSR2 4096 FRL Characters
User Name	Unknown User
----M8195A - HDMI Sig. Gen.----	
DVI Mode	False
Fill up blanking periods with Null packets	False
Keep the signals after test?	False
Skip Pattern generation	True
----SCDC Controller----	
SCDC supports Character Error Detections	False
Skip Link Training	False
Start delay between SCDC controller and TMDS signal	100 ms
----Dso----	
Use internal probe head termination voltage	True

Result	Vicm	Passed Diff. Swing [mV]	Link Training	FRL Start	BER [ ]	Cumulative Errors []	Iterations []	Total Measurement Interval [s]	Total Bits Processed [ ]
pass	V_icm1 (3.3V)	1200	True	True	0.000E+000	0	10	111.1000	1.045E+012

Figure 68 Example result for HFR2-1: Differential Swing Tolerance

- Result: (Pass/Fail) Pass indicates that the DUT passed this test step successfully.
- V icm: The common mode voltage Level.
- Passed Diff. Swing [mV]: The minimum differential swing when the DUT passed (separated for each FRL pair).
- Link Training: Value is ‘True’ if link training is successful.

- FRL Start: Value is 'True' if the "FRL_Start" flag is set true (1) in the DUT after link training is performed.
- BER: Measured Bit Error Ratio.
- Cumulative Errors: Number of errors in all lanes during the BER test.
- Iterations: Number of iterations into which the BER measurement is divided.
- Total Measurement Interval [s]: The duration of the BER test in seconds.
- Total Bits Processed: The number of bits processed during the BER test.

HFR2-2 Intra-Pair Skew

Availability

- HDMI 2.1 FRL
- Compliance Mode, Expert Mode
- Minimum supported FRL data rate, Maximum supported FRL data rate

Purpose and Method

This procedure tests for compliance according to HDMI Sink CTS Version 2.1i, Section 5.2.1.1 “Sink FRL Electrical Tests”, HFR2-2: “Sink FRL Electrical - Intrapair Skew” and “HFR2-2 Keysight MOI v1.0d”.

For each FRL lane pair, the intra-pair skew is set to the worst case value 150 mTBit + 30 ps, as required in the MOI. The skew must be applied twice – once each on the positive lines and on the negative lines.

The V_{ICM} is set to 3.135 V and the differential swing voltage is set to 1 V.

At each step, link training is performed between the Sink DUT and the FRL Signal Generator for the selected FRL rate. If the link training passes, the FRL test patterns are applied and the software performs the BER test. The test is considered as passed if there are no errors; else, the test is considered as failed.

This test must be conducted for the highest and the lowest supported data rates.

Connection Diagram

Refer to Figure 51 on page 116.

Result Description

HFR2-2 3Gbps Intrapair Skew

[Not Compliant]

----General----	
Offline	True
Software Version	1.3.0
Calibration Data Version	Unknown
Compliant	False
Non-compliance reason(s)	Procedure offline; Software status Lane2+_FrlLinkRate_3Gbps_ThreeLane, Calibration, FRL Swing Calibration Lane0-_FrlLinkRate_3Gbps_ThreeLane, Lane0+_FrlLinkRate_3Gbps_ThreeLane, Lane1-_FrlLinkRate_3Gbps_ThreeLane,
Video Mode	FRL0 (3 Lanes) : RXSB33PAT @ 3 GBit
Skew	240 mTBit
Skew in ps	80 ps
Cable Emulator	HDMI 2 1 WCM3
Starting Pattern on Lane 0	LTP5 - LFSR0 4096 FRL Characters
Starting Pattern on Lane 1	LTP6 - LFSR1 4096 FRL Characters
Starting Pattern on Lane 2	LTP7 - LFSR2 4096 FRL Characters
Enable Crosstalk	True
User Name	Unknown User
----M8195A - HDMI Sig. Gen.----	
DVI Mode	False
Fill up blanking periods with Null packets	False
Keep the signals after test?	False
Skip Pattern generation	True
----SCDC Controller----	
SCDC supports Character Error Detections	False
Skip Link Training	False
Start delay between SCDC controller and TMDS signal	100 ms
----Dso----	
Use internal probe head termination voltage	True

Result	FRL Lane	Link Training	FRL Start	BER [ ]	Cumulative Errors []	Iterations []	Total Measurement Interval [s]	Total Bits Processed [ ]
pass	All Lanes+	True	True	0.000E+000	0	10	111.1000	1.045E+012
pass	All Lanes-	True	True	0.000E+000	0	10	111.1000	1.045E+012

Figure 69 Example result for HFR2-2: Intra-Pair Skew

- Result: (Pass/Fail) Pass indicates that the DUT passed this test step successfully.
- FRL Lane: The lane where skew is applied.
- Link Training: Value is ‘True’ if link training is successful.
- FRL Start: Value is ‘True’ if the “FRL_Start” flag is set true (1) in the DUT after link training is performed.
- BER: Measured Bit Error Ratio.

- Cumulative Errors: Number of errors in all lanes during the BER test.
- Iterations: Number of iterations into which the BER measurement is divided.
- Total Measurement Interval: The duration of the BER test in seconds.
- Total Bits Processed: The number of bits processed during the BER test.

HFR2-3 Inter-Pair Skew

Availability

- HDMI 2.1 FRL
- Compliance Mode, Expert Mode
- Minimum supported FRL data rate, Maximum supported FRL data rate
- Lane0, Lane1, Lane2

Purpose and Method

This procedure tests for compliance according to HDMI Sink CTS Version 2.1i, Section 5.2.1.1 “Sink FRL Electrical Tests”, HFR2-3: “Sink FRL Electrical - Inter-Pair Skew” and “HFR2-3 Keysight MOI v1.0d”.

The data generator sets a delay of 400 mTBit + 500 ps on one lane against all other lanes. This inter-pair skew is applied first on the positive line then on the negative line of the tested lane. All lanes must be tested, therefore, the procedure must be run for each lane.

The V_{ICM} is set to 3.135 V and the differential swing voltage is set to 1 V.

At each step, link training is performed between the Sink DUT and the FRL Signal Generator for the selected FRL rate. If the link training passes, the FRL test patterns are applied and the software performs the BER test. The test is considered as passed if there are no errors; else, the test is considered as failed.

This test must be conducted for the highest and the lowest supported data rates.

Connection Diagram

Refer to Figure 51 on page 116.

Result Description

HFR2-3 3Gbps Inter-Pair Skew Lane0

[Not Compliant]

----General----	
Offline	True
Software Version	1.3.0
Calibration Data Version	Unknown
Compliant	False
Non-compliance reason(s)	Procedure offline; Software status Lane2+_FrlLinkRate_3Gbps_ThreeLane, Calibration, FRL Swing Calibration Lane0-_FrlLinkRate_3Gbps_ThreeLane, Lane0+_FrlLinkRate_3Gbps_ThreeLane, Lane1-_FrlLinkRate_3Gbps_ThreeLane,
Video Mode	FRL0 (3 Lanes) : RXSB33PAT @ 3 GBit
Cable Emulator	HDMI 2 1 WCM3
Starting Pattern on Lane 0	LTP5 - LFSR0 4096 FRL Characters
Starting Pattern on Lane 1	LTP6 - LFSR1 4096 FRL Characters
Starting Pattern on Lane 2	LTP7 - LFSR2 4096 FRL Characters
Enable Crosstalk	True
User Name	Unknown User
----M8195A - HDMI Sig. Gen.----	
DVI Mode	False
Fill up blanking periods with Null packets	False
Keep the signals after test?	False
Skip Pattern generation	True
----SCDC Controller----	
SCDC supports Character Error Detections	False
Skip Link Training	False
Start delay between SCDC controller and TMDS signal	100 ms
----Dso----	
Use internal probe head termination voltage	True

Result	Max Inter-Pair Skew [mTBit]	Link Training	FRL Start	BER [ ]	Cumulative Errors []	Iterations []	Total Measurement Interval [s]	Total Bits Processed [ ]
pass	5500	True	True	0.000E+000	0	10	111.1000	1.045E+012
pass	-5500	True	True	0.000E+000	0	10	111.1000	1.045E+012

Figure 70 Example result for HFR2-3: Inter-Pair Skew

- Result: (Pass/Fail) Pass indicates that the DUT passed this test step successfully.
- Max Inter-Pair Skew [mTBit]: The skew value applied to the tested lane.
- Link Training: Value is ‘True’ if link training is successful.
- FRL Start: Value is ‘True’ if the “FRL_Start” flag is set true (1) in the DUT after link training is performed.
- BER: Measured Bit Error Ratio.
- Cumulative Errors: Number of errors in all lanes during the BER test.

- Iterations: Number of iterations into which the BER measurement is divided.
- Total Measurement Interval: The duration of the BER test in seconds.
- Total Bits Processed: The number of bits processed during the BER test.

HFR2-4 Minimum Link Rate

Availability

- HDMI 2.1 FRL
- Compliance Mode, Expert Mode
- Minimum supported FRL data rate, Maximum supported FRL data rate

Purpose and Method

This procedure tests for compliance according to HDMI Sink CTS Version 2.1i, Section 5.2.1.1 “Sink FRL Electrical Tests”, HFR2-4: “Sink FRL Electrical - Minimum Link Rate Tolerance” and “HFR2-4 Keysight MOI v1.0d”.

The link rate tolerance is tested by applying a deviation of 300 ppm to the nominal value. Both positive and negative deviations are tested.

The V_{ICM} is set to 3.135 V and the differential swing voltage is set to 1 V.

At each step, link training is performed between the Sink DUT and the FRL Signal Generator for the selected FRL rate. If the link training passes, the FRL test patterns are applied and the software performs the BER test. The test is considered as passed if there are no errors; else, the test is considered as failed.

This test must be conducted for the highest and the lowest supported data rates.

Connection Diagram

Refer to Figure 51 on page 116.

Result Description

HFR2-4 3Gbps Minimum Link Rate Tolerance

[Not Compliant]

----General----	
Offline	True
Software Version	1.3.0
Calibration Data Version	Unknown
Compliant	False
Non-compliance reason(s)	Procedure offline; Software status Lane2+_FrlLinkRate_3Gbps_ThreeLane Calibration, FRL Swing Calibration Lane0-_FrlLinkRate_3Gbps_ThreeLane Lane0+_FrlLinkRate_3Gbps_ThreeLane Lane1-_FrlLinkRate_3Gbps_ThreeLane
Video Mode	FRL0 (3 Lanes) : RXSB33PAT @ 3 GBi
Cable Emulator	HDMI 2 1 WCM3
Starting Pattern on Lane 0	LTP5 - LFSR0 4096 FRL Characters
Starting Pattern on Lane 1	LTP6 - LFSR1 4096 FRL Characters
Starting Pattern on Lane 2	LTP7 - LFSR2 4096 FRL Characters
Enable Crosstalk	True
User Name	Unknown User
----M8195A - HDMI Sig. Gen.----	
DVI Mode	False
Fill up blanking periods with Null packets	False
Keep the signals after test?	False
Skip Pattern generation	True
----SCDC Controller----	
SCDC supports Character Error Detections	False
Skip Link Training	False
Start delay between SCDC controller and TMDS signal	100 ms
----Dso----	
Use internal probe head termination voltage	True

Result	Link Rate Deviation [Bit/s]	Link Training	FRL Start	BER [ ]	Cumulative Errors []	Iterations []	Total Measurement Interval [s]	Total Bits Processed [ ]
pass	3000900000	True	True	0.000E+000	0	10	111.1000	1.045E+012
pass	2999100000	True	True	0.000E+000	0	10	111.1000	1.045E+012

Figure 71 Example result for HFR2-4: Minimum Link Rate

- Result: (Pass/Fail) Pass indicates that the DUT passed this test step successfully.
- Link Rate Deviation [Bit/s]: The value of link rate deviation applied to the nominal value.
- Link Training: Value is 'True' if link training is successful.
- FRL Start: Value is 'True' if the "FRL_Start" flag is set true (1) in the DUT after link training is performed.
- BER: Measured Bit Error Ratio.

- Cumulative Errors: Number of errors in all lanes during the BER test.
- Iterations: Number of iterations into which the BER measurement is divided.
- Total Measurement Interval: The duration of the BER test in seconds.
- Total Bits Processed: The number of bits processed during the BER test.

HFR2-5 Jitter Tolerance

Availability

- HDMI 2.1 FRL
- Compliance Mode, Expert Mode
- Minimum supported FRL data rate, Maximum supported FRL data rate

Purpose and Method

This procedure tests for compliance according to HDMI Sink CTS Version 2.1i, Section 5.2.1.1 “Sink FRL Electrical Tests”, HFR2-5: “Sink FRL Electrical - Jitter Tolerance” and “HFR2-5 Keysight MOI v1.0d”.

In this procedure, the FRL data generator is configured to generate a signal that meets the compliance eye diagram mask according to the HDMI specifications.

The differential swing is set to meet the target eye height, which is a value between 150 mV and 100 mV, depending on the link rate tested.

The random jitter and PCB Loss Factor are set to meet the target width, which is a value between 500 mTBit and 350 mTBit, depending on the link rate tested.

Thereafter, link training is performed between the Sink DUT and the FRL Signal Generator for the selected FRL rate. If the link training passes, the FRL test patterns are applied and the software performs the BER test. The test is considered as passed if there are no errors; else, the test is considered as failed.

This procedure must be repeated for various sinusoidal jitter amplitude and frequency pairs:

- SJ = 1 UI @ $0.1*f_c$
- SJ = 0.51 UI @ $0.2*f_c$
- SJ = 0.22 UI @ $0.5*f_c$
- SJ = 0.14 UI @ $1*f_c$
- SJ = 0.11 UI @ $2*f_c$
- SJ = 0.10 UI @ $5*f_c$
- SJ = 0.10 UI @ $10*f_c$

Here, f_c is the clock frequency and has the values

- 4 MHz for FRL rate R_{bit} = 3 Gb/s
- R_{bit}/1500 for FRL rate R_{bit} = 6 Gb/s, 8 Gb/s, 10 Gb/s and12 Gb/s

This test must be conducted for the highest and the lowest supported data rates.

Connection Diagram

Refer to Figure 51 on page 116.

Result Description

HFR2-5 3Gbps Jitter Tolerance 1UI@400kHz

[Not Compliant]

----General----	
Offline	True
Software Version	1.3.0
Calibration Data Version	Unknown
Compliant	False
Non-compliance reason(s)	Procedure offline; Software status Lane2+_FrlLinkRate_3Gbps_ThreeLane Calibration, FRL Swing Calibration Lane0-_FrlLinkRate_3Gbps_ThreeLane Lane0+_FrlLinkRate_3Gbps_ThreeLane Lane1-_FrlLinkRate_3Gbps_ThreeLane
Video Mode	FRL0 (3 Lanes) : RXSB33PAT @ 3 GBi
Cable Emulator	HDMI 2 1 WCM3
Starting Pattern on Lane 0	LTP5 - LFSR0 4096 FRL Characters
Starting Pattern on Lane 1	LTP6 - LFSR1 4096 FRL Characters
Starting Pattern on Lane 2	LTP7 - LFSR2 4096 FRL Characters
Target Jitter Lane0	500 mUI
Target Jitter Lane1	500 mUI
Target Jitter Lane2	500 mUI
Eye Height Lane0	150 mV
Eye Height Lane1	150 mV
Eye Height Lane2	150 mV
SJ pk-pk	1 UI
SJ Frequency	400 kHz
Enable Crosstalk	True
User Name	Unknown User
----M8195A - HDMI Sig. Gen.----	
DVI Mode	False
Fill up blanking periods with Null packets	False
Keep the signals after test?	False
Skip Pattern generation	True
----SCDC Controller----	
SCDC supports Character Error Detections	False
Skip Link Training	False
Start delay between SCDC controller and TMDS signal	100 ms
----Dso----	
Use internal probe head termination voltage	True

Result	Total Jitter [mTBit]	Link Training	FRL Start	BER [ ]	Cumulative Errors []	Iterations []	Total Measurement Interval [s]	Total Bits Processed [ ]
pass		True	True	0.000E+000	0	10	111.1000	1.045E+012

Figure 72 Example result for HFR2-5: Jitter Tolerance

- Result: (Pass/Fail) Pass indicates that the DUT passed this test step successfully.
- Total Jitter [mTBit]: The total jitter added to the signal in this step.
- Link Training: Value is 'True' if link training is successful.
- FRL Start: Value is 'True' if the "FRL_Start" flag is set true (1) in the DUT after link training is performed.
- BER: Measured Bit Error Ratio.
- Cumulative Errors: Number of errors in all lanes during the BER test.
- Iterations: Number of iterations into which the BER measurement is divided.
- Total Measurement Interval [s]: The duration of the BER test in seconds.
- Total Bits Processed: The number of bits processed during the BER test.

Additional Sink Tests in Expert Mode

The tests described in this section are available only in Expert Mode and are intended for custom characterization and debugging of sink DUTs.

ID 8-15 Character Synchronization Test

Availability

- HDMI 1.4
- Expert Mode

Purpose and Method

This procedure tests for compliance according to HDMI CTS Version 1.4b, Section 8.4 “Sink – Protocol”, Test ID 8-15: “Character Synchronization”. A valid video signal with a resolution of 640 x 480p and a frequency of 60 Hz is generated with all blanking periods filled up with packets. The test is considered as passed if the Sink displays the expected video image without errors; otherwise, the test is considered as failed.

Connection Diagram

Refer to Figure 51 on page 116.

Result Description

ID 8-15: Character Synchronization Test

[Not Compliant]

CTS Test

----General----	
Offline	True
Software Version	1.3.0
Calibration Data Version	Unknown; '1.3.0
Compliant	False
Non-compliance reason(s)	Procedure offline; Software st Fall/Rise Time Calibration
User Name	Unknown User
----M8195A - HDMI Sig. Gen.----	
DVI Mode	False
Fill up blanking periods with Null packets	False
Keep the signals after test?	False
Skip Pattern generation	True
----SCDC Controller----	
SCDC supports Character Error Detections	False
Skip Link Training	False
Start delay between SCDC controller and TMDS signal	100 ms
----Dso----	
Use internal probe head termination voltage	True

Result	Pixel Errors
pass	No

Figure 73 Example result for Test ID 8-15: Character Synchronization

- Result: (Pass/Fail) Pass indicates that the DUT passed this test step successfully.
- Pixel Errors: (Yes/No) Output errors on DUT.

ID 8-16 Acceptance of All Valid Packet Types

Availability

- HDMI 1.4
- Expert Mode

Purpose and Method

This procedure tests for compliance according to HDMI CTS Version 1.4b, Section 8.4 “Sink – Protocol”, Test ID 8-16: “Acceptance of All Valid Packet Types”.

This is a compliance test to verify that a DUT supports all valid packet types. The procedure will verify all valid packet types as required by the CTS. At each step, the DUT must support the signal.

The test is considered as passed if the DUT shows an image; otherwise, the test is considered as failed.

Connection Diagram

Refer to Figure 51 on page 116.

Result Description

ID 8-16: Acceptance of All Valid Packet Types

[Not Compliant]

----General----	
Offline	True
Software Version	1.3.0
Calibration Data Version	Unknown; '1.3.0
Compliant	False
Non-compliance reason(s)	Procedure offline; Software st Fall/Rise Time Calibration
User Name	Unknown User
----M8195A - HDMI Sig. Gen.----	
DVI Mode	False
Fill up blanking periods with Null packets	False
Keep the signals after test?	False
Skip Pattern generation	True
----SCDC Controller----	
SCDC supports Character Error Detections	False
Skip Link Training	False
Start delay between SCDC controller and TMDS signal	100 ms
----Dso----	
Use internal probe head termination voltage	True

Result	Packet
pass	GeneralControl_Clear_AVMute_Clear, AVI Info, Audio Info, NULL packet, Vendor-specific Info, MPEG info, SPD info
pass	GeneralControl_Set_AVMute_Clear, AVI Info, Audio Info, NULL packet, Vendor-specific Info, MPEG info, SPD info
pass	ISRC1_Packet, AVI Info, Audio Info, NULL packet, Vendor-specific Info, MPEG info, SPD info
pass	ISRC2_Packet, AVI Info, Audio Info, NULL packet, Vendor-specific Info, MPEG info, SPD info
pass	

Figure 74 Example result for Test ID 8-16: Acceptance of All Valid Packet Types

- Result: (Pass/Fail) Pass indicates that the DUT passed this test step successfully.
- Packet: Name of the tested packet.

ID 8-19 Pixel Encoding Requirements

Availability

- HDMI 1.4
- Expert Mode

Purpose and Method

This procedure tests for compliance according to HDMI CTS Version 1.4b, Section 8.5 “Sink – Video”, Test ID 8-19: “Pixel Encoding Requirements”.

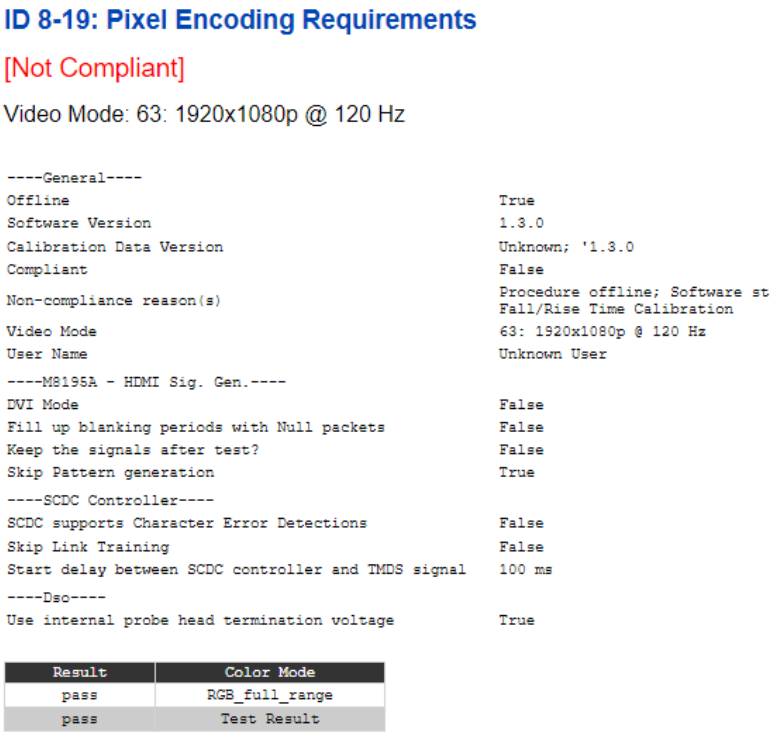
Depending on the supported pixel encoding by the DUT, a valid video signal with a resolution of 720 x 480p or 720 x 576p is generated at each step. The various supported pixel encodings are configured in the “Configure Product” dialog.

The test is considered as passed if, for all supported pixel encodings, the Sink displays the expected video image without errors; otherwise, the test is considered as failed.

Connection Diagram

Refer to Figure 51 on page 116.

Result Description



ID 8-19: Pixel Encoding Requirements

[Not Compliant]

Video Mode: 63: 1920x1080p @ 120 Hz

----General----	
Offline	True
Software Version	1.3.0
Calibration Data Version	Unknown; '1.3.0
Compliant	False
Non-compliance reason(s)	Procedure offline; Software st Fall/Rise Time Calibration
Video Mode	63: 1920x1080p @ 120 Hz
User Name	Unknown User
----M8195A - HDMI Sig. Gen.----	
DVI Mode	False
Fill up blanking periods with Null packets	False
Keep the signals after test?	False
Skip Pattern generation	True
----SCDC Controller----	
SCDC supports Character Error Detections	False
Skip Link Training	False
Start delay between SCDC controller and TMDS signal	100 ms
----Dso----	
Use internal probe head termination voltage	True

Result	Color Mode
pass	RGB_full_range
pass	Test Result

Figure 75 Example result for Test ID 8-19: Pixel Encoding Requirements

- Result: (Pass/Fail) Pass indicates that the DUT passed this test step successfully.
- Color Mode: The tested color mode. The final entry, “Test Result”, is for the entire test.

ID 8-20 Video Format Timing

Availability

- HDMI 1.4
- Expert Mode

Purpose and Method

This procedure tests for compliance according to HDMI CTS Version 1.4b, Section 8.5 “Sink – Video”, Test ID 8-20: “Video Format Timing”.

For each supported format and pixel clock frequency, two video signals are generated. These signals are generated with a pixel clock frequency deviation of either –0.5% or +0.5%.

The test is considered as passed if the Sink displays the expected video image at the minimum and maximum allowed pixel clock frequency for all supported formats and frequencies; otherwise, the test is considered as failed.

Connection Diagram

Refer to Figure 51 on page 116.

Result Description

ID 8-20: Video Format Timing

[Not Compliant]

----General----	
Offline	True
Software Version	1.3.0
Calibration Data Version	Unknown; '1.3.0
Compliant	False
Non-compliance reason(s)	Procedure offline; Software st Fall/Rise Time Calibration
User Name	Unknown User
----M8195A - HDMI Sig. Gen.----	
DVI Mode	False
Fill up blanking periods with Null packets	False
Keep the signals after test?	False
Skip Pattern generation	True
----SCDC Controller----	
SCDC supports Character Error Detections	False
Skip Link Training	False
Start delay between SCDC controller and TMDS signal	100 ms
----Dso----	
Use internal probe head termination voltage	True

Result	Video Mode
pass	01: 640x480p, Max(60.3 Hz)
pass	01: 640x480p, Min(59.64 Hz)
pass	02: 720x480p, Max(60.3 Hz)
pass	02: 720x480p, Min(59.64 Hz)
pass	03: 720x480p, Max(60.3 Hz)
pass	03: 720x480p, Min(59.64 Hz)
pass	04: 1280x720p, Max(60.3 Hz)
pass	04: 1280x720p, Min(59.64 Hz)
pass	05: 1920x1080i, Max(60.3 Hz)
pass	05: 1920x1080i, Min(59.64 Hz)
pass	06: 1440x480i, Max(60.3 Hz)
pass	06: 1440x480i, Min(59.64 Hz)
pass	07: 1440x480i, Max(60.3 Hz)
pass	07: 1440x480i, Min(59.64 Hz)
pass	08: 1440x240p, 22 VBlank lines, Max(60.415575 Hz)
pass	08: 1440x240p, 22 VBlank lines, Min(59.814425 Hz)
pass	08: 1440x240p, 23 VBlank lines, Max(60.415575 Hz)

Figure 76 Example result for Test ID 8-20: Video Format Timing (just the top of the table)

- Result: (Pass/Fail) Pass indicates that the DUT passed this test step successfully.
- Video Mode: The tested video mode. The final entry, “Test Result” (not shown here), is for the entire test.

ID 8-21 Audio Clock Regeneration

Availability

- HDMI 1.4
- Expert Mode

Purpose and Method

This procedure tests for compliance according to HDMI CTS Version 1.4b, Section 8.6 “Sink – Audio”, Test ID 8-21: “Audio Clock Regeneration”.

This test checks whether a DUT operates correctly with respect to Audio Clock Regeneration. A video format of 576p is used, including audio with a sampling rate of 48 kHz along with an ACR packet data at minimum deviation in the first step and maximum deviation in the second step. For both steps, a listening test must be performed.

The test is considered as Passed if sound is played appropriately; else, the test is considered as failed if there is no sound or extraneous sound, such as breaking up sound or unnecessary mute.

Connection Diagram

Refer to Figure 51 on page 116.

Result Description

ID 8-21: Audio Clock Regeneration

[Not Compliant]

----General----	
Offline	True
Software Version	1.3.0
Calibration Data Version	Unknown; '1.3.0
Compliant	False
Non-compliance reason(s)	Procedure offline; Software st Fall/Rise Time Calibration
User Name	Unknown User
----M8195A - HDMI Sig. Gen.----	
DVI Mode	False
Fill up blanking periods with Null packets	False
Keep the signals after test?	False
Skip Pattern generation	True
----SCDC Controller----	
SCDC supports Character Error Detections	False
Skip Link Training	False
Start delay between SCDC controller and TMDS signal	100 ms
----Dso----	
Use internal probe head termination voltage	True

Result	Audio clock regeneration
pass	CDF Pre-Test
pass	Minimum
pass	Maximum
pass	

Figure 77 Example result for Test ID 8-21: Audio Clock Regeneration

- Result: (Pass/Fail) Pass indicates that the DUT passed this test step successfully. The final row applies to the complete test.
- Audio clock regeneration: The type of audio clock regeneration.

ID 8-22 Audio Jitter Test

Availability

- HDMI 1.4
- Expert Mode

Purpose and Method

This procedure tests for compliance according to HDMI CTS Version 1.4b, Section 8.6 “Sink – Audio”, Test ID 8-22: “Audio Sample Packet Jitter”.

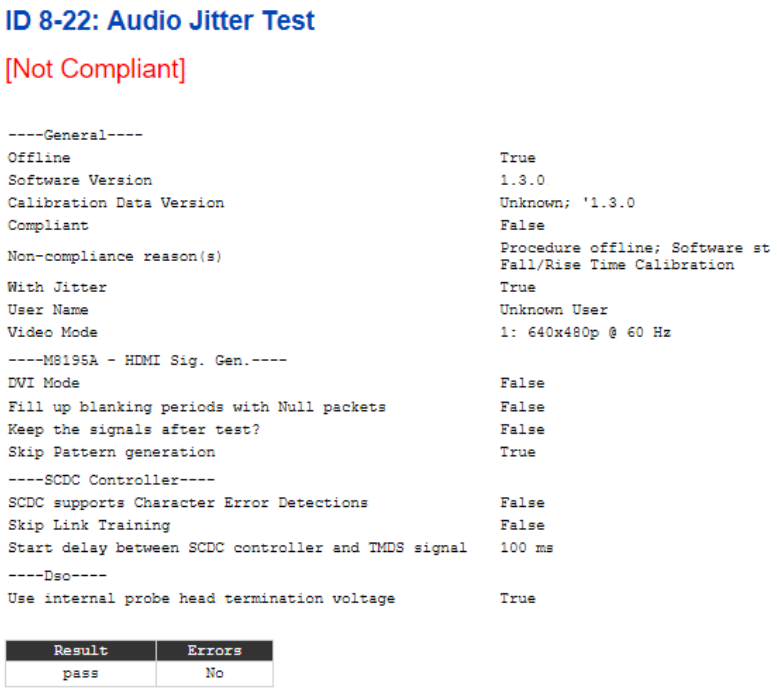
The purpose of this test is to find out if the DUT plays audio properly with the maximum allowed Audio Sample Jitter. It runs for the 480p, 576p or VGA video mode. The software applies maximum jitter to the Audio Sample Packet transmission timing. Then, a listening test is performed.

The test is considered as passed if sound is played appropriately; the test is considered as failed if there is either no sound or extraneous sound, such as crackling or it is unnecessarily muted.

Connection Diagram

Refer to Figure 51 on page 116.

Result Description



ID 8-22: Audio Jitter Test

[Not Compliant]

----General----	
Offline	True
Software Version	1.3.0
Calibration Data Version	Unknown; '1.3.0
Compliant	False
Non-compliance reason(s)	Procedure offline; Software st Fall/Rise Time Calibration
With Jitter	True
User Name	Unknown User
Video Mode	1: 640x480p @ 60 Hz
----M8195A - HDMI Sig. Gen.----	
DVI Mode	False
Fill up blanking periods with Null packets	False
Keep the signals after test?	False
Skip Pattern generation	True
----SCDC Controller----	
SCDC supports Character Error Detections	False
Skip Link Training	False
Start delay between SCDC controller and TMDS signal	100 ms
----Dso----	
Use internal probe head termination voltage	True

Result	Errors
pass	No

Figure 78 Example result for Test ID 8-22 Audio Jitter

- Result: (Pass/Fail) Pass indicates that the DUT passed this test step successfully.
- Errors: (Yes/No) Output errors detected.

ID 8-23 Audio Formats

Availability

- HDMI 1.4
- Expert Mode

Purpose and Method

This procedure tests for compliance according to HDMI CTS Version 1.4b, Section 8.6 “Sink – Audio”, Test ID 8-23: “Audio Formats”.

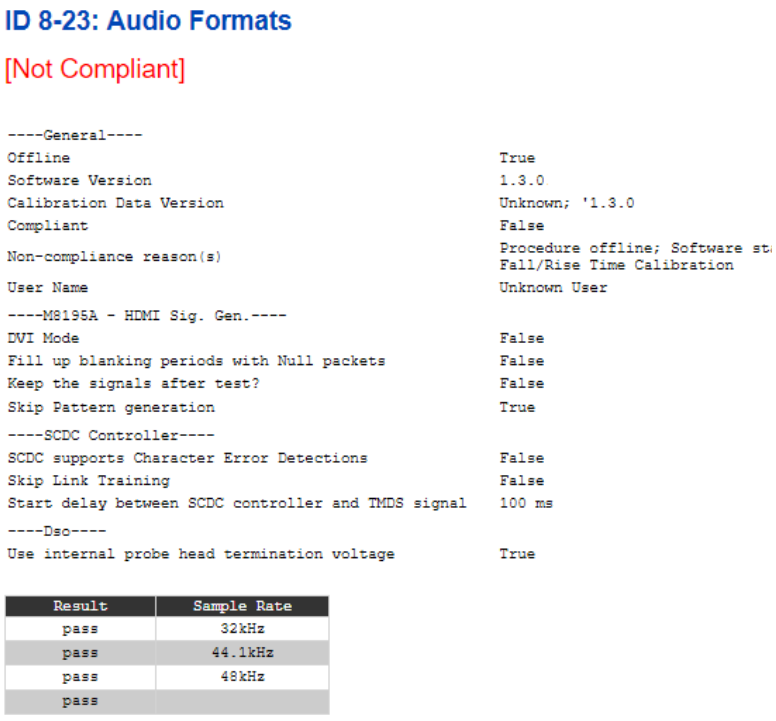
This test verifies if the DUT supports each and every audio format specified in EDID. For this purpose, any DUT-supported video format can be used. This video format is generated with three different audio sample rates: 32 kHz, 44.1 kHz and 48 kHz.

The test is considered as passed if the listening test is successful; the test is considered as failed if any of the sample rates are not supported by the DUT appropriately (listening test).

Connection Diagram

Refer to Figure 51 on page 116.

Result Description



ID 8-23: Audio Formats

[Not Compliant]

----General----	
Offline	True
Software Version	1.3.0
Calibration Data Version	Unknown; '1.3.0
Compliant	False
Non-compliance reason(s)	Procedure offline; Software st Fall/Rise Time Calibration
User Name	Unknown User
----M8195A - HDMI Sig. Gen.----	
DVI Mode	False
Fill up blanking periods with Null packets	False
Keep the signals after test?	False
Skip Pattern generation	True
----SCDC Controller----	
SCDC supports Character Error Detections	False
Skip Link Training	False
Start delay between SCDC controller and TMDS signal	100 ms
----Dso----	
Use internal probe head termination voltage	True

Result	Sample Rate
pass	32kHz
pass	44.1kHz
pass	48kHz
pass	

Figure 79 Example result for Test ID 8-23: Audio Formats

- Result: (Pass/Fail) Pass indicates that the DUT passed this test step successfully.
- Sample Rate: Tested Sample Rate.

ID 8-24 Interoperability with DVI

Availability

- HDMI 1.4
- Expert Mode

Purpose and Method

This procedure tests for compliance according to HDMI CTS Version 1.4b, Section 8.7 “Sink – Interoperability With DVI”, Test ID 8-24: “Interoperability With DVI”.

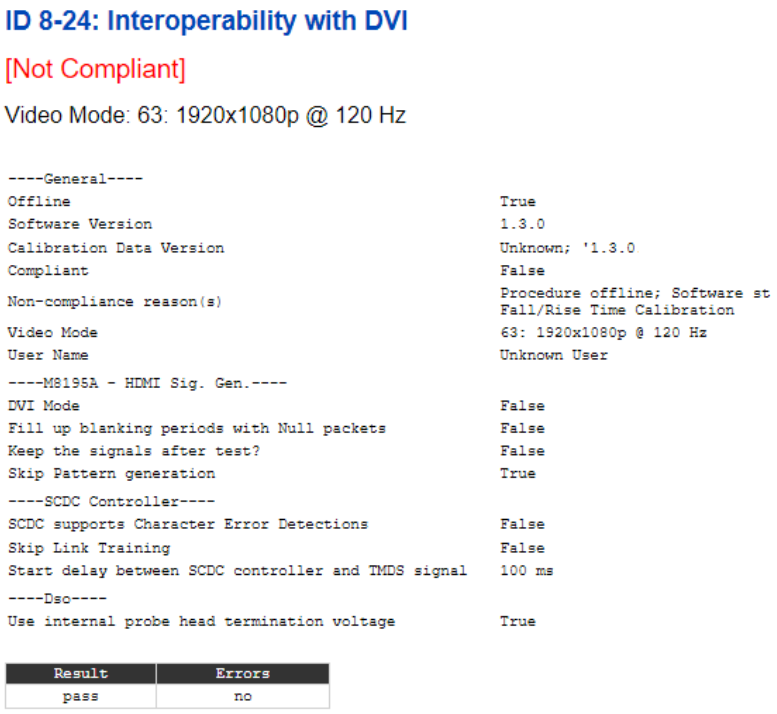
Depending on the formats supported by the DUT, a valid video signal with a resolution of either 720x480p or 720x576p is generated with RGB pixel encoding, without any Guard Bands or Data Islands.

The test is considered as passed if the sink displays the expected video image; otherwise, the test is considered as failed.

Connection Diagram

Refer to Figure 51 on page 116.

Result Description



ID 8-24: Interoperability with DVI

[Not Compliant]

Video Mode: 63: 1920x1080p @ 120 Hz

----General----	
Offline	True
Software Version	1.3.0
Calibration Data Version	Unknown; '1.3.0
Compliant	False
Non-compliance reason(s)	Procedure offline; Software st Fall/Rise Time Calibration
Video Mode	63: 1920x1080p @ 120 Hz
User Name	Unknown User
----M8195A - HDMI Sig. Gen.----	
DVI Mode	False
Fill up blanking periods with Null packets	False
Keep the signals after test?	False
Skip Pattern generation	True
----SCDC Controller----	
SCDC supports Character Error Detections	False
Skip Link Training	False
Start delay between SCDC controller and TMDS signal	100 ms
----Dso----	
Use internal probe head termination voltage	True

Result	Errors
pass	no

Figure 80 Example result for Test ID 8-24: Interoperability with DVI

- Result: (Pass/Fail) Pass indicates that the DUT passed this test step successfully.
- Errors: (Yes/No) Output errors detected.

ID 8-25 Deep Color

Availability

- HDMI 1.4
- Expert Mode
- Only video modes below 340 Mcsc
- Color depth 30 bit, 36 bit, 48 bit

Purpose and Method

This procedure tests for compliance according to HDMI CTS Version 1.4b, Section 8.8 “Sink – Advanced Features”, Test ID 8-25: “Deep Color”.

The purpose of this test is to verify that the DUT supports all selected deep color modes. The test processes all selected deep color modes (as 30 bit, 36 bit and 48 bit) with all supported video formats and checks if the DUT displays them accordingly.

The test is considered as passed if the DUT displays the expected image; otherwise, the test is considered as failed.

Connection Diagram

Refer to Figure 51 on page 116.

Result Description

ID 8-25: Deep Color

[Not Compliant]

----General----	
Offline	True
Software Version	2023
Calibration Data Version	Unknown; '1.3.0
Compliant	False
Non-compliance reason(s)	Procedure offline; Software st Fall/Rise Time Calibration
CTS Revision	1.4b
User Name	Unknown User
----M8195A - HDMI Sig. Gen.----	
DVI Mode	False
Fill up blanking periods with Null packets	False
Keep the signals after test?	False
Skip Pattern generation	True
----SCDC Controller----	
SCDC supports Character Error Detections	False
Skip Link Training	False
Start delay between SCDC controller and TMDS signal	100 ms
----Dso----	
Use internal probe head termination voltage	True

Result	Video Mode
pass	01: 640x480p @ 60 Hz _36_bit RGB_full_range
pass	02: 720x480p @ 60 Hz _36_bit RGB_limited_range
pass	01: 640x480p @ 60 Hz _48_bit RGB_full_range
pass	02: 720x480p @ 60 Hz _48_bit RGB_limited_range
pass	Test Result

Figure 81 Example result for Test ID 8-25: Deep Color

- Result: (Pass/Fail) Pass indicates that the DUT passed this test step successfully.
- Video Mode: Tested Video mode. The final entry, “Test Result”, is for the entire test.

ID 8-29: 3D Video Format Timing

Availability

- HDMI 1.4
- Expert Mode only

Purpose and Method

This procedure tests for compliance according to HDMI CTS Version 1.4b, Section 8.8 “Sink – Advanced Features”, Test ID 8-29: “3D Video Format Timing”.

This test verifies that the sink DUT supports the required variations on mandatory 3D video formats and other primary 3D video formats as listed in the EDID.

The software processes all selected video formats and tests them. The software generates two video signals for each combination of the supported video format, 3D mode and pixel clock frequency, with a pixel clock frequency deviation of either –0.5% or +0.5%.

The test is considered as passed if the DUT displays the image correctly at each step; otherwise, the test is considered as failed.

Connection Diagram

Refer to Figure 51 on page 116.

Result Description

ID 8-29: 3D Video Format Timing

[Not Compliant]

----General----	
Offline	True
Software Version	1.3.0
Calibration Data Version	Unknown; '1.3.0
Compliant	False
Non-compliance reason(s)	Procedure offline; Software st Fall/Rise Time Calibration
User Name	Unknown User
----M8195A - HDMI Sig. Gen.----	
DVI Mode	False
Fill up blanking periods with Null packets	False
Keep the signals after test?	False
Skip Pattern generation	True
----SCDC Controller----	
SCDC supports Character Error Detections	False
Skip Link Training	False
Start delay between SCDC controller and TMDS signal	100 ms
----Dso----	
Use internal probe head termination voltage	True

Result	Video Mode
pass	32: 1920x1080p @ 24 Hz _24_bit RGB_full_range FramePacking (max frequency 24.12 Hz)
pass	32: 1920x1080p @ 24 Hz _24_bit RGB_full_range FramePacking (min frequency 23.86 Hz)
pass	32: 1920x1080p @ 24 Hz _24_bit RGB_full_range TopBottom (max frequency 24.12 Hz)
pass	32: 1920x1080p @ 24 Hz _24_bit RGB_full_range TopBottom (min frequency 23.86 Hz)
pass	04: 1280x720p @ 60 Hz _24_bit RGB_full_range FramePacking (max frequency 60.3 Hz)
pass	04: 1280x720p @ 60 Hz _24_bit RGB_full_range FramePacking (min frequency 59.64 Hz)
pass	05: 1920x1080i @ 60 Hz _24_bit RGB_full_range SideBySide_Half (max frequency 60.3 Hz)
pass	05: 1920x1080i @ 60 Hz _24_bit RGB_full_range SideBySide_Half (min frequency 59.64 Hz)
pass	04: 1280x720p @ 60 Hz _24_bit RGB_full_range TopBottom (max frequency 60.3 Hz)
pass	04: 1280x720p @ 60 Hz _24_bit RGB_full_range TopBottom (min frequency 59.64 Hz)

Figure 82 Example result for Test ID 8-29: 3D Video Format Timing (just the top of the table)

- Result: (Pass/Fail) Pass indicates that the DUT passed this test step successfully.
- Video Mode: The tested video mode.

ID 8-30 4K x 2K Video Format Timing

Availability

- HDMI 1.4
- Expert Mode

Purpose and Method

This procedure tests for compliance according to HDMI CTS Version 1.4b, Section 8.5 “Sink – Video”, Test ID 8-30: “4K x 2K Video Format Timing”.

This test verifies that DUT supports the selected 4K x 2K video formats.

The software processes all selected HDMI 1.4 4K x 2K video formats (in CTS defined as HDMI_VIC) and tests them. The software generates two video signals for each combination of the supported video format and pixel clock frequency, with a pixel clock frequency deviation of either –0.5% or +0.5%.

The test is considered as passed if the DUT displays the image correctly at each step; else, the test is considered as failed.

Connection Diagram

Refer to Figure 51 on page 116.

Result Description

ID 8-30: 4k x 2k Video Format Timing

[Not Compliant]

----General----	
Offline	True
Software Version	1.3.0
Calibration Data Version	Unknown; '1.3.0
Compliant	False
Non-compliance reason(s)	Procedure offline; Software st Fall/Rise Time Calibration
User Name	Unknown User
----M8195A - HDMI Sig. Gen.----	
DVI Mode	False
Fill up blanking periods with Null packets	False
Keep the signals after test?	False
Skip Pattern generation	True
----SCDC Controller----	
SCDC supports Character Error Detections	False
Skip Link Training	False
Start delay between SCDC controller and TMDS signal	100 ms
----Dso----	
Use internal probe head termination voltage	True

Result	Video Mode
pass	93: 3840x2160p, Max(24.12 Hz)
pass	93: 3840x2160p, Min(23.86 Hz)
pass	94: 3840x2160p, Max(25.125 Hz)
pass	94: 3840x2160p, Min(24.875 Hz)
pass	95: 3840x2160p, Max(30.15 Hz)
pass	95: 3840x2160p, Min(29.82 Hz)
pass	98: 4096x2160p, Max(24.12 Hz)
pass	98: 4096x2160p, Min(23.86 Hz)
pass	99: 4096x2160p, Max(25.125 Hz)
pass	99: 4096x2160p, Min(24.875 Hz)
pass	100: 4096x2160p, Max(30.15 Hz)
pass	100: 4096x2160p, Min(29.82 Hz)
pass	103: 3840x2160p, Max(24.12 Hz)
pass	103: 3840x2160p, Min(23.86 Hz)
pass	104: 3840x2160p, Max(25.125 Hz)
pass	104: 3840x2160p, Min(24.875 Hz)
pass	105: 3840x2160p, Max(30.15 Hz)
pass	105: 3840x2160p, Min(29.82 Hz)
pass	Test Result

Figure 83 Example result for Test ID 8-30: 4K x 2K Video Format Timing

- Result: (Pass/Fail) Pass indicates that the DUT passed this test step successfully.
- Video Mode: The tested video mode.

ID 8-31 AVI InfoFrame supporting Extended Colorimetry, Content Type and Selectable YCC Quantization Range

Availability

- HDMI 1.4
- Expert Mode

Purpose and Method

This procedure tests for compliance according to HDMI CTS Version 1.4b, Section 8.8 “Sink – Advanced Features”, Test ID 8-31: “AVI InfoFrame supporting Extended Colorimetry, Content Type and Selectable YCC Quantization Range”.

This test verifies that the DUT supports the selected 4K x 2K video formats.

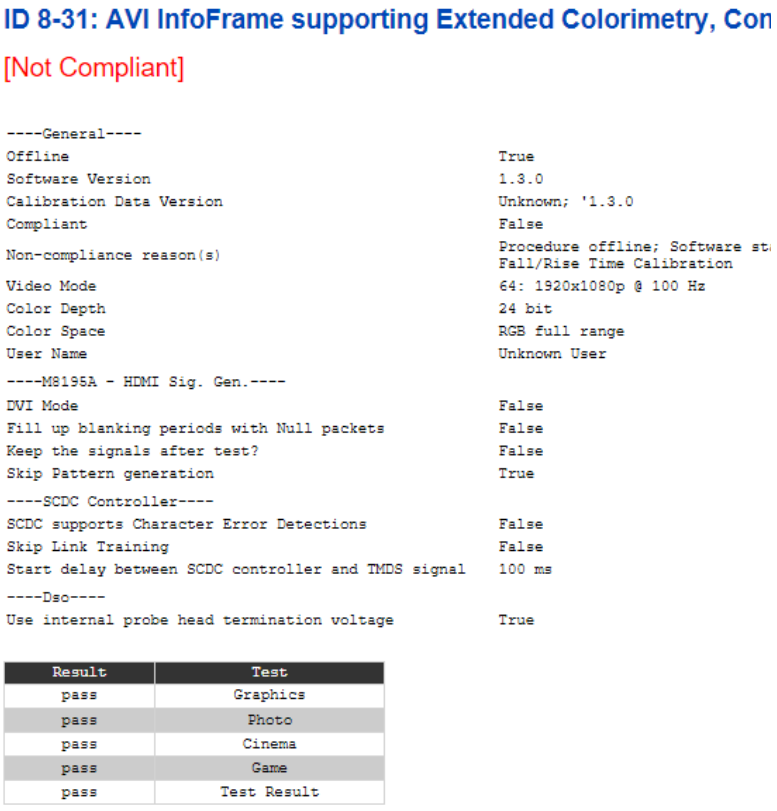
Depending on the combination of supported formats, extended colorimetry, content type and YCC quantization range settings, the software generates valid video signals with a resolution of either 720x480p or 720x576p. Initially, colorimetry video signals are generated. For each video signal, the software prompts you to check if the sink displays the expected video image without errors. Subsequently, different content types are tested, depending on the content types you select.

The test is considered as passed if the DUT displays the expected video images without any errors; else, the test is considered as failed.

Connection Diagram

Refer to Figure 51 on page 116.

Result Description



ID 8-31: AVI InfoFrame supporting Extended Colorimetry, Con

[Not Compliant]

----General----	
Offline	True
Software Version	1.3.0
Calibration Data Version	Unknown; '1.3.0
Compliant	False
Non-compliance reason(s)	Procedure offline; Software st Fall/Rise Time Calibration
Video Mode	64: 1920x1080p @ 100 Hz
Color Depth	24 bit
Color Space	RGB full range
User Name	Unknown User
----M8195A - HDMI Sig. Gen.----	
DVI Mode	False
Fill up blanking periods with Null packets	False
Keep the signals after test?	False
Skip Pattern generation	True
----SCDC Controller----	
SCDC supports Character Error Detections	False
Skip Link Training	False
Start delay between SCDC controller and TMDS signal	100 ms
----Dso----	
Use internal probe head termination voltage	True

Result	Test
pass	Graphics
pass	Photo
pass	Cinema
pass	Game
pass	Test Result

Figure 84 Example result for Test ID 8-31: AVI InfoFrame

- Result: (Pass/Fail) Pass indicates that the DUT passed this test step successfully.
- Test: Type of content. The final entry, “Test Result”, is for the entire test.

Differential Swing

Availability

- Expert Mode only
- TMDS Signal
- For: Clock Channel, Data Channel, All Channels sep

Purpose and Method

This procedure is an extension of the ID 8-5 Differential Swing test.

As defined in the CTS, the differential swing is set to 'All TMDS pairs' in the "ID 8-5 Differential Swing" test. With this additional test procedure, the software enables you to test only the clock, only the data or each channel separately.

In Expert mode, you may use a slider to set differential swing voltage levels (see Figure 85). If 'Use Slider Dialog' is set to 'True', the slider dialog is displayed and if set to 'False', only those voltage levels are tested that are required by the HDMI CTS.

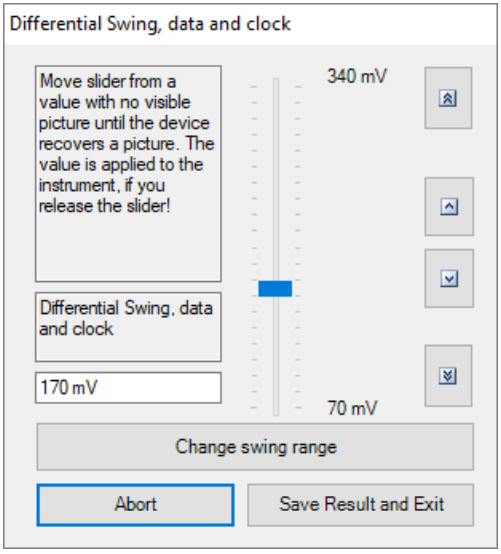


Figure 85 Slider dialog for Differential Swing in Expert Mode

The test is considered as passed if the Sink displays a video image without pixel errors for each step and the minimum voltage level attained is lower than 150 mV; else, the test is considered as failed.

Connection Diagram

Refer to Figure 51 on page 116.

Result Description

ID 8-5 D.Swing Clock_3.3 on Clock

[Not Compliant]

----General----	
Offline	True
Software Version	2023.
Calibration Data Version	Unknown; '1.3.0
Compliant	False
Non-compliance reason(s)	Procedure offline; Software st Calibration Clock-, Swing Cali Data1+, Swing Calibration Data Clock+, Swing Calibration Data
Video Mode	64: 1920x1080p @ 100 Hz
Color Depth	24 bit
Color Space	RGB full range
Use Color Bar pattern	False
Start Differential Swing	170 mV
Minimum Differential Swing	70 mV
Differential Swing Step Size	10 mV
Voltage Offset	3.3 V
User Name	Unknown User
----M8195A - HDMI Sig. Gen.----	
DVI Mode	False
Fill up blanking periods with Null packets	False
Keep the signals after test?	False
Skip Pattern generation	True
----SCDC Controller----	
SCDC supports Character Error Detections	False
Skip Link Training	False
Start delay between SCDC controller and TMDS signal	100 ms
----Dso----	
Use internal probe head termination voltage	True

Result	Channel	Min Passed Diff. Swing [mV]	Min Spec Diff. Swing [mV]	Max Swing Test [V]
pass	Clock	100	150	1.200

Figure 86 Example result for Differential Swing in Expert Mode

- Result: (Pass/Fail) Pass indicates that the DUT passed this test step successfully.
- Channel: The TMDS line where the voltage level is applied.
- Min Passed Diff. Swing [mV]: The minimum differential swing when the DUT passed (separated in each TMDS pair).

- Min Spec Diff. Swing [mV]: The required minimum differential swing voltage level (optionally defined through user-spec instead of CTS).
- Max Swing Test [V]: The maximum applied differential swing voltage level.

Sink Inter-Pair Skew

Availability

- Expert Mode only
- TMDS Signal
- Data0, Data1, Data2, Clock

Purpose and Method

This procedure is not part of the standard compliance tests document. The CTS Version 1.4 does not define an inter-pair skew compliance test for sink devices. The inter-pair skew test is provided by ValiFrame as an extension to the compliance tests. In this procedure, either one of the Data TMDS pairs or the TMDS clock pair is skewed against the residual TMDS pairs. At each step, the skew is increased until the DUT displays an erroneous video image. This is followed by smaller steps decreasing the skew, until the DUT recovers a video image without errors again.

The test is considered as passed if the Sink displays a video image without pixel errors for each step with a skew greater than or equal to the inter-pair skew defined in the HDMI specification; otherwise, the test is considered as failed.

Connection Diagram

Refer to Figure 51 on page 116.

Result Description

Inter Pair Skew Data0

[Not Compliant]

----General----	
Offline	True
Software Version	2023
Calibration Data Version	Unknown; '1.3.0
Compliant	False
Non-compliance reason(s)	Procedure offline; Software st Swing Calibration Clock-, HF S Swing Calibration Data1+, HF S Calibration, HF Swing Calibrat Data2-
Video Mode	96: 3840x2160p @ 50 Hz
Color Depth	24 bit
Color Space	RGB full range
Use Color Bar pattern	False
TMDS data to clock ratio 1:40	True
Use scrambled video signal	True

Skewed Channel [Data0,Data1,Data2 or Clock]	Data0
Maximum Skew	1 TBit
Initial Skew Step Size	100 mTBit
Skew Step Time	1 s
User Name	Unknown User
----M8195A - HDMI Sig. Gen.----	
DVI Mode	False
Fill up blanking periods with Null packets	False
Keep the signals after test?	False
Skip Pattern generation	True
----SCDC Controller----	
SCDC supports Character Error Detections	False
Skip Link Training	False
Start delay between SCDC controller and TMDS signal	100 ms
----Dso----	
Use internal probe head termination voltage	True

Result	Channel	Max Passed Skew [mTBit]	Min Failed Skew [mTBit]	Max Recovery Skew [mTBit]	Min Spec Skew [mTBit]
pass	Data0	1000	Invalid	N/A	1000

Figure 87 Example result for Sink Inter-Pair Skew Test

- Result: (Pass/Fail) Pass indicates that the DUT passed this test step successfully.
- Channel: The TMDS lane where the skew is applied.
- Max Passed Skew [mTBit]: The maximum value of inter-pair skew that the DUT passed.
- Min Failed Skew [mTBit]: The minimum value of inter-pair skew that the DUT failed.
- Max Recovery Skew [mTBit]: The maximum value of inter-pair skew for which the DUT recovered a video image without errors after a failed step.
- Min Spec Skew [mTBit]: The minimum allowed Inter-Pair Skew as specified in the HDMI specification.

Sensitivity to Jitter

Availability

- Expert Mode only
- HDMI 1.4 and HDMI 2.1 TMDS Signal Generator
- For: see Purpose and Method below

Purpose and Method

This procedure is divided into four different variants:

- Sensitivity Jitter Injection via Clock—This test measures the ability of a device to accurately receive valid HDMI signaling with additional jitter applied to the clock input.
- Sensitivity Worst Case Skew for Jitter Tolerance—The purpose of this test is to find the worst case skew for the jitter tolerance test.
- Sensitivity Data Jitter—Sink sensitivity test for jitter on data. This test measures the ability of a device to accurately receive valid HDMI signaling with additional jitter applied to the inputs.
- Sensitivity Clock Jitter—Sink sensitivity test for jitter on clock. This test measures the ability of a device to accurately receive valid HDMI signaling with additional jitter applied to the inputs.

For the Jitter Injection via Clock test, the 'Inject 2 Frequencies Jitter on Clock' dialog as shown in Figure 88 sets the data and clock jitter values.

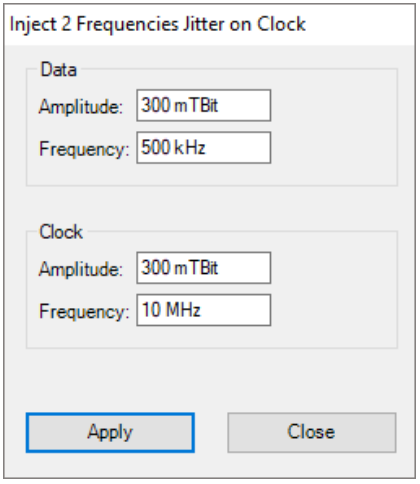


Figure 88 Parameter Setup dialog in Sensitivity Jitter Injection via Clock test

For the other sensitivity tests, the 'Parameter Setup Dialog' as shown in Figure 89 sets the desired differential swing and transition time converter values. When you click the "Set" button, a valid HDMI video signal is generated. In each step of the procedures, periodic jitter values are increased at different frequencies and are applied to the video signal.

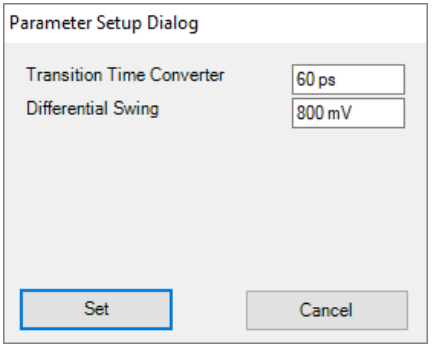


Figure 89 Parameter Setup Dialog in Sensitivity Jitter test

Connection Diagram

Refer to Figure 51 on page 116.

Result Description

Sensitivity Jitter Injection via Clock

[Not Compliant]

Sensitivity Jitter via Clock

----General----	
Offline	True
Software Version	2023.12.4.1558_InternalInstall
Calibration Data Version	Unknown; '1.3.0.9_RC
Compliant	False
Non-compliance reason(s)	Procedure offline; Software st Swing Calibration Clock-, HF S Swing Calibration Data1+, HF S Calibration, HF Swing Calibrat Data2-
Video Mode	96: 3840x2160p @ 50 Hz
Color Depth	24 bit
Color Space	RGB full range
Use Color Bar pattern	False
Cable Emulator	HDMI 2 0 NO SKEW
TMDS data to clock ratio 1:40	True
Use scrambled video signal	True
User Name	Unknown User

----M8195A - HDMI Sig. Gen.----	
DVI Mode	False
Fill up blanking periods with Null packets	False
Keep the signals after test?	False
Skip Pattern generation	True
----SCDC Controller----	
SCDC supports Character Error Detections	False
Skip Link Training	False
Start delay between SCDC controller and TMDS signal	100 ms
----Dso----	
Use internal probe head termination voltage	True

Result	Data Jitter Amplitude [TBit]	Data Jitter Frequency [MHz]	Clock Jitter Amplitude [TBit]	Clock Jitter Frequency [MHz]
pass	0.300	0.500	0.300	10.000

Figure 90 Example result for Sensitivity Jitter Injection via Clock Test

- Result: (Pass/Fail) Pass indicates that the DUT passed this test step successfully.
- Data Jitter Amplitude [TBit]: The amplitude of the jitter applied to the data.
- Data Jitter Frequency [MHz]: The frequency of the jitter applied to the data.
- Clock Jitter Amplitude [TBit]: The amplitude of the jitter applied to the clock.
- Clock Jitter Frequency [MHz]: The frequency of the jitter applied to the clock.

HF: Intra-Pair Skew

Availability

- Expert Mode only
- HDMI 2.1 TMDS Signal
- Data0, Data1, Data2, Clock Channel
- Vicm = 2.8, 3.3 V

Purpose and Method

This test is run for the characterization of the DUT. It is based on HDMI Sink CTS Version 2.1i, Section 5.1.1.1 “Sink TMDS ELectrical 6G Tests”, HF2-2: “Sink TMDS Electrical – 6G – Intra-Pair Skew” and “HF2-2 Keysight MOI v1.0c” but deviates from the test method described in the document. Therefore, the result cannot be considered for compliance validation.

In this procedure, an additional generator is used and the setup is changed in such a manner that the required intra-pair skew value is applied without adding delay lines.

The generated clock is not compliant according to the “HF2-2: Sink TMDS Electrical – 6G – Intra Pair Skew” test. However, this method may be used for quick characterization of intra-pair skew, since the clock might have less impact on the result of intra-pair skew on TMDS Data.

Connection Diagram

Refer to Figure 51 on page 116.

Result Description

HF: Intra-Pair Skew Data0 2.8 Vicm

[Not Compliant]

----General----	
Offline	True
Software Version	2023
Calibration Data Version	Unknown; '1.3.0
Compliant	False
Non-compliance reason(s)	Procedure offline; Software st. Fall/Rise Time Calibration
Video Mode	96: 3840x2160p @ 50 Hz
Color Depth	24 bit
Color Space	RGB full range
Use Color Bar pattern	False
Cable Emulator	HDMI 2 0 NO SKEW

TMDS data to clock ratio 1:40	True
Use scrambled video signal	True
Minimum Skew	-695 mTBit
Maximum Skew	695 mTBit
Skew Step Size	100 mTBit
User Name	Unknown User
----M8195A - HDMI Sig. Gen.----	
DVI Mode	False
Fill up blanking periods with Null packets	False
Keep the signals after test?	False
Skip Pattern generation	True
----SCDC Controller----	
SCDC supports Character Error Detections	False
Skip Link Training	False
Start delay between SCDC controller and TMDS signal	100 ms
----Dso----	
Use internal probe head termination voltage	True

Result	Channel	Max Passed Skew [mTBit]	Min Failed Skew [mTBit]	Max Recovery Skew [mTBit]	Spec. Skew [mTBit]
pass	Data0+	695	N/A	N/A	695
pass	Data0-	-695	N/A	N/A	695

Figure 91 Example result for HF Intra-Pair Skew Test

- Result: (Pass/Fail) Pass indicates that the DUT passed this test step successfully.
- Channel: The TMDS line where the intra-pair skew is applied.
- Max Passed Skew [mTBit]: The maximum value of intra-pair skew for which the DUT passed.
- Min Failed Skew [mTBit]: The minimum value of intra-pair skew for which the DUT failed.
- Max Recovery Skew [mTBit]: The maximum value of intra-pair skew for which the DUT recovered an error-ridden video image after a failed step.
- Spec. Skew [mTBit]: Required minimum skew as defined in the CTS.

Generic Video Format Timing

Availability

- Expert Mode only
- TMDS Signal

Purpose and Method

This procedure is not part of the standard compliance tests document. This test is an extension to all the other Sink Video Format Timing tests. With this procedure, you are allowed to test any Video Format, Color Depth, Color Space and 3D mode using user-defined frame-rate deviations. You may use this procedure either to characterize or to debug a DUT.

For the given video format and frequency combination, two video signals are generated. The first signal includes a pixel clock frequency deviation as defined in “Positive Framerate deviation” and the second signal includes a pixel clock frequency deviation as defined in “Negative Framerate deviation”.

The test is considered as passed if the Sink displays the expected video image at both deviations; else, the test is considered as failed.

Connection Diagram

Refer to Figure 51 on page 116.

Result Description

Generic Video Format Timing

[Not Compliant]

----General----	
Offline	True
Software Version	2023
Calibration Data Version	Unknown; '1.3.0
Compliant	False
Non-compliance reason(s)	Procedure offline; Software st Fall/Rise Time Calibration
Video Mode	96: 3840x2160p @ 50 Hz
Color Depth	24 bit
Color Space	RGB full range
Use Color Bar pattern	True
3D mode	2D
Negative Framerate deviation	-0.5 %
Positive Framerate deviation	0.5 %
Use scrambled video signal	False
TMDS data to clock ratio 1:40	False
User Name	Unknown User
----M8195A - HDMI Sig. Gen.----	
DVI Mode	False
Fill up blanking periods with Null packets	False
Keep the signals after test?	False
Skip Pattern generation	True
----SCDC Controller----	
SCDC supports Character Error Detections	False
Skip Link Training	False
Start delay between SCDC controller and TMDS signal	100 ms
----Dso----	
Use internal probe head termination voltage	True

Result	Video Mode
pass	Testing video mode: 96: 3840x2160p @ 50 Hz, Color Space: RGB_full_range, Color Depth: _24_bit, 3D mode: _2D at frame rate: 50.25 (Max)
pass	Testing video mode: 96: 3840x2160p @ 50 Hz, Color Space: RGB_full_range, Color Depth: _24_bit, 3D mode: _2D at frame rate: 49.75 (Min)
pass	Test Result

Figure 92 Example result for Generic Video Format Timing Test

- Result: (Pass/Fail) Pass indicates that the DUT passed this test step successfully.
- Video Mode: The tested video mode. The final entry, “Test Result”, is for the entire test.

Additional HDMI 2.1 FRL Signal Sink Tests in Expert Mode

The tests described in this section are available only in Expert Mode and are intended for custom characterization and debugging of FRL signal sink DUTs.

Differential Swing Tolerance

Availability

- Expert Mode only
- HDMI 2.1 FRL Signal
- Perform test at the minimum and maximum supported FRL data rates

Purpose and Method

This procedure tests for compliance according to HDMI Sink CTS Version 2.1i, Section 5.2.1.1 “Sink FRL Electrical Tests”, HFR2-1: “Sink FRL Electrical - Min/Max Differential Swing Tolerance” and “HFR2-1 Keysight MOI v1.0d”.

An FRL Gap character pattern (that is, RXSB33PAT, as defined in the CTS) is generated with calibrated voltage levels and without any jitter applied. HFR2-1 Differential Swing Tolerance on page 155 can be performed to find the maximum swing values, whereas the Expert Mode test described here is used to find the minimum swing value.

In Expert mode, the procedure can be used for the characterization of the DUT by changing the “Start Differential Swing” value and the step size. In this case, the differential swing voltage level is decreased from the start value until the DUT fails to support the signal without errors.

This test must be conducted for the highest and lowest supported data rates.

Connection Diagram

Refer to Figure 51 on page 116.

Result Description

HFR2-1 3Gbps Min Differential Swing Tolerance

[Not Compliant]

----General----	
Offline	True
Software Version	2023
Calibration Data Version	Unknown
Compliant	False
Non-compliance reason(s)	Procedure offline; Software status Lane2+_FrlLinkRate_3Gbps_ThreeLane, Calibration Lane0+_FrlLinkRate_3Gbp Calibration Lane1-_FrlLinkRate_3Gbp Lane1+_FrlLinkRate_3Gbps_ThreeLane, Lane2-_FrlLinkRate_3Gbps_ThreeLane
Video Mode	FRL0 (3 Lanes) : RXSB33PAT @ 3 GBit
Start Differential Swing	170 mV
Minimum Differential Swing	100 mV
Differential Swing Step Size	10 mV
Voltage Offset	3.3 V
Starting Pattern on Lane 0	LTP5 - LFSR0 4096 FRL Characters
Starting Pattern on Lane 1	LTP6 - LFSR1 4096 FRL Characters
Starting Pattern on Lane 2	LTP7 - LFSR2 4096 FRL Characters
User Name	Unknown User
----M8195A - HDMI Sig. Gen.----	
DVI Mode	False
Fill up blanking periods with Null packets	False
Keep the signals after test?	False
Skip Pattern generation	True
----SCDC Controller----	
SCDC supports Character Error Detections	False
Skip Link Training	False
Start delay between SCDC controller and TMDS signal	100 ms
----Dso----	
Use internal probe head termination voltage	True

Result	Vicm	Passed Diff. Swing [mV]	Link Training	FRL Start	BER [ ]	Cumulative Errors []	Iterations []	Total Measurement Interval [s]	Total Bits Processed [ ]
pass	V_icm1 (3.3V)	100	True	True	0.000E+000	0	10	111.1000	1.045E+012

Figure 93 Example result for Differential Swing Tolerance (min swing)

- Result: (Pass/Fail) Pass indicates that the DUT passed this test step successfully.
- V icm: The common mode voltage Level.
- Passed Diff. Swing [mV]: The minimum differential swing when the DUT passed (separated for each FRL pair).
- Link Training: Value is ‘True’ if link training is successful.

- FRL Start: Value is 'True' if the "FRL_Start" flag is set true (1) in the DUT after link training is performed.
- BER: Measured Bit Error Ratio.
- Cumulative Errors: Number of errors in all lanes during the BER test.
- Iterations: Number of iterations into which the BER measurement is divided.
- Total Measurement Interval [s]: The duration of the BER test in seconds.
- Total Bits Processed: The number of bits processed during the BER test.

FRL Error Pattern Check

Availability

- Expert Mode only
- HDMI 2.1 FRL Signal
- Perform test at the minimum and maximum supported FRL data rates

Purpose and Method

This test checks the ability of a device to detect the errors in an FRL input signal.

An FRL signal is generated with calibrated voltage levels and without jitter applied. The V_{ICM} is set to 3.135 V and the differential swing voltage is set to 1 V.

Thereafter, link training is performed between the Sink DUT and the FRL Signal Generator for the selected FRL rate. If the link training passes, the FRL test patterns are applied without errors initially, followed by patterns with a single disparity error. The software performs a BER test for each case. In the latter scenario, the number of cumulative errors should be greater than zero. This process is repeated as many times as defined in the “Number of Steps” parameter.

This test must be conducted for the highest and the lowest supported data rates.

Connection Diagram

Refer to Figure 51 on page 116.

Result Description

FRL Error Injection 3Gbps

[Not Compliant]

----General----	
Offline	True
Software Version	2023
Calibration Data Version	Unknown
Compliant	False
Non-compliance reason(s)	Procedure offline; Software status Lane2+_FrlLinkRate_3Gbps_ThreeLane, Calibration, FRL Swing Calibration Lane0-_FrlLinkRate_3Gbps_ThreeLane, Lane0+_FrlLinkRate_3Gbps_ThreeLane, Lane1-_FrlLinkRate_3Gbps_ThreeLane,
Video Mode	FRL0 (3 Lanes) : RXSB33PAT @ 3 GBit
Cable Emulator	None
Enable Crosstalk	False
Number of Steps	3
Starting Pattern on Lane 0	LTP5 - LFSR0 4096 FRL Characters
Starting Pattern on Lane 1	LTP6 - LFSR1 4096 FRL Characters
Starting Pattern on Lane 2	LTP7 - LFSR2 4096 FRL Characters
User Name	Unknown User
----M8195A - HDMI Sig. Gen.----	
DVI Mode	False
Fill up blanking periods with Null packets	False
Keep the signals after test?	False
Skip Pattern generation	True
----SCDC Controller----	
SCDC supports Character Error Detections	False
Skip Link Training	False
Start delay between SCDC controller and TMDS signal	100 ms
----Dso----	
Use internal probe head termination voltage	True

Result	FRL Pattern	Link Training	FRL Start	BER [ ]	Cumulative Errors []	Iterations []	Measurement Interval [s]	Bits Processed [ ]
*** FAIL ***	RXSB33PAT	True	True	0.000E+000	0	10	111.1000	1.045E+012
pass	Error Pattern	True	True	3.659E-010	121956	10	111.1000	1.045E+012
*** FAIL ***	RXSB33PAT	True	True	0.000E+000	0	10	111.1000	1.045E+012
pass	Error Pattern	True	True	3.661E-010	122006	10	111.1000	1.045E+012
*** FAIL ***	RXSB33PAT	True	True	0.000E+000	0	10	111.1000	1.045E+012
pass	Error Pattern	True	True	3.662E-010	122056	10	111.1000	1.045E+012

Figure 94 Example result for FRL Error Pattern Check

- Result: (Pass/Fail) Pass indicates that the DUT passed this test step successfully.
- FRL Pattern: The pattern applied to the FRL lanes for the BER test.
- Link Training: Value is ‘True’ if link training is successful.

- FRL Start: Value is 'True' if the "FRL_Start" flag is set true (1) in the DUT after link training is performed.
- BER: Measured Bit Error Ratio.
- Cumulative Errors: Total number of errors in all the iterations of the BER test.
- Iterations: Number of iterations into which the BER measurement is divided.
- Measurement Interval: The total duration of the BER test in seconds.
- Bits Processed: The total number of bits processed during the BER test.

Jitter Characterization Test

Availability

- Expert Mode only
- HDMI 2.1 FRL Signal
- Perform test at the maximum supported FRL data rate

Purpose and Method

The purpose of this procedure is to search for the maximum sinusoidal jitter that the Sink DUT can tolerate at a specific frequency.

For that, the data generator sets the sinusoidal jitter amplitude to “Start SJ pk-pk” and increases that value in steps of 100 mUI until the BER test fails. Then a binary search algorithm is used between the last point that passes and the first point that fails. When the BER test passes it goes forward and when the test fails it goes down. At each step, the step size is reduced until the target resolution is reached.

This test can be conducted for the highest and lowest supported data rates.

Connection Diagram

Refer to Figure 51 on page 116.

Result Description

FRL Jitter Characterization 3Gbps @66.66 MHz

[Not Compliant]

----General----	
Offline	True
Software Version	2023
Calibration Data Version	Unknown
Compliant	False
Non-compliance reason(s)	Procedure offline; Software status Lane2+_FrlLinkRate_3Gbps_ThreeLane, Calibration, FRL Swing Calibration Lane0-_FrlLinkRate_3Gbps_ThreeLane, Lane0+_FrlLinkRate_3Gbps_ThreeLane, Lane1-_FrlLinkRate_3Gbps_ThreeLane,
Video Mode	FRL0 (3 Lanes) : RXSB33PAT @ 3 GBit
Cable Emulator	HDMI 2 1 WCM3
Starting Pattern on Lane 0	LTP5 - LFSR0 4096 FRL Characters
Starting Pattern on Lane 1	LTP6 - LFSR1 4096 FRL Characters
Starting Pattern on Lane 2	LTP7 - LFSR2 4096 FRL Characters
Start SJ pk-pk	100 mUI
RJ pk-pk	100 mUI
PCB loss dB	1 dB
SJ Frequency	66.66 MHz
Enable Crosstalk	True
User Name	Unknown User
----M8195A - HDMI Sig. Gen.----	
DVI Mode	False
Fill up blanking periods with Null packets	False
Keep the signals after test?	False
Skip Pattern generation	True
----SCDC Controller----	
SCDC supports Character Error Detections	False
Skip Link Training	False
Start delay between SCDC controller and TMDS signal	100 ms
----Dso----	
Use internal probe head termination voltage	True

Result	SJ Amplitude [mUI]	Link Training	FRL Start	BER [ ]	Cumulative Errors []	Iterations []	Total Measurement Interval [s]	Total Bits Processed [ ]
pass	100	True	True	0.000E+000	0	10	111.1000	1.045E+012
pass	200	True	True	0.000E+000	0	10	111.1000	1.045E+012
pass	300	True	True	0.000E+000	0	10	111.1000	1.045E+012
pass	400	True	True	0.000E+000	0	10	111.1000	1.045E+012
pass	500	True	True	0.000E+000	0	10	111.1000	1.045E+012
pass	600	True	True	0.000E+000	0	10	111.1000	1.045E+012
pass	700	True	True	0.000E+000	0	10	111.1000	1.045E+012
pass	800	True	True	0.000E+000	0	10	111.1000	1.045E+012
pass	900	True	True	0.000E+000	0	10	111.1000	1.045E+012
pass	1000	True	True	0.000E+000	0	10	111.1000	1.045E+012

Figure 95 Example result for Jitter Characterization Test

- Result: (Pass/fail) Pass indicates that the DUT passed this test step successfully.
- SJ Amplitude [mUI]: The SJ amplitude added to the signal in this step.
- Link Training: True if the link training was successful.
- FRL Start: True if the FRL_start flag is set to True (1) in the DUT after link training.
- BER: Measured Bit Error Ratio.
- Cumulative Errors: Total number of errors in the BER test.
- Iterations: Number of iterations into which the BER measurement is divided.
- Total Measurement Interval [s]: The duration of the BER test in seconds.
- Total Bits Processed: The number of bits processed during the BER test.

8 HDMI Receiver Tests for Cables

Once the HDMI PHY Test Station has been calibrated, receiver test procedures can be run. The tests described in this chapter are for cable DUTs, most of which are required for compliance. The test described in the final section is available only in expert mode and is intended for custom characterization and debugging of cable DUTs.

Overview

HDMI cable electrical compliance testing is conducted by applying a stressed signal and measuring the output with a digital oscilloscope.

There are two test cases that are covered by compliance testing for Category 1 and Category 2 cables:

- Cable Eye Mask Measurement
- Cable Inter-Pair Skew Measurement

These are performed only for 74.25 MHz, 165 MHz and 340 MHz data rates.

For Category 3 cables, there are four test cases for compliance testing:

- DC Power Test
- Cable Eye Diagram
- Inter-Pair Skew
- Mode Conversion

whereby the latter two are available only for Active Cables.

ValiFrame automatically determines which tests are required according to the Cable Category. Additionally, whether it is an Active Cable (check box in Configure Product dialog) plays a role.

Tests for Category 1 and 2 Cables

ID 5-3 Cable Eye Mask Measurement

Availability

- HDMI 1.4 and HDMI 2.1 TMDS Signal
- Category 1, Category 2 cables
- Compliance Mode, Expert Mode
- Data0, Data1, Data2, Clock

Purpose and Method

This procedure tests for compliance according to HDMI CTS Version 1.4b, Section 5.2 “Cable – Electrical: Performance Tests”, Test ID 5-3: “TMDS Data Eye Diagram”.

Depending on the cable category, a video signal with a data rate of 74.25 MHz (Cat1) or 165 MHz and 340 MHz (Cat2) is generated and jitter applied.

The test is considered as passed when the cable assembly outputs a compliant data eye; else, the test is considered as failed.

Connection Diagram

The oscilloscope must be connected according to the data lane being tested.

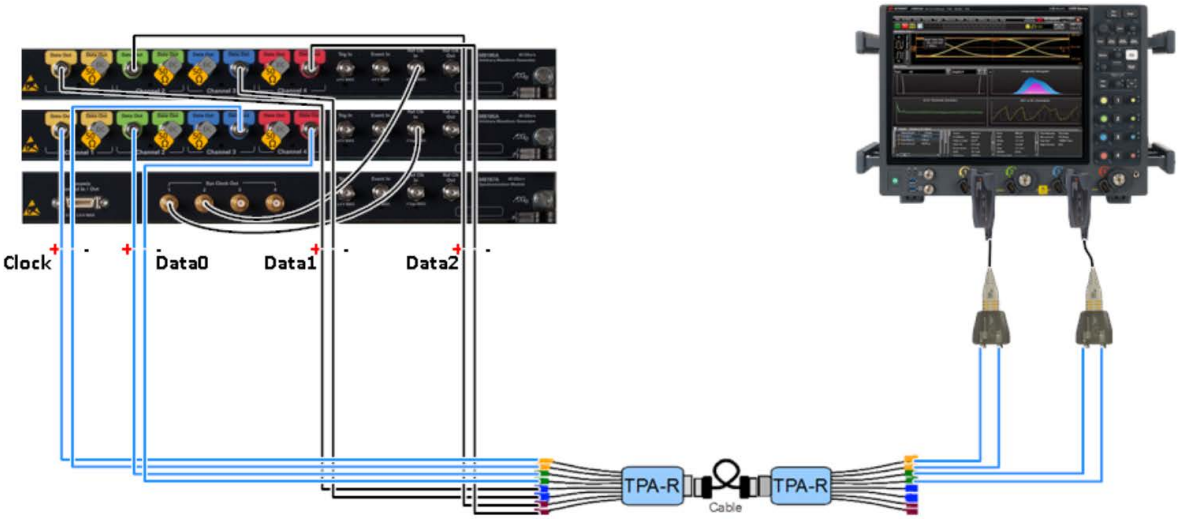


Figure 96 Example connection diagram for Test ID 5-3 Cable Eye Mask Measurement.Two-channel scope connection

Result Description

5-3 Cbl. Eye at 165 MHz D0

[Not Compliant]

Test 5-3 Cable Data Eye for Cable Category Cat_2 Jitter only on Clock

----General----	
Offline	True
Software Version	2023
Calibration Data Version	Unknown; '1.3.0
Compliant	False
Non-compliance reason(s)	Procedure offline; Software status unr Data1+, Swing Calibration Data2+, Swin 1280x1024p111Hz24, Swing Calibration C unknown/unreleased: Skew Calibration, Clock-, Swing Calibration Data0-, Swin
CTS Revision	1.4b
Video Mode	138: 1280x1024p @ 111 Hz
Color Depth	24 bit
Color Space	RGB limited range
Use Color Bar pattern	False
Differential Swing	800 mV
Cable Category	Category 2 (Home)
Mask Movement Type	Find Pass
Check worst case eye manually	False
Measure current on HPD +5V_Power	False
User Name	Unknown User
----M8195A - HDMI Sig. Gen.----	
Fill up blanking periods with Null packets	False
Keep the signals after test?	False
Skip Pattern generation	True
----Dso----	
Use internal probe head termination voltage	True

Result	Data Jitter Amplitude [TBit]	Data Jitter Frequency [MHz]	Mask Violations []
pass	0.190	0.5	0

Figure 97 Example result for Test ID 5-3: Cable Eye Mask Measurement

- Result: (Pass/Fail) Pass indicates that the DUT passed this test step successfully.
- Data Jitter Amplitude [TBit]: Injected data jitter amplitude.
- Data Jitter Frequency [MHz]: Frequency of the data jitter.
- Mask Violations: Number of waveforms violating the eye mask.

ID 5-5 Cable Inter-Pair Skew Measurement

Availability

- HDMI 1.4 and HDMI 2.1 TMDS Signal
- Category 1, Category 2 cables
- Expert Mode; for Active Cables also Compliance Mode
- Data0, Data1, Data2

Purpose and Method

This procedure tests for compliance according to HDMI CTS Version 1.4b, Section 5.3 “Cable – Electrical: Parametric Tests”, Test ID 5-5: “Inter-Pair Skew”.

Depending on the cable category, a video signal with a data rate of 74.25 MHz, 165 MHz or 340 MHz is generated and jitter applied. The skew between all TMDS data pairs is measured.

The test is considered as passed if the cable inter-pair skew is less than or equal to that specified in the CTS; else, the test is considered as failed.

Connection Diagram

The oscilloscope must be connected according to the inter-pair skew being tested.

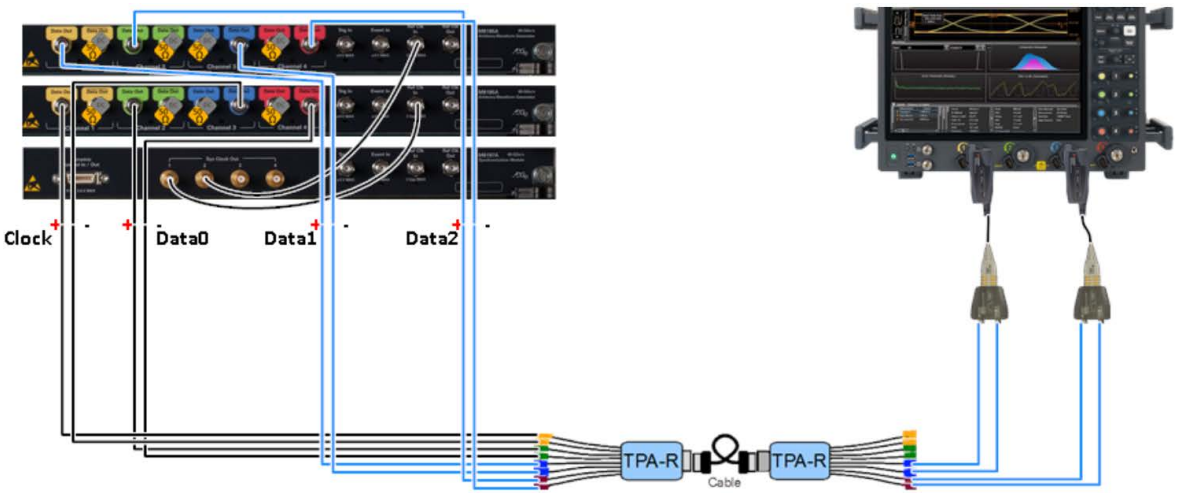


Figure 98 Example connection diagram for Test ID 5-3 Cable Inter-Pair Skew Measurement

Result Description

5-5 Cable Inter-Pair D1-D2

[Not Compliant]

Test 5-5 Cable Inter-Pair Skew for Cat_2 Cable Data 1 - Data 2

----General----	
Offline	True
Software Version	2023
Calibration Data Version	Unknown; '1.3.0
Compliant	False
Non-compliance reason(s)	Procedure offline; Software status unr Time Calibration
CTS Revision	1.4b
Video Mode	138: 1280x1024p @ 228.5 Hz
Color Depth	24 bit
Color Space	RGB limited range
Use Color Bar pattern	False
Differential Swing	800 mV
Cable Category	Category 2 (Home)
Measurement Threshold	0 V
Hysteresis	10 mV
Maximum Tries	3
Additional Sync Pattern	None
Additional Guard Band Pattern	None
Inter-Pair Skew Trigger Length	20 Bits
User Name	Unknown User
Cable Equalizer	5m Cable Equalizer
----M8195A - HDMI Sig. Gen.----	
Fill up blanking periods with Null packets	False
Keep the signals after test?	False
Skip Pattern generation	True
----Dso----	
Use internal probe head termination voltage	True

Result	Cable Skew [ns]	Max. Spec. [ns]
pass	0.00	1.78

Figure 99 Example result for Test ID 5-5: Cable Inter-Pair Skew Measurement

- Result: (Pass/Fail) Pass indicates that the DUT passed this test step successfully.
- Cable Skew [ns]: Measured inter-pair skew.
- Max. Spec. [ns]: Maximum skew as defined in the HDMI specification.

Tests for Category 3 (FRL) Cables

HFR7-1 DC Power Test

Availability

- HDMI 2.1 FRL Signal
- Category 3 cables
- Compliance Mode, Expert Mode

Purpose and Method

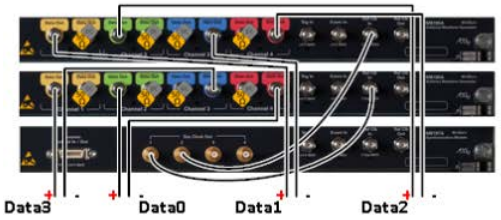
This procedure tests for compliance according to HDMI Generic CTS Version 2.1c for Cat 3 Cables, Section 7.1 “FRL Data Lane Parametric Electrical Tests”, HFR 7-1: “DC Power Test”. This test confirms that a cable assembly can supply at least 50 mA on the +5 V Power Pin to a sink while not requiring more than 55 mA input.

With the sink powered off, the source-side power supply must be set to 5.3 V and the current drawn at the sink side to 50 mA. Then the voltage and the current of the cable must be measured. This is repeated with the source-side power supply set to 4.8 V.

With the sink powered on, the source-side power supply must be set to 5.3 V and the current drawn at the sink side to 10 mA. Then the Vhpd, the voltage and the current of the cable, and the Vpk-pk of each lane must be measured. This is repeated with the source-side power supply set to 4.8 V.

If the measured cable voltage is between 4.7 and 5.3 V and the measured current is below 55 mA, the test is passed; otherwise, the test is failed.

Connection Diagram



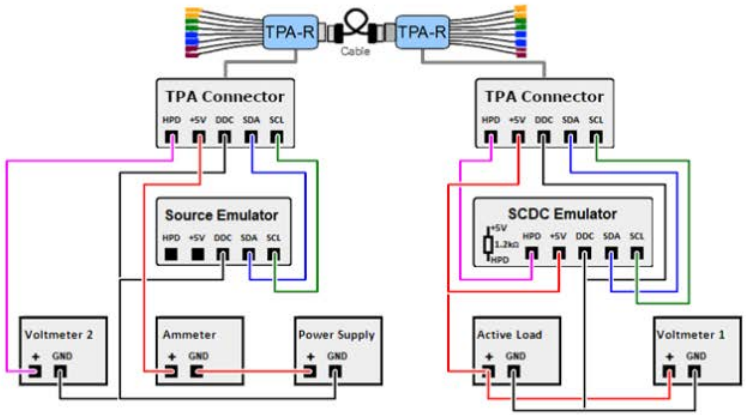


Figure 100 Example connection diagram for Cable DC Power Test (Sink Condition: PoweredOff)

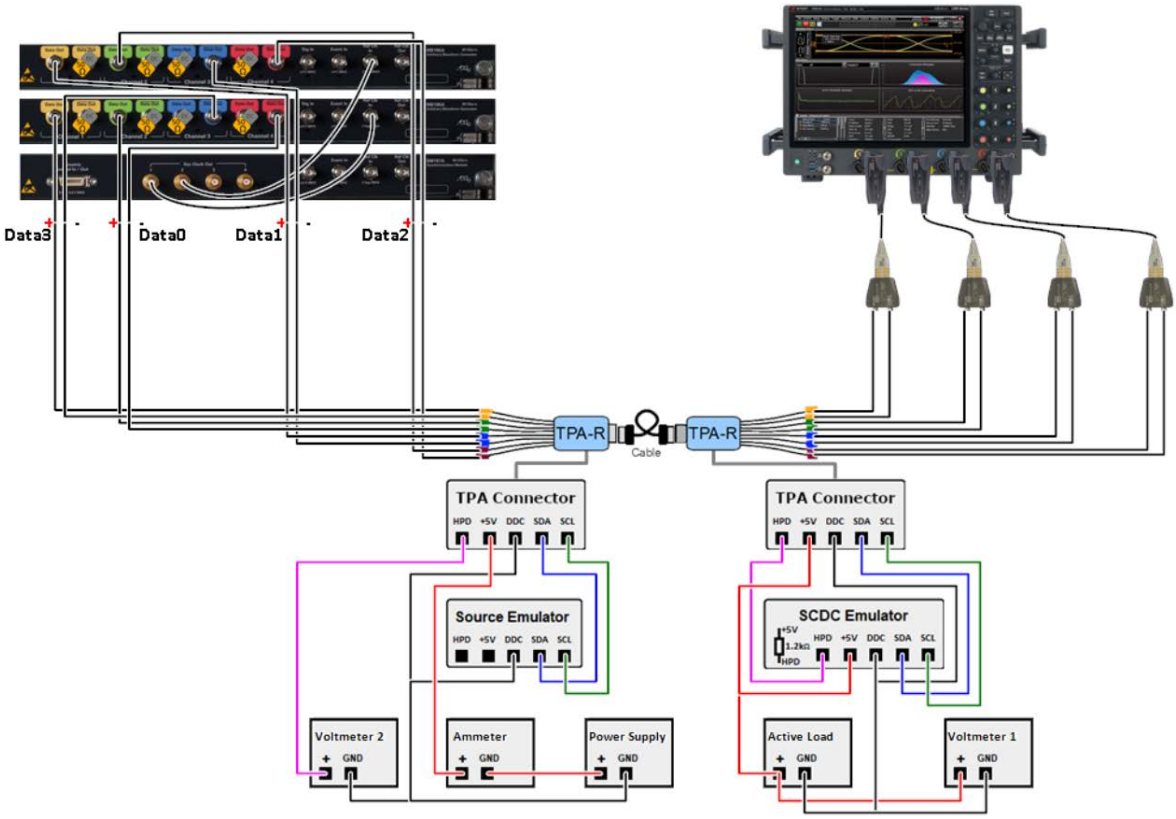


Figure 101 Example connection diagram for Cable DC Power Test (Sink Condition: PoweredOn)

Result Description

HFR7-1 DC Power Test

[Not Compliant]

----General----	
Offline	True
Software Version	2023
Calibration Data Version	Unknown
Compliant	False
Non-compliance reason(s)	Procedure offline; Software status unre Lane1+_FrlLinkRate_12Gbps_FourLane, FRI Calibration Lane3+_FrlLinkRate_12Gbps_F Lane0-_FrlLinkRate_12Gbps_FourLane, FRI Calibration Lane2-_FrlLinkRate_12Gbps_F Calibration Lane0+_FrlLinkRate_12Gbps_F Swing Calibration Lane2+_FrlLinkRate_12
gCTS Revision	2.1h
MOI Revision	v1d
Cable Emulator	None
Enable Crosstalk	False
Pext required	False
V_drop TP1	300 mV
V_drop TP2	0 V
User Name	Unknown User
Cable Equalizer	Off
----M8195A - HDMI Sig. Gen.----	
Fill up blanking periods with Null packets	False
Keep the signals after test?	False
Skip Pattern generation	True
----Dso----	
Use internal probe head termination voltage	True

Result	Sink Condition	Voutput [V]	Vcable [V]	Read EDID	Current [mA]	Vhpd [V]	Vpk [L0;L1;L2;L3]
pass	PoweredOffSink	5.600	5.000	Pass	50.000	-	N/A
pass	PoweredOffSink	5.100	5.000	Pass	50.000	-	N/A
pass	PoweredOnSink	5.360	5.000	Pass	50.000	5.000	5 V, 5 V, 5 V, 5 V
pass	PoweredOnSink	4.860	5.000	-	50.000	-	5 V, 5 V, 5 V, 5 V

Figure 102 Example result for HFR7-1: DC Power Test

- Result: (pass/fail) Result is pass if the cable complies with the conditions given in the CTS, otherwise fail.
- Sink Condition: Either Powered Off or Powered On.
- Voutput [V]: The set output voltage of the power supply.
- Vcable [V]: The measured output voltage of the cable under test.
- Read EDID: Pass if it was possible to read the EDID.
- Current [mA]: The current from the power supply.

- Vhpd [V]: HPD voltage at the source side of the cable. Not applicable for the powered-off state.
- Vpk [L0; L1; L2; L3]: Measured peak voltage of each lane. Not applicable for the powered-off state.

HFR7-21 Cable Eye Diagram

Availability

- HDMI 2.1 FRL Signal
- Category 3 cables
- Compliance Mode, Expert Mode

Purpose and Method

This procedure tests for compliance according to the HDMI Generic CTS Version 2.1h for Cat_3 Cables, Section 7.4 “Eye Diagram Tests”, HFR7-21: “Cable Eye Diagram”. It verifies that the cable meets the eye diagram requirements defined in the spec.

It is performed for 12 Gbps FRL data rate and for all lanes. The pattern applied to each FRL lane of the DUT cable is: LTP5, LTP6, LTP7 and LTP8, respectively. The jitter settings are set to the worst case.

When the cable assembly outputs a compliant eye diagram, the test is passed; otherwise, the test is failed.

Connection Diagram

The oscilloscope must be connected according to the lane being tested and the unused lanes must be terminated.

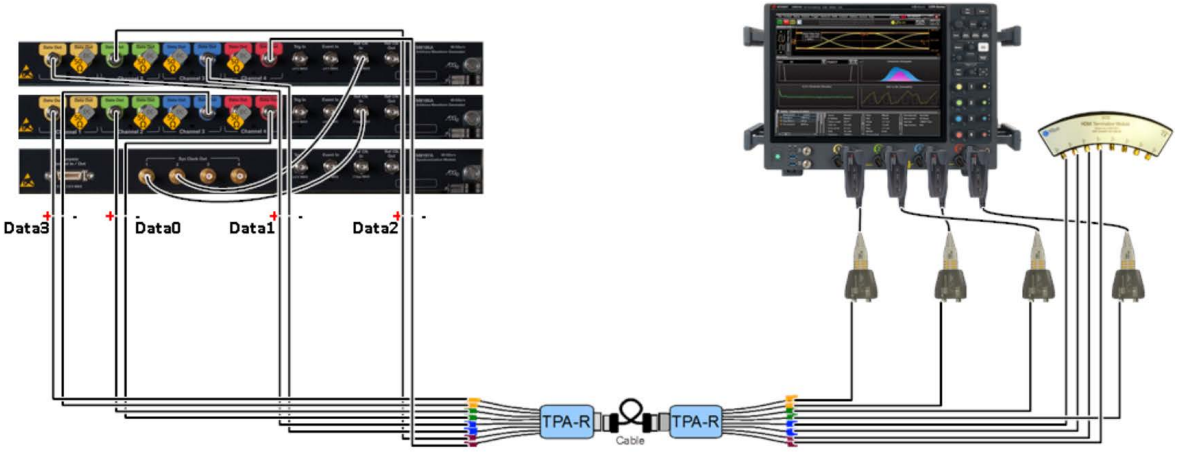


Figure 103 Example connection diagram for HFR7-21: Cable Eye Diagram

Result Description

HFR7-21 Data Eye - FrlLane3

[Not Compliant]

----General----	
Offline	True
Software Version	2023
Calibration Data Version	Unknown; '2023
Compliant	False
Non-compliance reason(s)	Procedure offline; Software status unr Lane2+_FrlLinkRate_12Gbps_FourLane, FR Calibration Lane3+_FrlLinkRate_12Gbps_ L2; Required cal offline: Skew Calibra Swing Calibration Lane0-_FrlLinkRate_1 Cable Swing Calibration Lane3-_FrlLink Calibration, FRL Cable Swing Calibrati Lane0-_FrlLinkRate_12Gbps_FourLane, FR Calibration Lane3-_FrlLinkRate_12Gbps_
gCTS Revision	2.1h
MOI Revision	v1d
FRLTurnOnInterpolation	OFF
Start CTLE (dB)	1
User Name	Unknown User
----M8195A - HDMI Sig. Gen.----	
Fill up blanking periods with Null packets	False
Keep the signals after test?	False
Skip Pattern generation	True
----Dso----	
Use internal probe head termination voltage	True

Result	AVcc [V]	Lane	Eye Width [ps]	Eye Height [mV]	Mask Failures []	CTLE [dB]
pass	3.135	FrlLane3	60.000	500.000	0.000	1.000

Figure 104 Example result for HFR7-21: Cable Eye Diagram

- Result: (pass/fail) Pass means the eye is within the spec.
- AVcc [V]: The AVcc voltage set on the DC power supply.
- Lane: The lane measured (0, 1, 2, or 3).
- Eye Width [ps]: The eye width measured for the tested lane.
- Eye Height [mV]: The eye height measured for the tested lane.
- Mask Failures: Number of times that the cable eye violates the compliance mask.
- CTLE [dB]: The applied CTLE.

HFR7-22 Inter-Pair Skew

Availability

- HDMI 2.1 FRL Signal
- Category 3 cables
- Compliance Mode, Expert Mode
- Only for Active Cables

Purpose and Method

This procedure tests for compliance according to HDMI Generic CTS Version 2.1h, Section 7.5 “Active Cable Assembly Electrical Tests”, HFR7-22: “Inter-Pair Skew”. This test measures the difference in time between any two FRL data lanes of an active cable.

In compliance mode the FRL data rates tested are 3 Gbps, 6 Gbps and 12 Gbps. The patterns applied to the FRL lanes of the DUT cable are LTP5, LTP6, LTP7 and LTP8 for Lanes 0, 1, 2 and 3, respectively.

If the measured skew does not exceed 500 ps, the test is passed; otherwise, the test is failed.

Connection Diagram

Refer to Figure 103 on page 227. The connection diagram is the same as for HFR7-21 Cable Eye Diagram. You will be required to reconnect during the test when prompted by a new connection diagram appearing in the app.

Result Description

HFR7-22 Inter-Pair Skew - 3 GBit/s

[Not Compliant]

----General----	
Offline	True
Software Version	2023
Calibration Data Version	Unknown
Compliant	False
Non-compliance reason(s)	Procedure offline; Software status unr Lane2+_FrlLinkRate_3Gbps_ThreeLane, FR Skew Calibration, FRL Cable Swing Cali Lane0-_FrlLinkRate_3Gbps_ThreeLane, FR Lane0+_FrlLinkRate_3Gbps_ThreeLane, FR Calibration Lane1-_FrlLinkRate_3Gbps_T
gCTS Revision	2.1h
MOI Revision	v1e
Skew Offset	4 TBit
User Name	Unknown User

```
----M8195A - HDMI Sig. Gen.----
Fill up blanking periods with Null packets     False
Keep the signals after test?                   False
Skip Pattern generation                        True
----Dso----
Use internal probe head termination voltage    True
```

Result	AVcc [V]	Lanes	Added Inter-Pair Skew offset [TBit]	Measured Skew with offset [mTBit]	Measured Skew with offset [ps]	Measured Skew [mTBit]	Measured Skew [ps]
pass	3.300	Lane0Lane1	4.000	3919.000	1306.333	-81.000	-27.000
pass	3.300	Lane1Lane2	4.000	4039.000	1346.333	39.000	13.000
pass	3.300	Lane0Lane2 (calculated)	4.000	3958.000	1319.333	-42.000	-14.000
pass	3.300	Lane0Lane1	-4.000	-4081.000	-1360.333	-81.000	-27.000
pass	3.300	Lane1Lane2	-4.000	-3961.000	-1320.333	39.000	13.000
pass	3.300	Lane0Lane2 (calculated)	-4.000	-4042.000	-1347.333	-42.000	-14.000

Figure 105 Example result for HFR7-22: Inter-Pair Skew

- Result: (Pass/Fail) The test is passed if the skew does not exceed the value given in the spec.
- AVcc [V]: Power supply voltage of the analog part of the cable under test.
- Lanes: The two lanes between which the skew was measured.
- Added Inter-Pair Skew offset [TBit]: Offset added between the two FRL data lanes.
- Measured Skew with offset [mTBit]: Skew measured including the offset, in mTBit.
- Measured Skew with offset [ps]: Skew measured including the offset, in picoseconds.
- Measured Skew [mTBit]: Measured inter-pair skew for the given lanes, in mTBit.
- Measured Skew [ps]: Measured inter-pair skew for the given lanes, in picoseconds.

HFR7-23 Mode Conversion

Availability

- HDMI 2.1 FRL Signal
- Category 3 cables
- Compliance Mode only
- Only for Active Cables
- Only at 10 GHz data rate

Purpose and Method

This procedure tests for compliance according to HDMI Generic CTS Version 2.1c, Section 7.5 “Active Cable Assembly Electrical Tests”, HFR7-23: “Mode Conversion”. It is used to confirm that the mode conversions of an FRL lane do not exceed the maximum specified in the CTS.

The pattern generator transmits the LPT3 pattern at 12 Gbps per lane. ScdXY and SdcXY are measured for all the data lanes.

If the maximum mode conversion (Scd21, Scd12, Sdc21, Sdc12) is below –16 dB at 6 GHz, the test is passed; otherwise, it is failed.

This calibration is available only if you check “Active Cable” in the Configure Product dialog, only in Compliance mode and only for 10 GBit/s.

Connection Diagram

Refer to Figure 103 on page 227. The connection diagram is the same as for HFR7-21 Cable Eye Diagram.

Result Description

HFR7-23 Mode Conversion

[Not Compliant]

----General----	
Offline	True
Software Version	2023
Calibration Data Version	Unknown
Compliant	False
Non-compliance reason(s)	Procedure offline; Software status unr FRL Cable Mode Conversion Swing Calibr Calibration Lane3-, Mode Conversion Ca Calibration Lane2+, FRL Cable Mode Con Conversion Swing Calibration Lane3-, M Mode Conversion Swing Calibration Lane FRL Cable Mode Conversion Swing Calibr
gCTS Revision	2.1h
MOI Revision	v1c
Cable Emulator	None
Enable Crosstalk	False
Vcm_Input_Lane_0_83ps_Skew	16 mV
Vcm_Input_Lane_1_83ps_Skew	15 mV
Vcm_Input_Lane_2_83ps_Skew	16 mV
Vcm_Input_Lane_3_83ps_Skew	15 mV
Vdm_Input_Lane_0_0ps_Skew	45 mV
Vdm_Input_Lane_1_0ps_Skew	35 mV
Vdm_Input_Lane_2_0ps_Skew	45 mV
Vdm_Input_Lane_3_0ps_Skew	35 mV
Is cable bidirectional	False
User Name	Unknown User
----M8195A - HDMI Sig. Gen.----	
Fill up blanking periods with Null packets	False
Keep the signals after test?	False
Skip Pattern generation	True
----Dso----	
Use internal probe head termination voltage	True

Result	AVcc [V]	Lane	VCM_Output [mV]	VDM_Output [mV]	VCM_BaseLine [mV]	VDM_BaseLine [mV]	Sdc21 [dB]	Scd21 [dB]
pass	3.135	FrlLane3	0.033	0.370	0.025	0.054	-38.178	-54.490
pass	3.135	FrlLane0	0.035	0.370	0.024	0.045	-38.739	-56.162
pass	3.135	FrlLane1	0.033	0.370	0.025	0.054	-38.178	-54.490
pass	3.135	FrlLane2	0.035	0.370	0.024	0.045	-38.739	-56.162

Figure 106 Example result for HFR7-23: Mode Conversion

- Result: (Pass/Fail) Pass means that the measured S-parameters are within the specs.
- AVcc: The AVcc voltage at the DC power.
- Lane: The tested lane at this step.
- VCM_Output [mV]: The Vcm_Output measured at 6 GHz.

- VDM_Output [mV]: The Vdm_Output measured at 6 GHz.
- VCM_BaseLine [mV]: The Vcm_Output measured at 6 GHz when the skew is set to 0 ps.
- VDM_BaseLine [mV]: The measured Vdm_Output at 6 GHz when the skew is set to 0 ps.
- Sdc21 [dB]: The Sdc21 calculated for each lane.
- Scd21 [dB]: The Scd21 calculated for each lane.

Cable Tests in Expert Mode

HF Cable Eye Mask Measurement

Availability

- Expert Mode only
- HDMI 2.1 TMDS Signal
- Category 1, Category 2 cables

Purpose and Method

This procedure allows you to generate a 6 Gb/s signal to test cables with. It is based on the ID 5-3 Cable Eye Mask Measurement test but runs at a higher data rate.

This test does not appear in any CTS and is only used to characterize cable DUTs at a higher data rate.

Connection Diagram

Refer to Figure 97 on page 219.

The oscilloscope must be connected according to the data lane being tested.

Result Description

HF Cbl. Eye at 594 MHz D0

[Not Compliant]

Test HF Cable Data Eye Jitter only on Clock

----General----	
Offline	True
Software Version	2023
Calibration Data Version	Unknown; '1.3.0
Compliant	False
Non-compliance reason(s)	Procedure offline; Software status unr Calibration Data1+, HF Swing Calibrati clock) Calibration 6G TP1 4096x2160p60 Swing Calibration Data2-; Required cal Data1+, HF Swing Calibration Data2+, H
Differential Swing	800 mV
Cable Category	Category 1 (Home)
Check worst case eye manually	False
Measure current on HPD +5V_Power	False
TMDS data to clock ratio 1:40	True
User Name	Unknown User
----M8195A - HDMI Sig. Gen.----	
Fill up blanking periods with Null packets	False
Keep the signals after test?	False
Skip Pattern generation	True
----Dso----	
Use internal probe head termination voltage	True

Result	Data Jitter Amplitude [TBit]	Data Jitter Frequency [MHz]	Mask Violations []
pass	0.190	0.5	0

Figure 107 Example result for HF Cable Eye Mask Measurement

- Result: (Pass/Fail) Pass indicates that the DUT passed this test step successfully.
- Data Jitter Amplitude [TBit]: Amplitude of the jitter applied to the data.
- Data Jitter Frequency [MHz]: Frequency of the jitter applied to the data.
- Mask Violations: Number of waveforms violating the eye mask.

Keysight N5991HP1A HDMI 2.1 Receiver Compliance Test Automation Software

User Guide

9 Appendix: HDMI Parameters

This Appendix contains lists and descriptions of parameters used in the Keysight N5991HP1A HDMI 2.1 Receiver Compliance Test Automation Software user interface.

KEYSIGHT TECHNOLOGIES

Overview

The parameters used in ValiFrame for HDMI are divided here into

- Sequencer Parameters (Table 8 on page 239)
- HDMI PHY Common Parameters (Table 9 on page 240)
- HDMI PHY Parameters for individual Procedures
  - HDMI PHY Parameters that appear in (practically) all individual procedures (Table 10 on page 241).
  - HDMI PHY Parameters for Individual Calibrations (Table 11 on page 242 (sink) and Table 12 on page 246 (cable)
  - HDMI PHY Parameters for Individual Tests (Table 13 on page 250 (sink) and Table 14 on page 259 (cable))

With the exception of Table 9 on page 240, in the tables the parameters are listed in alphabetical order.

NOTE If the value of a parameter appears in boldface type in the parameter grid of the GUI, this indicates that the value is not the default value.

NOTE If a parameter is read-only (gray) in the parameter grid, it can usually be set either in the Station Configurator or when configuring the DUT.

Sequencer Parameters

Table 8 HDMI PHY Sequencer Parameters

Parameter name	Description
Procedure Error Case Behavior	▪ "Proceed With Next Procedure"–If an error occurs in the test or calibration procedure, continue by running the next procedure in the sequence. ▪ "Abort Sequence"–Abort further running of the sequence.
Procedure Failed Case Behavior	▪ "Proceed With Next Procedure"–If the test or calibration procedure fails, continue by running the next procedure in the sequence. ▪ "Abort Sequence"–Abort further running of the sequence.
Repetitions	The number of times the group or procedure will be repeated. If the value is '0', it runs only once.

HDMI PHY Common Parameters

Table 9 HDMI PHY Common Parameters

Heading / Parameter name	Description
None	
Repetitions	The number of times the group will be repeated. If the value is '0', it runs only once.
User Name	The User Name entered in the Configure Product dialog.
Dso	
Use internal probe head termination voltage	If set to 'True', the internal termination voltage of the probe heads (e.g., N5444) is used.
M8195A – HDMI Sig. Gen.	
DVI Mode	If set to 'True', TMDS Generator generates DVI instead of HDMI data.
Fill up blanking periods with Null packets	Fills up all blanking periods with null packets to reduce unbalanced HDMI symbols to a minimum.
Keep the signals after test?	If set to 'True', the signal is retained after each test to allow additional items to be measured.
Skip Pattern generation	Only relevant for offline runs: If set to 'True', pattern generation will be skipped for offline runs. This reduces the time taken.
Offset position of first packet in line	This value shifts out the position of the first packet in a line relative to the HSync Active Start. Control sequences are added until this offset is reached.
SCDC Controller	
SCDC supports Character Error Detections	If set to 'True', the SCDC controller is used as the error detector.
Skip Link Training	The test pattern is directly applied to the Sink DUT; link training is bypassed.
Start delay between SCDC Controller and TMDS signal	Delay duration (in milliseconds) before configuring the SCDC controller. This value must be evaluated for each setup manually.

HDMI PHY Parameters for Individual Procedures

HDMI PHY Parameters Used in All Individual Procedures

Table 10 lists the parameters that are used in (practically) all procedures. They appear at the top of the parameter grid are listed here in alphabetical order.

Table 10 HDMI PHY Parameters for All Individual Procedures

Parameter	Description
Calibration Data Version	The version of the N5991 ValiFrame software that was used to obtain the data of the prerequisite calibrations, i.e., the calibration data required in order to perform the procedure (test or calibration).
Compliant	Read-only in the parameter grid. It indicates whether the procedure you are running is compliant with the HDMI PHY specification. ▪ True: You are working in Compliance Mode OR you are working in Expert Mode but all parameters that can be edited only in Expert Mode have their default values. ▪ False: You are working in Expert mode and a parameter that can be edited only in Expert Mode does not have its default value. The mode can be selected in the Configure DUT panel. False is also shown if you are working offline or if any of the prerequisite calibrations were not performed in compliant conditions. If the value is False, an additional property (Non-compliance reason(s)) is shown to indicate why the data is not compliant.
CTS Revision	The revision number of the Compliance Test Specification on which the test is based. (Only for HDMI 1.4 test procedures.)
gCTS Revision	The revision number of the Generic Compliance Test Specification on which the test is based. (Only for HDMI 2.1 TMDS and FRL test procedures.)
MOI Revision	The revision number of the Method of Implementation on which the test is based. (Only for HDMI 2.1 TMDS and FRL test procedures.)
Non-compliance reason(s)	Possible reasons include: the required calibrations were run offline, with unreleased software, with old firmware.
Offline	▪ If True, the test automation software is not connected to any instrument. This mode should be used for demonstrations and checks only. It is not valid for calibrations or measurements. ▪ If False, the software is connected to instruments and produces valid data. It is read-only in the parameter grid. It can be set in the Instrument Configuration step of the Station Configurator.
Software Version	The version of the N5991 ValiFrame software currently being used.

HDMI PHY Parameters for Individual Sink Calibrations

The parameters for individual calibrations listed here are in addition to the parameters that are used in (practically) all procedures, which are listed in Table 10 on page 241.

Table 11 HDMI PHY Parameters for Individual Sink Calibrations

Parameter	Description, Which Procedures
Applied Voltage Step	The amount by which the differential voltage is decreased at each step. ▪ Eye Height Calibration
Cable Emulator	Select the cable type to be simulated in the M8195A for TP2 calibrations. An S-parameter file (.s2p or .s4p) can be used by selecting the "Custom" option. Choose the file in the Custom ISI Emulator field. Note: A separate license is required to enable this custom S-parameter option. ▪ Clock Jitter Calibration TP2 ▪ HF Clock Jitter Calibration ▪ HF Data Jitter Calibration ▪ Eye Width Calibration ▪ Eye Height Calibration
Color Depth	The color depth used for this test. Values: 24, 30, 36, 48 bit ▪ Swing Calibration ▪ Clock Jitter Calibration ▪ Data Jitter (on clock/data) Calibration ▪ HF Swing Calibration ▪ HF Clock Jitter Calibration ▪ HF Data Jitter Calibration
Color Space	The color space used for this test. ▪ Swing Calibration ▪ Clock Jitter Calibration ▪ Data Jitter (on clock/data) Calibration ▪ HF Swing Calibration ▪ HF Clock Jitter Calibration ▪ HF Data Jitter Calibration
Differential Swing	The differential voltage level of the signal. ▪ Fall/Rise Time Calibration ▪ Clock Jitter Calibration ▪ Data Jitter (on clock/data) Calibration ▪ HF Clock Jitter Calibration ▪ HF Data Jitter Calibration ▪ Random Jitter Calibration ▪ Eye Width Calibration
DSO Channel used for Calibration	DSO channel selected as Input. ▪ Swing Calibration ▪ HF Swing Calibration ▪ FRL Swing Calibration
DSO Channel used for Termination	DSO channel selected as Termination ▪ Swing Calibration ▪ HF Swing Calibration ▪ FRL Swing Calibration

Parameter	Description, Which Procedures
Enable Crosstalk	Set to 'True' to enable crosstalk in the FRL signal generator ▪ Eye Width Calibration ▪ Eye Height Calibration
First Differential Voltage	First differential voltage amplitude that is calibrated. It depends on the data rate. ▪ Eye Height Calibration
Integration Time	The acquisition time for the captured signal in seconds. Decreasing this value may speed up the calibration but reduces accuracy. ▪ Fall/Rise Time Calibration
Jitter Step Size	The value by which the jitter amplitude is increased per step. ▪ Clock Jitter Calibration ▪ Data Jitter (on clock/data) Calibration ▪ HF Clock Jitter Calibration ▪ HF Data Jitter Calibration
Max Jitter	The maximum jitter amplitude. This is the stop value. ▪ Clock Jitter Calibration ▪ Data Jitter (on clock/data) Calibration ▪ HF Clock Jitter Calibration ▪ HF Data Jitter Calibration
Max Swing Value	The maximum amplitude that will be calibrated. ▪ Swing Calibration ▪ HF Swing Calibration ▪ FRL Swing Calibration
Max Transition	The maximum fall/rise time that will be calibrated. Default: 1 ns transition time of highest video mode in TBit. ▪ Fall/Rise Time Calibration
Measurement Cycles	The number of times that the eye is measured at each step. After that, all results are averaged. ▪ Eye Width Calibration ▪ Eye Height Calibration
Min Jitter	The minimum jitter amplitude. This is the start value. ▪ Clock Jitter Calibration ▪ Data Jitter (on clock/data) Calibration ▪ HF Clock Jitter Calibration ▪ HF Data Jitter Calibration
Min Swing Value	The minimum amplitude that will be calibrated. ▪ Swing Calibration ▪ HF Swing Calibration ▪ FRL Swing Calibration
Min Transition	The minimum fall/rise time that will be calibrated. ▪ Fall/Rise Time Calibration

Parameter	Description, Which Procedures
Perform full D9021HDMC mask test for each calibration step	If True, a full D9021HDMC mask test will be performed for each calibration step. ▪ Data Jitter (on clock/data) Calibration ▪ HF Data Jitter Calibration
Start PCB Loss Factor	First PCB loss factor value that is calibrated. It depends on the data rate. ▪ Eye Width Calibration
Step Size	The value by which the parameter (voltage, time) is increased/decreased per step during calibration. ▪ Fall/Rise Time Calibration ▪ Swing Calibration ▪ HF Swing Calibration ▪ FRL Swing Calibration
Step size of sample frequency	The amount by which the sample frequency is increased between steps. ▪ Skew Calibration
Stop Jitter (RMS)	The maximum random jitter value that is calibrated. ▪ Random Jitter Calibration
Target Height Lane0/Lane1/ Lane2	This determines the last calibration step. When the measured eye height is less than the target height, the calibration ends. ▪ Eye Height Calibration
Target Jitter Lane0/Lane1/Lane2	This determines the last calibration step. When the measured total jitter is higher than the target jitter, the calibration ends. For Eye Height Calibration: The amount of jitter added to the signal. It is applied by setting the required PCB Loss Factor according to the Eye Width calibration. ▪ Eye Width Calibration ▪ Eye Height Calibration
TMDS Clock	The calculated TMDS Clock used for this test. ▪ Fall/Rise Time Calibration ▪ Swing Calibration ▪ Clock Jitter Calibration ▪ Data Jitter (on clock/data) Calibration ▪ HF Swing Calibration ▪ HF Clock Jitter Calibration ▪ HF Data Jitter Calibration
TMDS Data to Clock Ratio 1:40	The ratio between the TMDS data and TMDS clock can be set either as 1:40 or as 1:10. Set to 'True' to configure the ratio as 1:40. ▪ HF Clock Jitter Calibration ▪ HF Data Jitter Calibration
Use Color Bar Pattern	Set to True to use a color bar pattern. Set to False to use a gray scale. ▪ Clock Jitter Calibration ▪ Data Jitter (on clock/data) Calibration ▪ HF Clock Jitter Calibration ▪ HF Data Jitter Calibration

Parameter	Description, Which Procedures
Use Scrambled Video Signal	Set to 'True' to generate a scrambled signal. ▪ HF Clock Jitter Calibration ▪ HF Data Jitter Calibration
Video Mode	The video mode used for the procedure, or, the FRL rate for this calibration. ▪ Swing Calibration ▪ Clock Jitter Calibration ▪ Data Jitter (on clock/data) Calibration ▪ HF Swing Calibration ▪ HF Clock Jitter Calibration ▪ HF Data Jitter Calibration ▪ FRL Swing Calibration ▪ Random Jitter Calibration ▪ Eye Width Calibration ▪ Eye Height Calibration

HDMI PHY Parameters for Individual Cable Calibrations

The parameters for individual calibrations listed here are in addition to the parameters that are used in (practically) all procedures, which are listed in Table 10 on page 241.

Table 12 HDMI PHY Parameters for Individual Cable Calibrations

Parameter	Description, Which Procedures
Applied Voltage Step	The amount by which the differential voltage is decreased at each step. ▪ Eye Height Calibration
Cable Emulator	Select the cable type to be simulated in the M8195A for TP2 calibrations. An S-parameter file (.s2p or .s4p) can be used by selecting the "Custom" option. Choose the file in the Custom ISI Emulator field. Note: A separate license is required to enable this custom S-parameter option. ▪ Eye Width Calibration ▪ Eye Height Calibration ▪ Mode Conversion Calibration
Color Depth	The color depth used for the procedure. ▪ Swing Calibration ▪ Data Jitter (on clock) Calibration ▪ HF Swing Calibration ▪ Data Jitter (on clock) Calibration 6G
Color Space	The color space used for the procedure. ▪ Swing Calibration ▪ Data Jitter (on clock) Calibration ▪ HF Swing Calibration ▪ Data Jitter (on clock) Calibration 6G
Differential Swing	The differential voltage level of the signal. ▪ Fall/Rise time Calibration ▪ Data Jitter (on clock) Calibration ▪ Data Jitter (on clock) Calibration 6G ▪ Random Jitter Calibration ▪ Eye Width Calibration
DSO Channel Used for Calibration	DSO channel selected as Input. ▪ Swing Calibration ▪ HF Swing Calibration ▪ FRL Cable Swing Calibration ▪ FRL Cable Mode Conversion Swing Calibration
DSO Channel Used for Termination	DSO channel selected as Termination. ▪ Swing Calibration ▪ HF Swing Calibration ▪ FRL Cable Swing Calibration ▪ FRL Cable Mode Conversion Swing Calibration

Parameter	Description, Which Procedures
Enable Crosstalk	If set to True, crosstalk is enabled. ▪ Eye Width Calibration ▪ Eye Height Calibration ▪ Mode Conversion Calibration
First Differential Voltage	First differential voltage amplitude that is calibrated. It depends on the data rate. ▪ Eye Height Calibration
Integration Time	The acquisition time for the captured signal in seconds. Decreasing this value may speed up the calibration but reduces accuracy. ▪ Fall/Rise time Calibration
Jitter Step Size	The step size that is used to increase the jitter amplitude. ▪ Data Jitter (on clock) Calibration ▪ Data Jitter (on clock) Calibration 6G
Max Jitter	The maximum jitter amplitude. This is the stop value. ▪ Data Jitter (on clock) Calibration ▪ Data Jitter (on clock) Calibration 6G
Max Swing Value	The maximum voltage swing amplitude that will be calibrated. ▪ Swing Calibration ▪ HF Swing Calibration ▪ FRL Cable Swing Calibration ▪ FRL Cable Mode Conversion Swing Calibration
Max Transition	The maximum Fall/Rise Time that will be calibrated. Default: 1 ns transition time of highest video mode in TBit. ▪ Fall/Rise time Calibration
Measurement Cycles	The number of times that the eye is measured at each step. After that, all results are averaged. ▪ Eye Width Calibration ▪ Eye Height Calibration
Min Jitter	The minimum jitter amplitude. This is the start value. ▪ Data Jitter (on clock) Calibration ▪ Data Jitter (on clock) Calibration 6G
Min Swing Value	The minimum voltage swing amplitude that will be calibrated. ▪ Swing Calibration ▪ HF Swing Calibration ▪ FRL Cable Swing Calibration ▪ FRL Cable Mode Conversion Swing Calibration
Min Transition	The minimum Fall/Rise Time that will be calibrated. ▪ Fall/Rise time Calibration

Parameter	Description, Which Procedures
Perform full D9021HDNC mask test for each calibration step	Set to True to perform a full D9021HDNC mask test for each calibration step. ▪ Data Jitter (on clock) Calibration ▪ Data Jitter (on clock) Calibration 6G
Start PCB Loss Factor	First PCB loss factor value that is calibrated. It depends on the data rate. ▪ Eye Width Calibration
Step Size	The value by which the parameter value is increased/decreased per step. ▪ Fall/Rise time Calibration ▪ Swing Calibration ▪ HF Swing Calibration ▪ FRL Cable Swing Calibration ▪ FRL Cable Mode Conversion Swing Calibration
Step Size of Sample Frequency	The value by which the sample frequency is increased/decreased per step during calibration. ▪ Skew Calibration
Stop Jitter (RMS)	The maximum random jitter value that is calibrated. ▪ Random Jitter Calibration
Target Height Lane2	This determines the last calibration step. When the measured eye height is less than the target height, the calibration ends. ▪ Eye Height Calibration
Target Jitter Lane2	This determines the last calibration step. When the measured total jitter is higher than the target jitter, the calibration ends. For Eye Height Calibration: The amount of jitter added to the signal. It is applied by setting the required PCB Loss Factor according to the Eye Width calibration. ▪ Eye Width Calibration ▪ Eye Height Calibration
TMDS Clock	The calculated TMDS Clock used for the procedure. ▪ Fall/Rise time Calibration ▪ Swing Calibration ▪ Data Jitter (on clock) Calibration ▪ HF Swing Calibration ▪ Data Jitter (on clock) Calibration 6G
TMDS data to clock ratio 1:40	The ratio between TDMS data and TDMS clock can be either 1:40 or 1:10. Selecting True sets the ratio to 1:40. ▪ Data Jitter (on clock) Calibration 6G
Use Color Bar Pattern	Set to True to use a color bar pattern. Set to False to use a gray scale. ▪ Data Jitter (on clock) Calibration ▪ Data Jitter (on clock) Calibration 6G

Parameter	Description, Which Procedures
Use scrambled video signal	Set to 'True' to generate a scrambled signal. ▪ Data Jitter (on clock) Calibration 6G
Use Swing Calibration	If True, calibrated swing levels will be used. ▪ Mode Conversion Calibration
Video Mode	The video mode used for the test. ▪ Swing Calibration ▪ Data Jitter (on clock) Calibration ▪ HF Swing Calibration ▪ Data Jitter (on clock) Calibration 6G ▪ FRL Cable Swing Calibration ▪ Random Jitter Calibration ▪ Eye Width Calibration ▪ Eye Height Calibration ▪ FRL Cable Mode Conversion Swing Calibration

HDMI PHY Parameters for Individual Sink Tests

The parameters for individual tests listed here are in addition to the parameters that are used in (practically) all procedures, which are listed in Table 10 on page 241.

NOTE

Sink tests for HDMI 1.4 with TMDS signal begin “ID X-Y”, where X and Y are numbers.

Sink tests for HDMI 2.1 with TMDS signal begin “ID HFX-Y”, where X and Y are numbers.

Sink tests for HDMI 2.1 with FRL signal begin “HFRX-Y”, where X and Y are numbers.

Sink tests available only in expert mode are denoted by “(Exp)” at the beginning of the name.

Table 13 HDMI PHY Parameters for Individual Sink Tests

Parameter	Description, Which Procedures
3D Mode	Set to ‘2D’ if a 3D mode is not used. Otherwise, set the 3D mode used for the test. ▪ (Exp) Generic Video Format Timing
Alternate Jitter Amplitude	Sets the amplitude of the second sinusoidal jitter component. ▪ (Exp) Sensitivity to Jitter (Data/Clock)
Alternate Jitter Frequency	Sets the frequency of the second sinusoidal jitter component. ▪ (Exp) Sensitivity to Jitter (Data/Clock)
Cable Emulator	Select the cable emulator type. An S-parameter file (.s2p or .s4p) can be used by selecting the “Custom” option. Choose the file in the Custom ISI Emulator field. Note: A separate license is required to enable this custom S-parameter option. ▪ ID 8-7: Jitter Tolerance ▪ ID HF2-2: Intra-Pair Skew ▪ ID HF2-3: Jitter Tolerance ▪ HFR2-2: Intra-Pair Skew ▪ HFR2-3: Inter-Pair Skew ▪ HFR2-4: Minimum Link Rate ▪ HFR2-5: Jitter Tolerance ▪ (Exp) Sensitivity to Jitter (Injection via Clock) ▪ (Exp) Sensitivity to Jitter (Worst Case Skew) ▪ (Exp) Sensitivity to Jitter (Data/Clock) ▪ (Exp) HF: Intra-Pair Skew ▪ (Exp FRL) FRL Error Pattern Check ▪ (Exp FRL) Jitter Characterization Test

Parameter	Description, Which Procedures
Characterization Mode	Set to 'True' to characterize the DUT. Set to 'False' to check for compliance. If set to 'True', set the desired values of min/max frequencies; otherwise, check specification to ensure that the values of the parameters 'Min Frequency' and 'Max Frequency' are set suitably. ▪ (Exp) Sensitivity to Jitter (Data/Clock)
Clock Jitter Margin	If this margin is set to a value not equal to 0, the test starts with a higher clock jitter than specified; the value is the specified clock jitter plus the margin value. ▪ ID 8-7: Jitter Tolerance ▪ ID HF2-3: Jitter Tolerance
Color Depth	The color depth used for this test. Values: 24, 30, 36, 48 bit ▪ ID 8-5: Differential Swing ▪ ID 8-6: Intra-Pair Skew ▪ ID 8-7: Jitter Tolerance ▪ ID HF2-1: Differential Swing ▪ ID HF2-2: Intra-Pair Skew ▪ ID HF2-51: Inter-Pair Skew ▪ ID HF2-3: Jitter Tolerance ▪ (Exp) ID 8-31: AVI InfoFrame supporting Extended Colorimetry, Content Type and ... ▪ (Exp) Differential Swing ▪ (Exp) Sink Inter-Pair Skew ▪ (Exp) Sensitivity to Jitter (Injection via Clock) ▪ (Exp) Sensitivity to Jitter (Worst Case Skew) ▪ (Exp) Sensitivity to Jitter (Data/Clock) ▪ (Exp) HF: Intra-Pair Skew ▪ (Exp) Generic Video Format Timing
Color Space	The color space used for this test. ▪ ID 8-5: Differential Swing ▪ ID 8-6: Intra-Pair Skew ▪ ID 8-7: Jitter Tolerance ▪ ID HF2-1: Differential Swing ▪ ID HF2-2: Intra-Pair Skew ▪ ID HF2-51: Inter-Pair Skew ▪ ID HF2-3: Jitter Tolerance ▪ (Exp) ID 8-31: AVI InfoFrame supporting Extended Colorimetry, Content Type and ... ▪ (Exp) Differential Swing ▪ (Exp) Sink Inter-Pair Skew ▪ (Exp) Sensitivity to Jitter (Injection via Clock) ▪ (Exp) Sensitivity to Jitter (Worst Case Skew) ▪ (Exp) Sensitivity to Jitter (Data/Clock) ▪ (Exp) HF: Intra-Pair Skew ▪ Generic Video Format Timing (Exp)
Data Jitter Margin	If this margin is set to a value not equal to 0, the test starts with a higher data jitter than specified; the value is the specified data jitter plus the margin value. ▪ ID 8-7: Jitter Tolerance ▪ ID HF2-3: Jitter Tolerance
Desired Jitter Accuracy	This is the minimum step size required for the search performed by the software, which uses a binary search algorithm, for the maximum passed value of jitter. ▪ (Exp) Sensitivity to Jitter (Worst Case Skew) ▪ (Exp) Sensitivity to Jitter (Data/Clock)
Desired Skew Accuracy	This is the minimum step size required for the search performed by the software, which uses a binary search algorithm, for the maximum passed value of skew. ▪ ID 8-7: Jitter Tolerance

Parameter	Description, Which Procedures
Differential Swing	Differential voltage level. ▪ ID 8-7: Jitter Tolerance ▪ ID HF2-3: Jitter Tolerance ▪ (Exp) Sensitivity to Jitter (Worst Case Skew) ▪ (Exp) Sensitivity to Jitter (Data/Clock)
Differential Swing Step Size	The value by which the differential swing is decreased per step. ▪ ID 8-5: Differential Swing ▪ ID HF2-1: Differential Swing ▪ HFR2-1: Differential Swing Tolerance ▪ (Exp) Differential Swing ▪ (Exp FRL) Differential Swing Tolerance
Enable Crosstalk	Set to 'True' to enable crosstalk. ▪ HFR2-2: Intra-Pair Skew ▪ HFR2-3: Inter-Pair Skew ▪ HFR2-4: Minimum Link Rate ▪ HFR2-5: Jitter Tolerance ▪ (Exp FRL) FRL Error Pattern Check ▪ (Exp FRL) Jitter Characterization Test
Eye Height Lane0/Lane1/Lane2/Lane3	The compliance eye height according to the HDMI specifications for each lane. ▪ HFR2-5 Jitter Tolerance
Frequency Steps	Defines how many frequencies are tested between the values for the parameters 'Min. Frequency' and 'Max. Frequency'. ▪ (Exp) Sensitivity to Jitter (Data/Clock)
Initial Skew Step Size	The amount by which the skew is decreased/increased between steps. ▪ (Exp) Sink Inter-Pair Skew
Initial Margin Step Size	Step size used in the margin value search. ▪ ID 8-7: Jitter Tolerance ▪ ID HF2-3: Jitter Tolerance
Jitter Frequency	Frequency of the jitter applied in the test. ▪ (Exp) Sensitivity to Jitter (Worst Case Skew)
Jitter Phase (Data to Clock)	Applied jitter phase. ▪ (Exp) Sensitivity to Jitter (Data/Clock)
Linear Frequency Steps	Set to 'True' if frequency steps are classified as linear. ▪ (Exp) Sensitivity to Jitter (Worst Case Skew) ▪ (Exp) Sensitivity to Jitter (Data/Clock)
Link Rate Deviation	The applied deviation of the link rate from the nominal value. ▪ HFR2-4: Minimum Link Rate

Parameter	Description, Which Procedures
Margin Accuracy	The minimum step size for which it is required to perform the search for the margin using a binary search algorithm. ▪ ID 8-7: Jitter Tolerance ▪ ID HF2-3: Jitter Tolerance
Margin Search	Values: None, Clock Jitter, Data Jitter, Both If this parameter is set to the default value 'None', the test runs with jitter amplitudes as specified plus the values in Data Jitter Margin and Clock Jitter Margin. If the test fails, it is repeated at the specified values. For the other values, if a test fails, the software uses a binary search algorithm to start searching for the margin, and this search continues until it finds the value where the DUT stops failing. ▪ ID 8-7: Jitter Tolerance ▪ ID HF2-3: Jitter Tolerance
Max Frequency	The maximum jitter frequency that is applied. ▪ (Exp) Sensitivity to Jitter (Data/Clock)
Max Jitter	The maximum jitter amplitude. This is the stop value. ▪ (Exp) Sensitivity to Jitter (Worst Case Skew) ▪ (Exp) Sensitivity to Jitter (Data/Clock)
Max Skew / Maximum Skew	The maximum value of skew applied to the DUT. ▪ ID 8-6: Intra-Pair Skew ▪ (Exp) Sink Inter-Pair Skew ▪ (Exp) Sensitivity to Jitter (Worst Case Skew) ▪ (Exp) HF: Intra-Pair Skew
Max Spec. Inter-Pair Skew	The maximum inter-pair skew value according to the specification. ▪ HFR2-3: Inter-Pair Skew
Max Voltage Offset	The upper limit of the voltage offset range used for the test. ▪ ID HF2-3: Jitter Tolerance
Minimum Differential Swing	The minimum voltage swing that will be applied. ▪ ID 8-5: Differential Swing ▪ ID HF2-1: Differential Swing ▪ HFR2-1: Differential Swing Tolerance ▪ (Exp) Differential Swing ▪ (Exp FRL) Differential Swing Tolerance
Min Frequency	The minimum jitter frequency that is applied. ▪ (Exp) Sensitivity to Jitter (Data/Clock)
Min Jitter	The minimum jitter amplitude. This is the start value. ▪ (Exp) Sensitivity to Jitter (Worst Case Skew) ▪ (Exp) Sensitivity to Jitter (Data/Clock)
Minimum Passing Skew	Minimum skew value to determine if the test is passed or failed. (Read only) ▪ ID 8-6: Intra-Pair ▪ (Exp) HF: Intra-Pair Skew

Parameter	Description, Which Procedures
Min Skew / Minimum Skew	The minimum applied value of skew. ▪ ID 8-6: Intra-Pair ▪ (Exp) Sensitivity to Jitter (Worst Case Skew) ▪ (Exp) HF: Intra-Pair Skew
Min Voltage Offset	The lower limit of the voltage offset range used for the test. ▪ ID HF2-3 Jitter Tolerance
Negative Framerate Deviation	The negative deviation from the nominal frame rate. ▪ (Exp) Generic Video Format Timing
Number of Steps	The number of times the BER test must be performed for the error-free and error-inducing patterns. ▪ (Exp FRL) FRL Error Pattern Check
PCB loss dB	The PCB loss added for the test. ▪ (Exp FRL) Jitter Characterization Test
Positive Framerate Deviation	The positive deviation from the nominal frame rate. ▪ (Exp) Generic Video Format Timing
RJ pk-pk	The peak-to-peak amplitude of the random jitter for the test. ▪ (Exp FRL) Jitter Characterization Test
SJ Frequency	The frequency of the sinusoidal jitter for the test. ▪ HFR2-5 Jitter Tolerance ▪ (Exp FRL) Jitter Characterization Test
SJ pk-pk	The peak-to-peak amplitude of the sinusoidal jitter for the test. ▪ HFR2-5 Jitter Tolerance
Skew / Skew in ps	Value of skew in TBit and ps, respectively. ▪ ID HF2-2: Intra-Pair Skew ▪ ID HF2-51: Inter-Pair Skew ▪ HFR2-2: Intra-Pair Skew
Skew Step Size	The amount by which the skew is decreased per step. ▪ ID 8-6: Intra-Pair Skew ▪ (Exp) Sensitivity to Jitter (Worst Case Skew) ▪ (Exp) HF: Intra-Pair Skew
Skew Step Time	Time waited between applying the signal and showing the pass/fail dialog. ▪ (Exp) Sink Inter-Pair Skew

Parameter	Description, Which Procedures
Skewed Channel [Data0, Data1, Data2 or Clock]	The skew of the TMDS pair against other TMDS pairs. ▪ (Exp) Sink Inter-Pair Skew
Start Differential Swing	The initial value of the differential voltage level. ▪ ID 8-5: Differential Swing ▪ ID HF2-1: Differential Swing ▪ HFR2-1: Differential Swing Tolerance ▪ (Exp) Differential Swing ▪ Differential Swing Data Channel (Exp) ▪ Differential Swing All Channels sep. (Exp) ▪ (Exp FRL) Differential Swing Tolerance
Start SJ pk-pk	Initial value of the sinusoidal jitter peak-to-peak amplitude. ▪ (Exp FRL) Jitter Characterization Test
Starting Pattern on Lane0/Lane1/ Lane2/Lane3	The pattern sent on each lane for the Link Training. ▪ HFR2-1: Differential Swing Tolerance ▪ HFR2-2: Intra-Pair Skew ▪ HFR2-3: Inter-Pair Skew ▪ HFR2-4: Minimum Link Rate ▪ HFR2-5: Jitter Tolerance ▪ (Exp FRL) Differential Swing Tolerance ▪ (Exp FRL) FRL Error Pattern Check ▪ (Exp FRL) Jitter Characterization Test
Target Jitter Lane0/Lane1/Lane2/ Lane3	The jitter amplitude required on the signal to meet the compliance eye width for each lane. ▪ HFR2-5: Jitter Tolerance
Test Channel	Defines which lanes are tested. Values: Data0, Data1, Data2, Clock or All. ▪ Differential Swing Data Channel (Exp)
Test Image	Image used for the test. Values: Default, ColorBar or AspectRatioCube. ▪ ID HF2-25: Sink Video Timing – 21:9 (64:27)
TMDS Clock	The calculated TMDS Clock used for the test. (Read only) ▪ ID 8-5: Differential Swing ▪ ID 8-6: Intra-Pair Skew ▪ ID 8-7: Jitter Tolerance ▪ ID HF2-1: Differential Swing ▪ ID HF2-2: Intra-Pair Skew ▪ ID HF2-51: Inter-Pair Skew ▪ ID HF2-3: Jitter Tolerance ▪ (Exp) ID 8-19: Pixel Encoding Requirements ▪ (Exp) ID 8-24: Interoperability with DVI ▪ (Exp) Differential Swing ▪ (Exp) Sink Inter-Pair Skew ▪ (Exp) Sensitivity to Jitter (Injection via Clock) ▪ (Exp) Sensitivity to Jitter (Worst Case Skew) ▪ (Exp) Sensitivity to Jitter (Data/Clock) ▪ (Exp) HF: Intra-Pair Skew ▪ (Exp) Generic Video Format Timing

Parameter	Description, Which Procedures
TMDS data to clock ratio 1:40	The ratio between the TMDS data and TMDS clock can be set as either 1:40 or 1:10. Set to 'True' to configure the ratio as 1:40. This setting enables signals compliant with HDMI 1.4 or HDMI 2.1 to be sent. ▪ ID 8-5: Differential Swing ▪ ID 8-6: Intra-Pair Skew ▪ ID HF2-1: Differential Swing ▪ ID HF2-2: Intra-Pair Skew ▪ ID HF2-51: Inter-Pair Skew ▪ ID HF2-3: Jitter Tolerance ▪ ID HF2-6: Video Timing 2160p 24 bit ▪ ID HF2-7: Video Timing 2160p Deep Color ▪ ID HF2-8: Video Timing 2160p 3D ▪ ID HF2-36: Video Timing non 2160p 24bit ▪ ID HF2-37: Video Timing non 2160p Deep Color ▪ ID HF2-38: Video Timing non 2160p 3D ▪ (Exp) Sink Inter-Pair Skew ▪ (Exp) Sensitivity to Jitter (Injection via Clock) ▪ (Exp) Sensitivity to Jitter (Worst Case Skew) ▪ (Exp) Sensitivity to Jitter (Data/Clock) ▪ (Exp) HF: Intra-Pair Skew ▪ (Exp) Generic Video Format Timing
Transition Time Converter	Sets a filter with the selected transition time. ▪ (Exp) Sensitivity to Jitter (Worst Case Skew) ▪ (Exp) Sensitivity to Jitter (Data/Clock)
Use Color Bar Pattern	Set to 'True' to use a color bar pattern. Set to 'False' to use a gray scale. ▪ ID 8-5: Differential Swing ▪ ID 8-6: Intra-Pair Skew ▪ ID 8-7: Jitter Tolerance ▪ ID HF2-1: Differential Swing ▪ ID HF2-2: Intra-Pair Skew ▪ ID HF2-51: Inter-Pair Skew ▪ ID HF2-3: Jitter Tolerance ▪ (Exp) Differential Swing ▪ (Exp) Sink Inter-Pair Skew ▪ (Exp) Sensitivity to Jitter (Injection via Clock) ▪ (Exp) Sensitivity to Jitter (Worst Case Skew) ▪ (Exp) Sensitivity to Jitter (Data/Clock) ▪ (Exp) HF: Intra-Pair Skew ▪ (Exp) Generic Video Format Timing
Use Scrambled Video Signal	Set to 'True' to generate a scrambled signal. ▪ ID 8-5: Differential Swing ▪ ID 8-6: Intra-Pair Skew ▪ ID HF2-1: Differential Swing ▪ ID HF2-2: Intra-Pair Skew ▪ ID HF2-51: Inter-Pair Skew ▪ ID HF2-3: Jitter Tolerance ▪ (Exp) Sink Inter-Pair Skew ▪ (Exp) Sensitivity to Jitter (Injection via Clock) ▪ (Exp) Sensitivity to Jitter (Worst Case Skew) ▪ (Exp) Sensitivity to Jitter (Data/Clock) ▪ (Exp) HF: Intra-Pair Skew ▪ (Exp) Generic Video Format Timing
Use separated YCbCr 4:2:0 test images	Instead of using one image with a color bar in the upper half and black/white bars in the lower half, you can use two separate images. ▪ ID HF2-23: Pixel Decoding YCbCr 4:2:0 ▪ ID HF2-24: Pixel Decoding YCbCr 4:2:0 Deep Color
Use Slider Dialog	In Expert mode, you may use a slider to set differential swing voltage levels (see Figure 50 on page 114). If set to 'True', the slider dialog is displayed and if set to 'False', only such voltage levels are tested that are required by the HDMI CTS. ▪ ID 8-5: Differential Swing ▪ (Exp) Differential Swing

Parameter	Description, Which Procedures
Use Swing Calibration	Set to 'True' to use calibrated swing voltage levels for this procedure. ▪ ID 8-6: Intra-Pair Skew ▪ ID 8-7: Jitter Tolerance ▪ ID HF2-2: Intra-Pair Skew ▪ ID HF2-51: Inter-Pair Skew ▪ ID HF2-6: Video Timing 2160p 24bit ▪ ID HF2-7: Video Timing 2160p Deep Color ▪ ID HF2-8: Video Timing 2160p 3D ▪ ID HF2-23: Pixel Decoding YCbCr 4:2:0 ▪ ID HF2-24: Pixel Decoding YCbCr 4:2:0 Deep Color ▪ ID HF2-25: Sink Video Timing – 21:9 (64:27) ▪ ID HF2-36: Video Timing non 2160p 24bit ▪ ID HF2-37: Video Timing non 2160p Deep Color ▪ ID HF2-38: Video Timing non 2160p 3D ▪ HFR2-3: Inter-Pair Skew ▪ HFR2-5: Jitter Tolerance ▪ (Exp) ID 8-15: Character Synchronization Test ▪ (Exp) ID 8-16: Acceptance of All Valid Packet Types ▪ (Exp) ID 8-19: Pixel Encoding Requirements ▪ (Exp) ID 8-20: Video Format Timing ▪ (Exp) ID 8-21: Audio Clock Regeneration ▪ (Exp) ID 8-22: Audio Jitter Test ▪ (Exp) ID 8-23: Audio Formats ▪ (Exp) ID 8-24: Interoperability with DVI ▪ (Exp) ID 8-25: Deep Color ▪ (Exp) ID 8-29: Video Format Timing ▪ (Exp) ID 8-30: 4k x 2k Video Format Timing ▪ (Exp) ID 8-31: AVI InfoFrame supporting Extended Colorimetry, Content Type and ... ▪ (Exp) Sink Inter-Pair Skew ▪ (Exp) Sensitivity to Jitter (Injection via Clock) ▪ (Exp) Sensitivity to Jitter (Worst Case Skew) ▪ (Exp) Sensitivity to Jitter (Data/Clock) ▪ (Exp) HF: Intra-Pair Skew ▪ (Exp) Generic Video Format Timing ▪ (Exp FRL) Jitter Characterization Test
Video Mode	The video mode used for the test. ▪ ID 8-5: Differential Swing ▪ ID 8-6: Intra-Pair Skew ▪ ID 8-7: Jitter Tolerance ▪ ID HF2-1: Differential Swing ▪ ID HF2-2: Intra-Pair Skew ▪ ID HF2-51: Inter-Pair Skew ▪ ID HF2-3: Jitter Tolerance ▪ HFR2-1: Differential Swing Tolerance ▪ HFR2-2: Intra-Pair Skew ▪ HFR2-3: Inter-Pair Skew ▪ HFR2-4: Minimum Link Rate ▪ HFR2-5: Jitter Tolerance ▪ (Exp) ID 8-19: Pixel Encoding Requirements ▪ (Exp) ID 8-24: Interoperability with DVI ▪ (Exp) ID 8-31: AVI InfoFrame supporting Extended Colorimetry, Content Type and ... ▪ (Exp) Differential Swing ▪ (Exp) Sink Inter-Pair Skew ▪ (Exp) Sensitivity to Jitter (Injection via Clock) ▪ (Exp) Sensitivity to Jitter (Worst Case Skew) ▪ (Exp) Sensitivity to Jitter (Data/Clock) ▪ (Exp) HF: Intra-Pair Skew ▪ (Exp) Generic Video Format Timing ▪ (Exp FRL) Differential Swing Tolerance ▪ (Exp FRL) FRL Error Pattern Check ▪ (Exp FRL) Jitter Characterization Test
Voltage Offset	The voltage offset used for the test. ▪ ID 8-5: Differential Swing ▪ ID HF2-1: Differential Swing ▪ HFR2-1: Differential Swing Tolerance ▪ (Exp) Differential Swing ▪ (Exp FRL) Differential Swing Tolerance
Voltage Offset, Vicm1/Vicm2	The voltage offsets for input common mode 1 and input common mode 2 in the test. ▪ ID HF2-2: Intra-Pair Skew ▪ ID HF2-51: Inter-Pair Skew

Parameter	Description, Which Procedures
Voltage Offset Factor / Voltage Swing Factor	The HDMI levels are defined relative to the high level, which is nominally at $V_{NominalOffset}$ = 3.3 V. The instrument defines levels that are relative to the center of the signal. To calculate the instrument offset, use the formula $V_{OffsetInstrument} = V_{OffsetFactor} * V_{OffsetHDMI} - V_{SwingFactor} * (V_{diff}/2) - V_{NominalOffset}$ These factors allow another definition to be set for the offset in HDMI. It is imperative that the AC-coupled source is enabled to set the factors $V_{OffsetFactor}$ = 1 and $V_{SwingFactor}$ = 0. ▪ ID 8-5: Differential Swing ▪ ID HF2-1: Differential Swing ▪ ID HF2-2: Intra-Pair Skew ▪ ID HF2-51: Inter-Pair Skew ▪ ID HF2-3: Jitter Tolerance ▪ HFR2-1: Differential Swing Tolerance ▪ (Exp) Differential Swing ▪ (Exp FRL) Differential Swing Tolerance
With Jitter	Set to 'False' to disable the jitter in the placement of the audio jitter packets. This can be used to verify proper operation of the DUT under normal conditions. ▪ (Exp) ID 8-22: Audio Jitter Test

HDMI PHY Parameters for Individual Cable Tests

The parameters for individual tests listed here are in addition to the parameters that are used in (practically) all procedures, which are listed in Table 10 on page 241.

Table 14 HDMI PHY Parameters for Individual Cable Tests

Parameters	Description, Which Procedures
Abort on Fail	Set to True if the procedure should abort if the test fails. ▪ HFR7-1 DC Power Test
Additional Guard Band Pattern	This field allows you to enter additional Guard Band patterns to search for, besides the default pattern. You can only enter the digits 0 and 1 here. The pattern must be ten bits long, six of which must consist of alternating 1s and 0s. The application uses the default pattern only when None is selected. If you have more than one pattern to enter, use a comma (,) to separate them (e.g., 0101010100, 1010101011). ▪ ID 5-5: Cable Inter-Pair Skew Measurement
Additional Sync Pattern	This field allows you to enter additional patterns to search for, besides the default pattern. You can only enter the digits 0 and 1 here. The pattern must be ten bits long, six of which must consist of alternating 1s and 0s. The application uses the default pattern only when None is selected. If you have more than one pattern to enter, use a comma (,) to separate them (example: 0101010100, 1010101011). ▪ ID 5-5: Cable Inter-Pair Skew Measurement
Cable Category	Select Category 1 (Home), Category 2 (Home), Category 3 (FRL) or User Defined. ▪ ID 5-3: Cable Eye Mask Measurement ▪ ID 5-5: Cable Inter-Pair Skew Measurement ▪ (Exp) HF Cable Eye Mask Measurement
Cable Emulator	The cable type to be simulated in the M8195A. An S-parameter file (.s2p or .s4p) can be used by selecting the “Custom” option. Choose the file in the Custom ISI Emulator field. Note: A separate license is required to enable this custom S-parameter option. ▪ HFR7-1 DC Power Test ▪ HFR7-21 Cable Eye Diagram ▪ HFR7-23 Mode Conversion
Check worst case eye manually	If set to ‘True’, you must manually check for the worst eye. ▪ ID 5-3: Cable Eye Mask Measurement ▪ (Exp) HF Cable Eye Mask Measurement
Color Depth	The color depth used for the test. Select in the Configure Product dialog. Values: 24, 30, 36, 48 bit. ▪ ID 5-3: Cable Eye Mask Measurement ▪ ID 5-5: Cable Inter-Pair Skew Measurement
Color Space	The color space used for the test. Select in the Configure Product dialog. ▪ ID 5-3: Cable Eye Mask Measurement ▪ ID 5-5: Cable Inter-Pair Skew Measurement

Parameters	Description, Which Procedures
Differential Swing	The applied value of differential swing voltage level. ▪ ID 5-3: Cable Eye Mask Measurement ▪ ID 5-5: Cable Inter-Pair Skew Measurement ▪ (Exp) HF Cable Eye Mask Measurement
Enable Crosstalk	Set to True to enable crosstalk. ▪ HFR7-1 DC Power Test ▪ HFR7-23 Mode Conversion
FRL Turn On Interpolation	OFF, INT2 or INT4 correspond to the level of interpolation used on the signal. ▪ HFR7-21 Cable Eye Diagram
Hysteresis	This parameter corresponds to the 'Cable Measurement Hysteresis' parameter in the 'Configure' tab of the oscilloscope's HDMI application. ▪ ID 5-5: Cable Inter-Pair Skew Measurement
Inter-Pair Skew Trigger Length	Select 10 bits or 20 bits as the length of the trigger pattern for the Inter-Pair Skew Test. ▪ ID 5-5: Cable Inter-Pair Skew Measurement
Is cable bidirectional	Set to True for a bidirectional cable. Then the measurement will be done in both directions. ▪ HFR7-23 Mode Conversion
Mask Movement Type	The manner in which the oscilloscope moves the mask. Options are 'Find pass', 'Fixed', 'Find margin' and 'Manual'. ▪ ID 5-3: Cable Eye Mask Measurement
Maximum Tries	Specifies the maximum number of tries before timeout. This setting needs to be increased when testing at a lower pixel rate. ▪ ID 5-5: Cable Inter-Pair Skew Measurement
Measure Current on HPD +5V_Power	If set to 'True', the HPD Power's current is measured. ▪ ID 5-3: Cable Eye Mask Measurement ▪ (Exp) HF Cable Eye Mask Measurement
Measurement Threshold	This parameter corresponds to the Cable Measurement Threshold parameter available in the 'Configure' tab of the oscilloscope's HDMI application. ▪ ID 5-5: Cable Inter-Pair Skew Measurement
Pext required	Set to True if the cable requires an additional power supply (USB connection, external power supply, etc). ▪ HFR7-1 DC Power Test
Skew Offset	Value of applied skew offset. ▪ HFR7-22 Inter-Pair Skew

Parameters	Description, Which Procedures
Start CTLE (dB)	Starting value for CTLE in dB. ▪ HFR7-21 Cable Eye Diagram
TMDS Clock	The calculated TMDS Clock used for the test. ▪ ID 5-3: Cable Eye Mask Measurement ▪ ID 5-5: Cable Inter-Pair Skew Measurement
TMDS data to clock ratio 1:40	The ratio between the TMDS data and TMDS clock can be set as either 1:40 or 1:10. Set to 'True' to configure the ratio as 1:40. This setting enables signals compliant with HDMI 1.4 or HDMI 2.1 to be sent. ▪ (Exp) HF Cable Eye Mask Measurement
Use Color Bar Pattern	Set to 'True' to use a color bar pattern. Set to 'False' to use a gray scale. ▪ ID 5-3: Cable Eye Mask Measurement ▪ ID 5-5: Cable Inter-Pair Skew Measurement
Use Swing calibration	Set to 'True' to use calibrated swing levels. ▪ ID 5-3: Cable Eye Mask Measurement ▪ ID 5-5: Cable Inter-Pair Skew Measurement ▪ (Exp) HF Cable Eye Mask Measurement ▪ HFR7-1 DC Power Test ▪ HFR7-21 Cable Eye Diagram ▪ HFR7-22 Inter-Pair Skew ▪ HFR7-23 Mode Conversion
V_drop TP1, V_drop TP2	These are the V_{drop} values that are calculated at the beginning of the test procedure by measuring the voltage at TP1 and TP2. ▪ HFR7-1 DC Power Test
Vcm_Input_Lane_X_83ps_Skew (X = 0, 1, 2, 3)	The Vcm_Input measured in the Mode Conversion Calibration for lane X. ▪ HFR7-23 Mode Conversion
Vdm_Input_Lane_X_0ps_Skew (X = 0, 1, 2, 3)	The Vdm_Input measured in the Mode Conversion Calibration for lane X. ▪ HFR7-23 Mode Conversion
Video Mode	The video mode used for the test. ▪ ID 5-3: Cable Eye Mask Measurement ▪ ID 5-5: Cable Inter-Pair Skew Measurement

10 Appendix: Acronyms and Abbreviations

This Appendix contains a list of acronyms and abbreviations used in the Keysight N5991 HDMI Test Automation Software Platform User Guide.

List of Acronyms

Acronym	Definition
ACR	Automatic Content Recognition
AVI	Audio Video Interleave
AWG	Arbitrary Waveform Generator
BER	Bit Error Ratio
CDF	Capabilities Declaration Form
CE	Cable Emulator
CEA	Consumer Electronics Association
CED	Character Error Detection
CTLE	Continuous-Time Linear Equalizer
CTS	Compliance Test Specification
DJ	Deterministic Jitter
DSO	Digital Storage Oscilloscope
DUT	Device Under Test
DVI	Digital Visual Interface
EDID	Extended Display Identification Data
FRL	Fixed Rate Link
GPIB	General Purpose Interface Bus
HDMI	High-Definition Multimedia Interface
HF	High Frequency
HPD	Hot Plug Detect
HTML	HyperText Markup Language
ICM	Input Common Mode
IO	Input–Output
ISI	Inter-Symbol Interference
JAE	Japan Aviation Electronics Industry
LAN	Local Area Network

Acronym	Definition
L-PCM	Linear Pulse Code Modulation
Mcsc	Mega Characters per Second per Channel
MOI	Method of Implementation
PC	Personal Computer
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
pk-pk	Peak to Peak
PRBS	PseudoRandom Binary Sequence
RJ	Random Jitter
RMS	Root Mean Squared
SCDC	Status and Control Data Channel
SCM	Short Cable Model
SJ	Sinusoidal Jitter
TMDS	Transition-Minimized Differential Signaling
TP	Test Point
TPA	Test Point Adapter
TTC	Transition Time Converter
UI	Unit Interval
USB	Universal Serial Bus
VIC	Video Identification Code
Vicm	Common Mode Input Voltage
VISA	Virtual Instrument System Architecture
WCM	Worst Cable Model
YCbCr	A color space

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