Agilent 871xE series to ENA 6 series Code Conversion Tips

Hints and examples for converting from 871xE series program codes to ENA 6 series codes

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1. Channel and trace setting

The ENA 6 series has 4 channels and 4 traces in each channel, compared to 2 channels and 1 trace in 871X series. So it is recommended that existing 871X series setting codes be changed as follows to maximize usability in ENA 6 series. Markers and formats couple display setting is allowed in the same channel. To convert channel and trace setting, following 3 types are major ones.

a) When using only “Meas 1” in 871X

Set ENA 6 series’s channel and trace mode as 1 channel and 1 trace.

Sample code (717 is unit’s GPIB address)

```
10 OUTPUT 717;":DISP:SPL D1"              ! Set channel layout in which the window for channel 1 only is displayed on the entire display. (Default setting)
20 OUTPUT 717;":CALC1:PAR:COUN 1"         ! Set trace number as 1. (Default setting)
30 OUTPUT 717;":DISP:WIND1:SPL D1"        ! Set trace layout in which one graph is displayed in the entire window. (Default setting)
```

b) When using “Meas 1” and “Meas 2” with alternative sweep “OFF” in 871X

Set ENA 6 series’s channel and trace mode as 1 channel and 2 traces.

Sample code

```
10 OUTPUT 717;":DISP:SPL D1"              ! Set channel layout as 1 screen. . (Default setting)
20 OUTPUT 717;":CALC1:PAR:COUN 2"         ! Set trace number as 2
30 OUTPUT 717;":DISP:WIND1:SPL D1_2"      ! Set trace layout in which 2 graphs in total are displayed in the upper part and lower part of the window.
```

c) When using “Meas 1” and “Meas 2” with alternative sweep “ON” in 871X

Set ENA 6 series’s channel and trace mode as 2 channels and 1 trace.

Sample code

```
10 OUTPUT 717;":DISP:SPL D1_2"          ! Set channel layout in which the window for channel 1 is displayed in the upper part and the window for channel 2 in the lower part.
20 OUTPUT 717;":CALC1:PAR:COUN 1"       ! Set channel 1's trace number as 1.  (Default setting)
30 OUTPUT 717;":CALC2:PAR:COUN 1"       ! Set channel 2's trace number as 1. ((Default setting)
40 OUTPUT 717;":DISP:WIND1:SPL D1"  ! Set trace layout in which one graph is displayed in the entire window for channel 1. (Default setting)
50 OUTPUT 717;":DISP:WIND2:SPL D1"  ! Set trace layout in which one graph is displayed in the entire window for channel 2. (Default setting)
```

2. Trigger setting

Basically, 871XE series and ENA 6 series have similar trigger system concept. But there are a few differences between them.

To trigger once and detect sweep end, 871XE series uses “:INIT” and “*WAI”.

In ENA 6 series, “:TRIG:SING” and “*OPC?” need to be used to detect sweep end.

Followings are some sample codes for ENA 6 series

a) Trigger continuous for only channel 1

```
10 OUTPUT 717;":ABORt"          !Set all channel's trigger state to "Hold"
20 OUTPUT 717;":TRIG:SOUR INT"          !Set trigger source as internal. (Default)
30 OUTPUT 717;":INIT1:CONT ON"          !Set channel 1's trigger state Active, waiting for trigger, mode.
```

b) Single trigger for channel 1 and channel 2, and detects sweep end by *OPC? Commands

```
5 DIM A$[10]
10 OUTPUT 717;":ABORt"          !Set all channel's trigger state to "Hold"
20 OUTPUT 717;":TRIG:SOUR BUS"          !Set trigger source as BUS. (Basically for *TRG command).
30 OUTPUT 717;":INIT1:CONT ON"          !Set channel 1's trigger state Active, waiting for trigger, mode.
40 OUTPUT 717;":INIT2:CONT ON"          !Set channel 2's trigger state Active, waiting for trigger, mode.
```

```
50 OUTPUT 717;":TRIG:SING"              !Send single trigger commands.
60 OUTPUT 717;"*OPC?"                   ! "*OPC?" commands return 1 after the whole sweep is completed.
70 ENTER 717;A$                         ! A$ is 1 after sweep is end.
80 PRINT "Measurement Complete"
90 END
```

c) Single trigger for channel 1 and channel 2, and detects sweep end using Status Byte Register.

This case, target register is bit 4 of Operation Status condition Register that sets to "1" during measurement. When bit 4 of Operation Status condition Register turns to "0", it means, the sweep ends. Thus, using negative transfer filter function, this program arrange Service Request Enable register turns to "1", when measurement is finished.

```
5 DIM A$[10]
10 OUTPUT 717;":ABORt"          !Set all channel's trigger state to "Hold"
20 OUTPUT 717;":TRIG:SOUR BUS"          !Set trigger source as BUS. (Basically for *TRG command).
30 OUTPUT 717;":INIT1:CONT ON"          !Set channel 1's trigger state Active, waiting for trigger, mode.
40 OUTPUT 717;":INIT2:CONT ON"          !Set channel 2's trigger state Active, waiting for trigger, mode.
50 OUTPUT 717;":STAT:OPER:PTR 0"        !Set positive transfer filter invalid in whole range
60 OUTPUT 717;":STAT:OPER:NTR 16"       !Set negative transfer filter valid at 16 (= bit 4)
70 OUTPUT 717;":STAT:OPER:ENAB 16"      !Set Operation Status Enable register valid at 16 (=bit 4)
80 OUTPUT 717;"*SRE 128"                !Set Service Request Enable Register valid at 128 (=bit 7)
90 OUTPUT 717;"*CLS"                    !Clear all status byte register
100 OUTPUT 717;"*OPC?"                  !Confirm that "*CLS" command effective
110 ENTER 717;A$
120 !
130 ON INTR 7 GOTO Meas_end             !Declare that if service request (SRQ) generates, goto "Meas_end"
140 ENABLE INTR 7;2                     !Set SRQ enable
150 OUTPUT 717;"*TRG"                   !Send trigger command
160 PRINT "Waiting..."
170 Meas_wait: GOTO Meas_wait           !Wait until SRQ generates using loop sentence.
180 Meas_end: OFF INTR 7
190 PRINT "Measurement Complete"
```

200 END

Please refer to Programming section of Help for the detail definition of status byte register.

3. Data collection

Followings are Readable (R) and Writable (W) measurement data arrays of each product.

871X series

- Raw data of A,B,R (R) (W)
- Error coefficient arrays(R) (W)
- Corrected Data(R) (W)
- Corrected Memory(R) (W)
- Formatted Data (R) (W)
- Formatted Memory (R) (W)

ENA 6 series

- Corrected Data (R) (W)
- Corrected Memory (R) (W)
- Formatted Data (R) (W)
- Formatted Memory (R) (W)

In ENA 6 series, raw data, and Error coefficient arrays are not accessible.

To read or write data arrays in ENA 6 series, users need to specify the eligible channel and trace by ":CALC[1-4]:PAR[1-4]:SEL" command.

Sample code for taking Channel 1's Trace 1 formatted data and stimulus data

```
10 REAL Fdata(1:201,1:2), Freq(1:201)      ! Define Fdata and Freq. Each measurement point has primary and secondary data. So Fdata is defined as two-dimensional array. For example, in Smith or Polar format, primary and secondary data are assigned to format type such as resistance ( R) and reactance (X) value. In other hands, other format such as a log magnitude format, secondary data is always 0.
20 OUTPUT 717;":FORM:DATA ASC"      !Set data transfer type as ascii.
```

```
30 OUTPUT 717;":CALC1:PAR1:SEL"        !Select eligible channel and trace for following commands
40 OUTPUT 717;":CALC1:DATA:FDAT?"      !Get formatted data array of selected trace (Ch1 Tr1)
50 ENTER 717;Fdata(*)
60 OUTPUT 717;":SENS1:FREQ:DATA?"      !Get stimulus data of channel 1
70 ENTER 717;Freq(*)
80 END
```

Other examples such as getting trace data with binary format are listed in programming section of Help.

4. Limit test setting

Each instruments has limit test function, but its setting process is different.
In ENA 6 series, limit test conditions are set using array data with
":CALCulate[1-4][:SELected]:LIMit:DATA" commands.
Please refer to programming section of Help for the detail data setting.

ENA 6 series does not have marker limit function in its firmware function.

5. Status byte register handling

Both 871X series and ENA 6 series have status byte register (STB), but register's number or definition is somewhat different. Followings are correspond chart of 871X series STB and ENA 6 series STB

871X		Name	Description	Correspond ENA 6 series register
Status Byte *STB? reads the value of the instrument's status byte. This is a non-destructive read. The Status Byte is cleared by the *CLS command.	Bit 2	Device Status Summary	(bit 2) is set to 1 when one or more enabled bits in the Device Status event register are set to 1.	No correspond register
	Bit 3	Questionable Status Summary	(bit 3) is set to 1 when one or more enabled bits in the Questionable Status event register are set to 1	Same register
	Bit 4	Message Available	(bit 4) is set to 1 when the output queue contains a response	Same register

*SRE <num> sets bits in the Service Request Enable register. The current setting of the Service Request Enable register is stored in non-volatile memory. If *PSC has been set, it will be saved at power on. *SRE? reads the current state of the Service Request Enable register.			message.	
	Bit 5	Standard Event Status Summary	(bit 5) is set to 1 when one or more enabled bits in the Standard Event Status event register are set to 1.	Same register
	Bit 6	Master Summary Status	(bit 6, when read by *STB) is set to 1 when one or more enabled bits in the Status Byte register are set to 1.	No correspond register
	Bit 6	Request Service	(bit 6, when read by serial poll) is set to 1 by the service request process.	Same register
	Bit 7	Operational Status Summary	(bit 7) is set to 1 when one or more enabled bits in the Operational Status event register are set to 1.	Same register
871X		**Name**	**Description**	**Correspond ENA 6 series register**
Device Status Register Status:DEVice	Bit 0	Key Pressed	(bit 0) is set to 1 when one of the analyzer's front panel keys has been pressed.	No correspond register
	Bit 1	Any Softkey Pressed	(bit 1) is set to 1 when one of the analyzer's softkeys has been pressed.	No correspond register
	Bit 2	Any External Keyboard Key Pressed	(bit 2) is set to 1 when a key has been pressed on an external keyboard connected to the DIN KEYBOARD connector on the rear panel of the analyzer.	No correspond register
	Bit 3	Front Panel Knob Turned	(bit 3) is set to 1 when the analyzer's front panel knob is turned.	No correspond register
871X		**Name**	**Description**	**Correspond ENA 6 series register**
Limit Fail Register STATus:QUEStionable:LIMit	Bit 0	Measurement Channel 1 Limit Failed	(bit 0) is set to 1 when limit testing is enabled and any point on measurement channel 1 fails the limit test, or when any enabled marker limit on measurement channel 1 has failed.	Questionable Limit Status Condition Register Bit 1 or Questionable Limt Channel 1 Status Condition Register Bit 1for trace 1 (If Meas 1 is assigned to ENA-L's channel 1 trace 1)
	Bit 1	Measurement Channel 2 Limit Failed	(bit 1) is set to 1 when limit testing is enabled and any point on measurement channel 2 fails the limit test, or when any enabled marker limit on measurement channel 2 has failed.	Questionable Limit Status Condition Register Bit 2 or Questionable Limit Channel 1 Status Condition Register Bit 2 for trace 2. (If Meas 2 is assigned to ENA-L's channel 1 trace 2)
	Bit 2	Measurement Channel 1	(bit 2) is set to 1 when any enabled marker limit on	No correspond register

		Marker Limit Failed	measurement channel 1 has failed.	
	Bit 3	Measurement Channel 2 Marker Limit Failed	(bit 3) is set to 1 when any enabled marker limit on measurement channel 2 has failed.	No correspond register
871X		**Name**	**Description**	**Correspond ENA 6 series register**
Questionable Status Register STATus:QUEStionable	Bit 9	Limit Fail	(bit 9) is set to 1 when one or more enabled bits in the Limit Fail event register are set to 1.	Questionable Status Condition Register Bit 10
	Bit 0	Data Questionable	(bit 10) is set to 1 when a change in the analyzer's configuration requires that new measurement data be taken.	No correspond register
871X		**Name**	**Description**	**Correspond ENA 6 series register**
Standard Event Status Register *ESR? reads the value of the standard event status register. *ESE <num> sets bits in the standard event status enable register. The current setting of the standard event statue enable register is stored in non-volatile memory. If *PSC has been set, it will be saved at power on. *ESE? reads the current state of the standard event status enable register.	Bit 0	Operation Complete	(bit 0) is set to one when the following two events occur (in the order listed): 1. The *OPC command is sent to the analyzer. 2. The analyzer completes all pending overlapped Commands	Same register
	Bit 1	Request Control	(bit 1) is set to 1 when both of the following conditions are true: ● The analyzer is configured as a talker/listener for GPIB operation. ● The analyzer is instructed to do something (such as plotting or printing) that requires it to take control of the bus.	No correspond register
	Bit 2	Query Error	(bit 2) is set when the command parser detects a query error. A query error indicates that one or both of the following actions occurred: ● An attempt to read data from the Output Queue when no data was present. ● That data in the Output Queue was lost. An example of this would be queue overflow.	Same register
	Bit 3	Device Dependent Error	(bit 3) is set to 1 when the command parser detects a device-dependent error. A device dependent error is any analyzer operation that did not execute properly due to some internal condition such as over range. This bit indicates that the error was not a command, query, or an execution error.	Same register

	Bit 4	Execution Error	(bit 4) is set to 1 when the command parser detects an execution error. Execution errors occur when the following conditions occur: ● A <PROGRAM DATA> element received in a command was outside the legal range for the analyzer, or inconsistent with the operation of the analyzer. ● The analyzer could not execute a valid command due to some analyzer condition.	Same register
	Bit 5	Command Error	(bit 5) is set to 1 when the command parser detects a command error. The following events cause a command error: ● An IEEE 488.2 syntax error occurred. This means that the analyzer received a message that did not follow the syntax defined by the 488.2 standard. ● A semantic error occurred. For example, the analyzer received an incorrectly spelled command. Another example would be that the analyzer received an optional 88.2 command that it does not implement.	Same register
	Bit 6	User Request	(bit 6) is not implemented. For keypress related functions, see "Device Status Register Set"	No correspond register
	Bit 7	Power On	(bit 7) is set to 1 when you turn on the analyzer.	Same register
871X		**Name**	**Description**	**Correspond ENA 6 series register**
Measuring Status Register STATus:OPERation:MEASuring	Bit 0	Channel 1 Measuring	(bit 0) is set to 1 while the analyzer is Collecting measurement data on channel 1.	Only Operation Status Condition Register Bit 4 for all channel's measurement condition.
	Bit 1	Channel 2 Measuring	(bit 1) is set to 1 while the analyzer is collecting measurement data on channel 2.	Only Operation Status Condition Register Bit 4 for all channel's measurement condition.
871X		**Name**	**Description**	**Correspond ENA 6 series register**
Averaging Status Regsiter STATus:OPERation:AVERaging	Bit 0	Measurement Channel 1 Averaging	(bit 0) is set to 1 while the analyzer is sweeping on measurement channel 1 and the number of sweeps completed (since "average restart") is less than the averaging factor.	No correspond register
	Bit 1	Measurement	(bit 1) is set to 1 while the	No correspond register

		Channel 2 Averaging	analyzer is sweeping on measurement channel 2 and the number of sweeps completed (since "average restart") is less than the averaging factor.	
871X		**Name**	**Description**	**Correspond ENA 6 series register**
Operational Status Register STATus:OPERation:MEASuring	Bit 0	Calibrating	(bit 0) is set to 1 while the instrument is zeroing the broadband diode detectors.	No correspond register
	Bit 1	Settling	(bit 1) is set to 1 while the measurement hardware is settling.	No correspond register
	Bit 4	Measuring	(bit 4) is set to 1 when one or more enabled bits in the Measuring Status event register are set to 1	Same register
	Bit 7	Correcting	(bit 7) is set to 1 while the analyzer is performing a calibration function.	Directory no correspond register. Operational Status Condition register Bit 4 may use
	Bit 8	Averaging	(bit 8) is set to 1 when one or more enabled bits in the Averaging Status event register are set to 1.	No correspond register
	Bit 9	Hardcopy Running	(bit 9) is set to 1 while the analyzer is performing a hardcopy (print or plot) function.	No correspond register
	Bit 10	Test Running	(bit 10) is set to 1 when one of the analyzer's internal service tests is being run.	No correspond register
	Bit 14	Program Running	(bit 14) is set to 1 while an HP Instrument BASIC program is running on the analyzer's internal controller.	Same register. For VBA programming.

Please refer to ENA 6 series programming section of Help for additional and detail information such as ENA 6 series unique status byte registers.