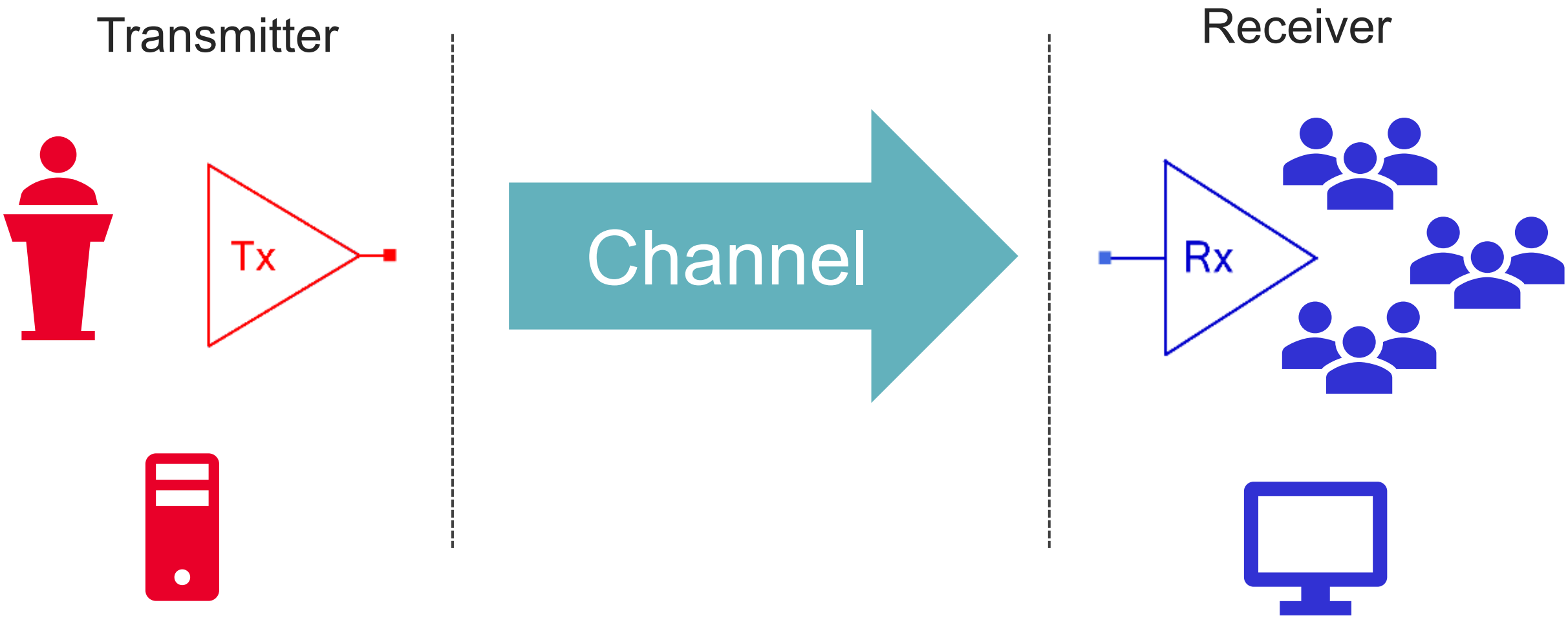
KEYSIGHT

Bridging Worlds: Mastering TDR and De-embedding through Simulation and Measurement

Presented by:
Mike Resso, Signal Integrity Application Scientist
Tim Wang Lee, PhD., Signal Integrity Application Scientist

Signal Integrity Is All Around Us



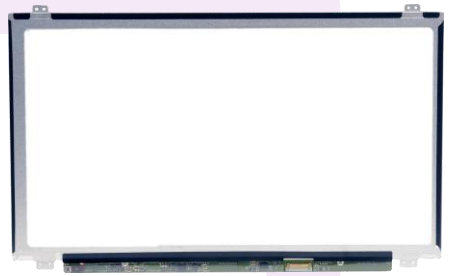
Signal Integrity in Digital Communication Channel

CPU

Graphic card

Cable

On board video processor

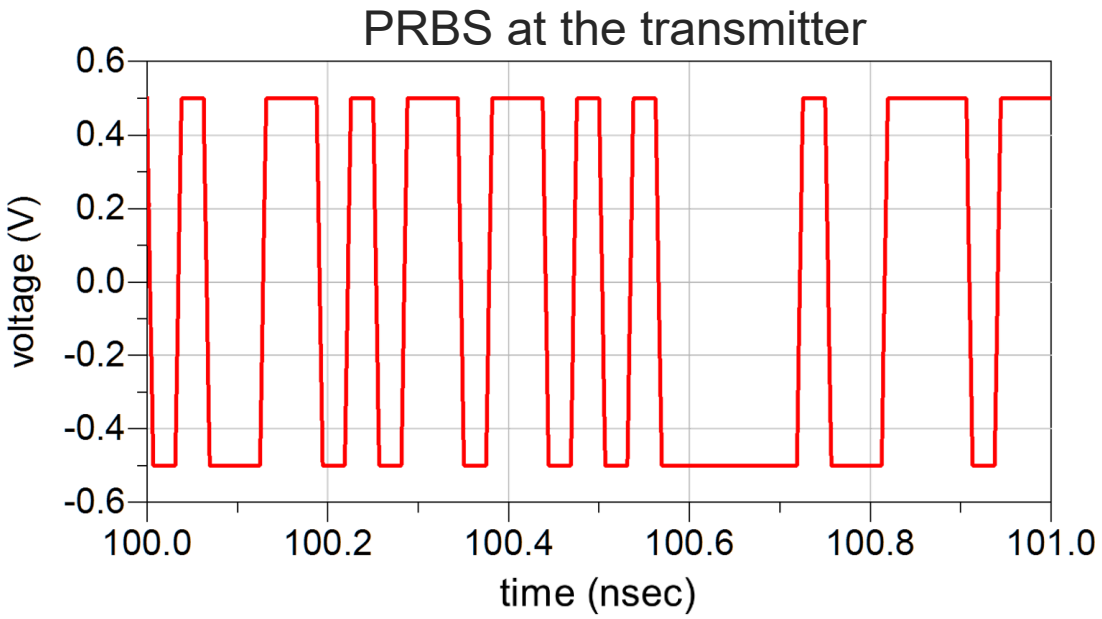


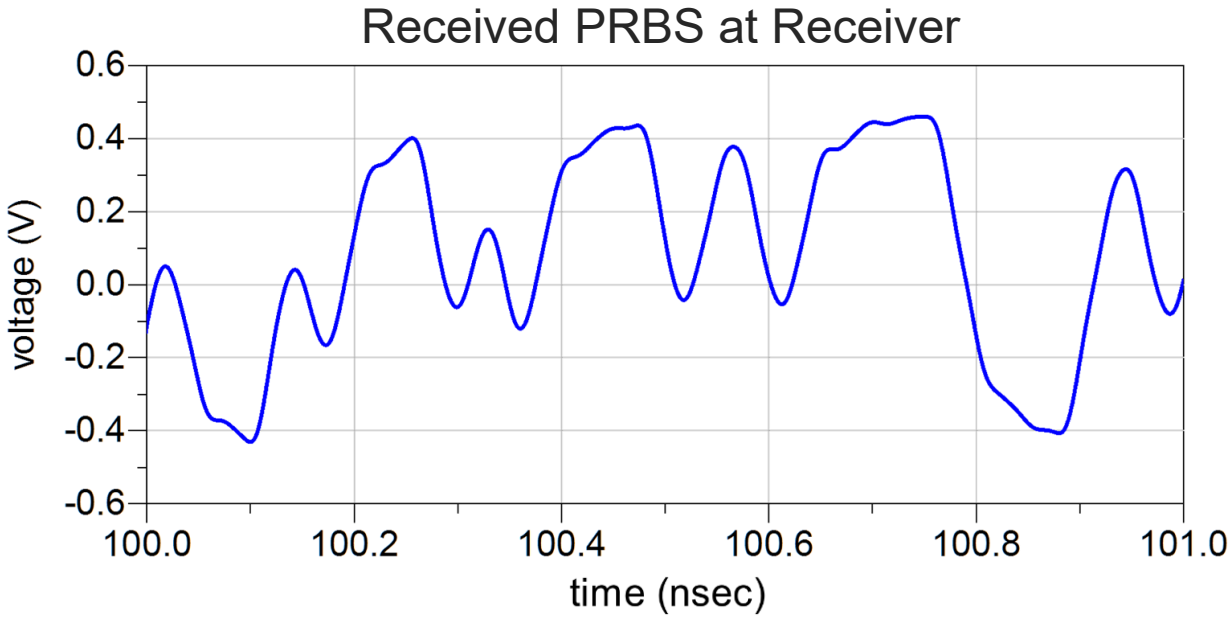
LED display

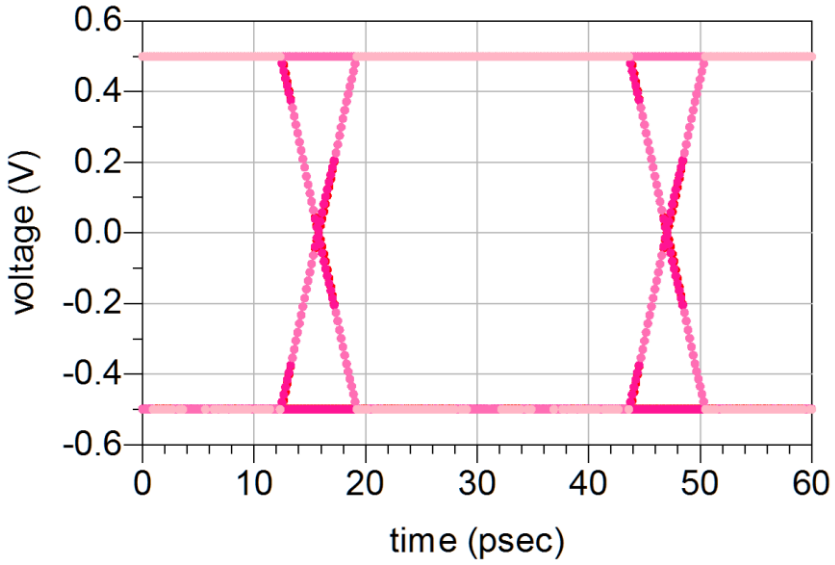
Interconnects

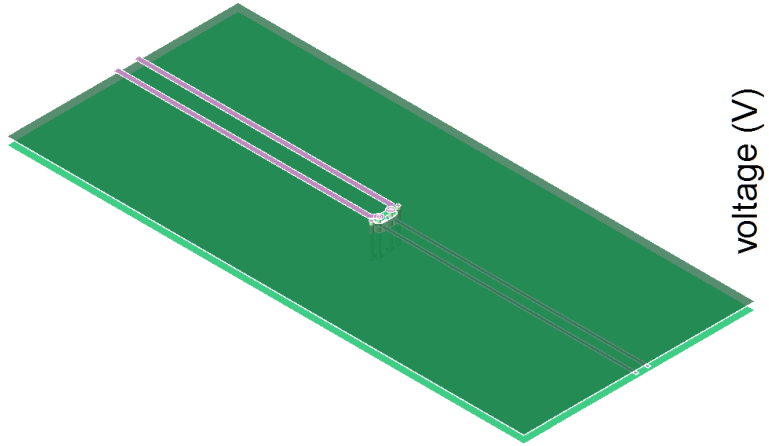
> Signal integrity is about the problems interconnects introduce and how to avoid them.
>
> – Dr. Eric Bogatin

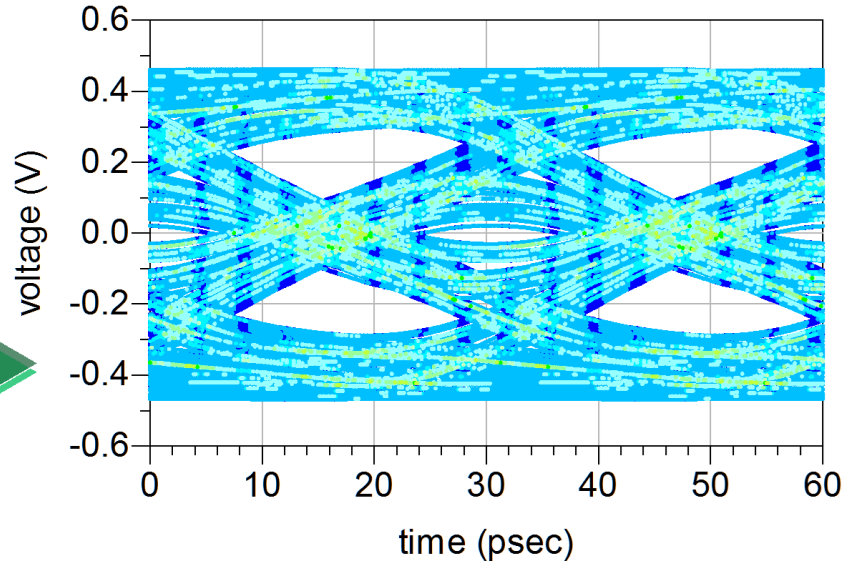
Closed Eye at the Receiver: Signal Integrity Problem



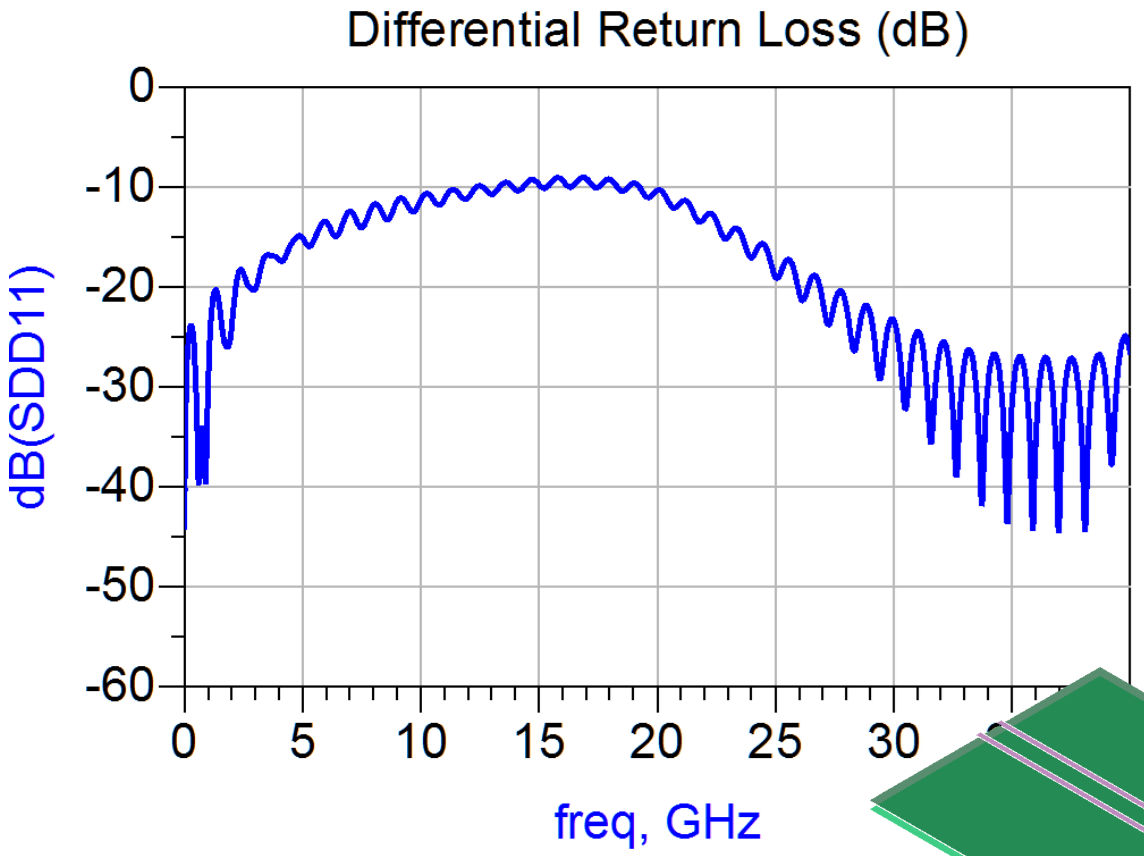


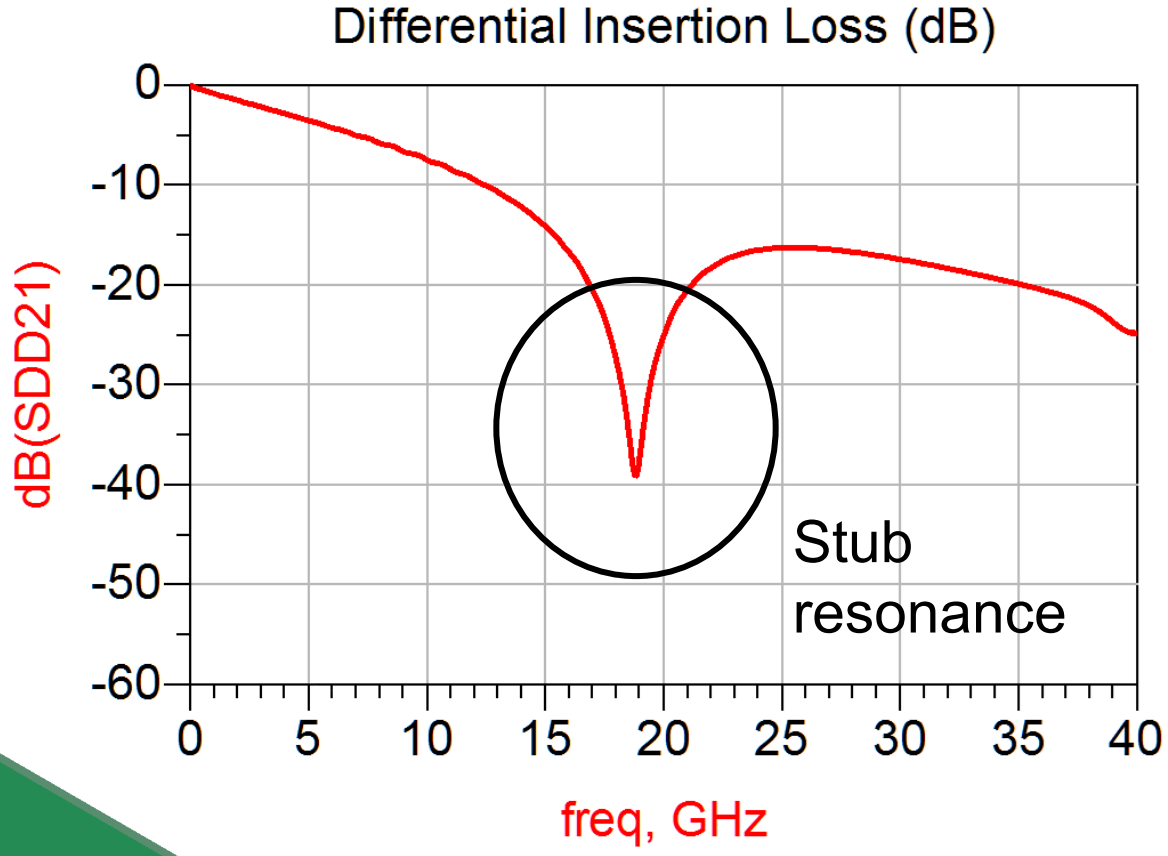


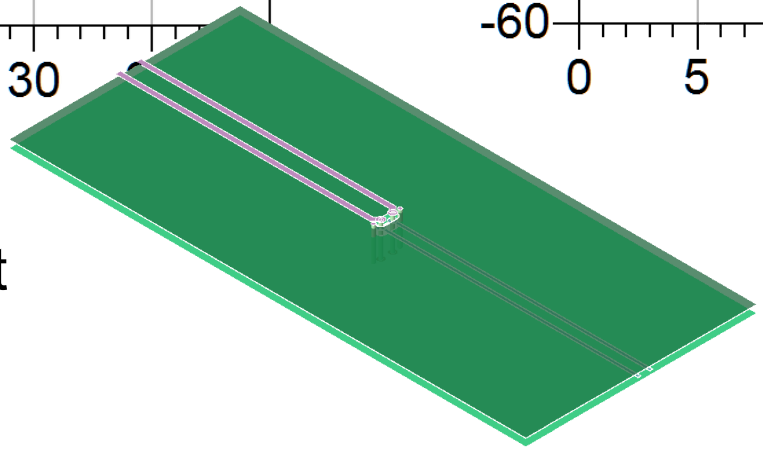




S-Parameters Do Not Directly Tell Us Impedance Information







S-parameters is useful but do not directly tell you the impedance information.

S-parameters is useful but do not directly tell you the length information.

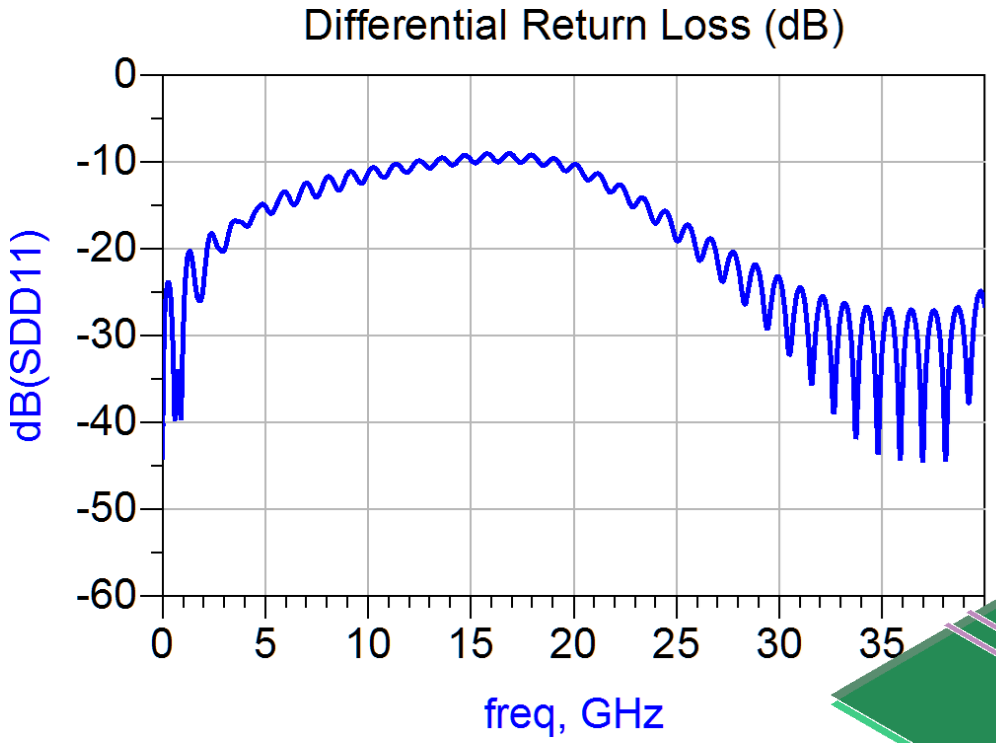
Agenda: Bridging the TDR Worlds

- TDR is the fastest path to physical insight
- What is the TDR telling us?
- How to get good TDR result from your S-parameters?

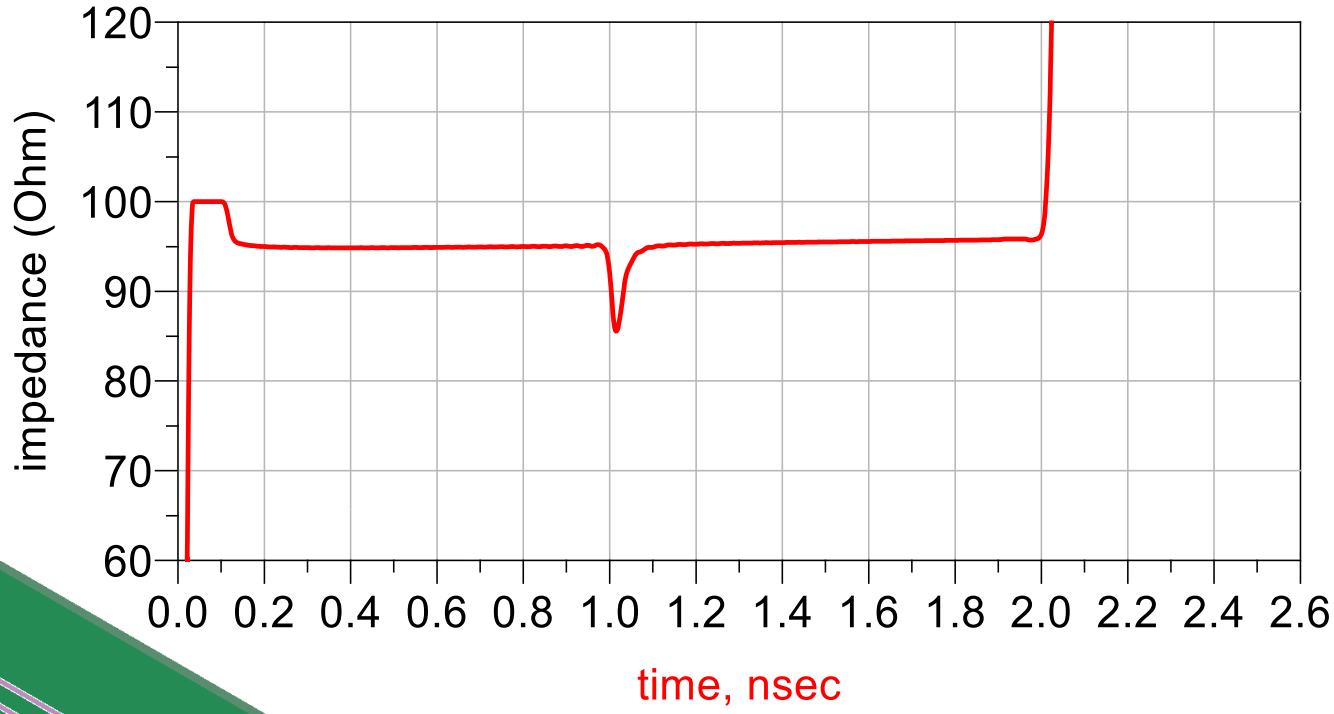
- From calibration, de-embedding to fixture removal
- How to best de-embed your fixtures
- Channel S-parameter measurement and TDR

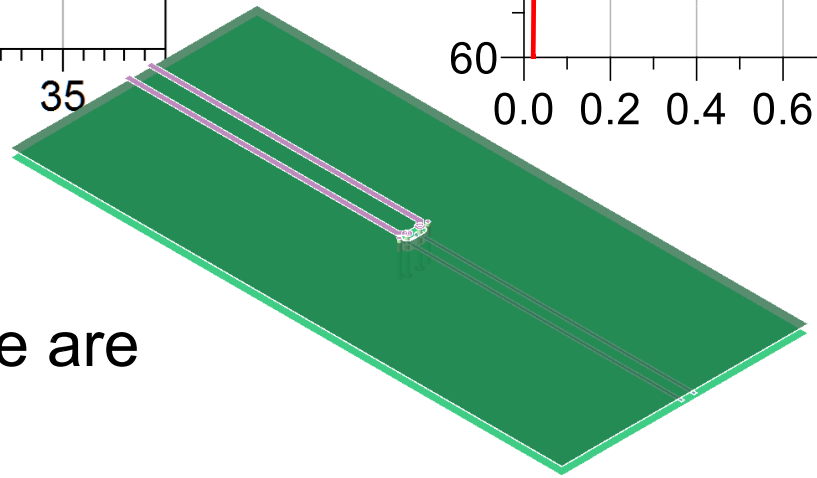
TDR Informs Us about DUT Timing and Impedances Quickly

S-parameter



TDR



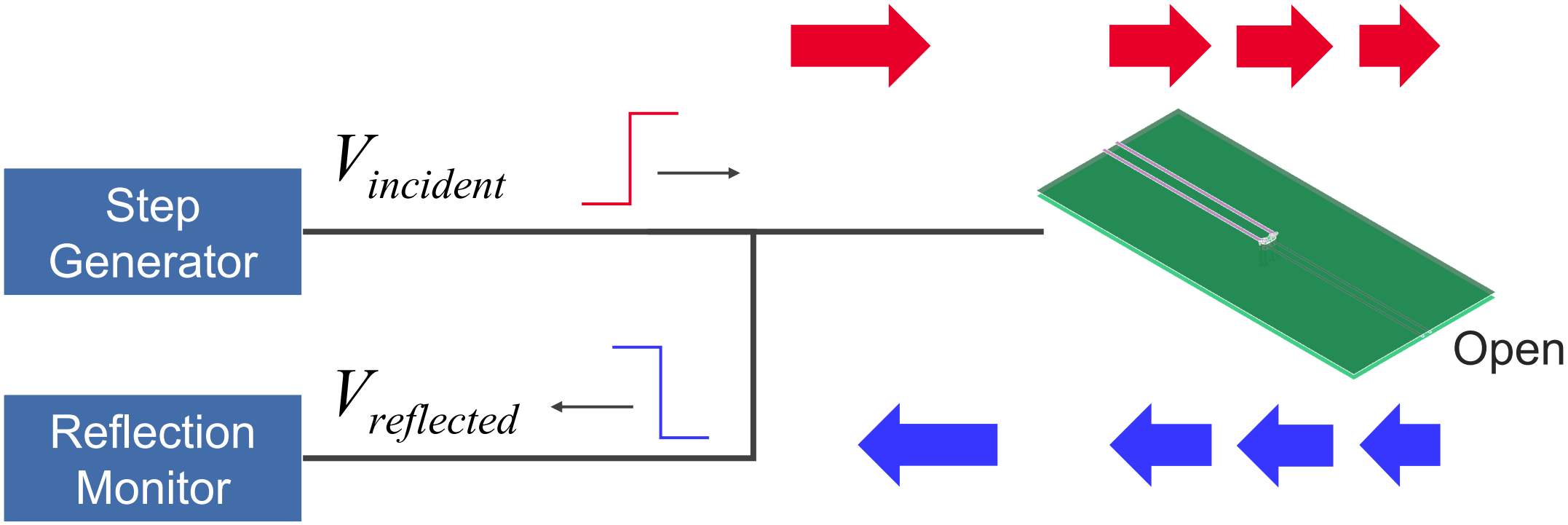


Hard to know what impedance profile we are looking at

Easy to know the impedance profile and the length of the structure

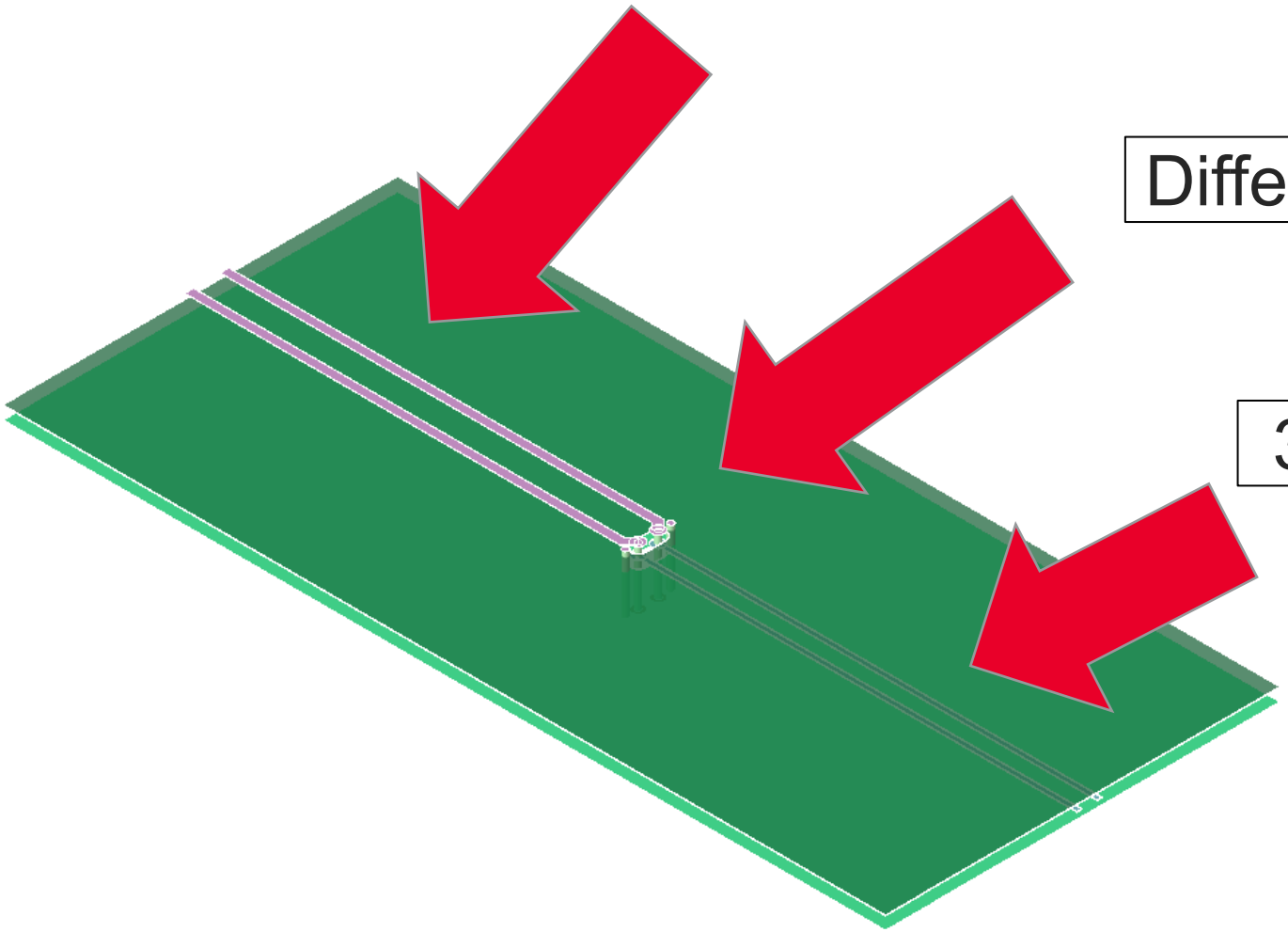
Perform TDR Calculation with the Device Under Test

$$Z_{DUT}(t) = Z_0 \frac{1+\Gamma(t)}{1-\Gamma(t)} \qquad \Gamma(t) = \frac{V_{reflected}(t)}{V_{incident}(t)}$$



First Glimpse of the Virtual Channel

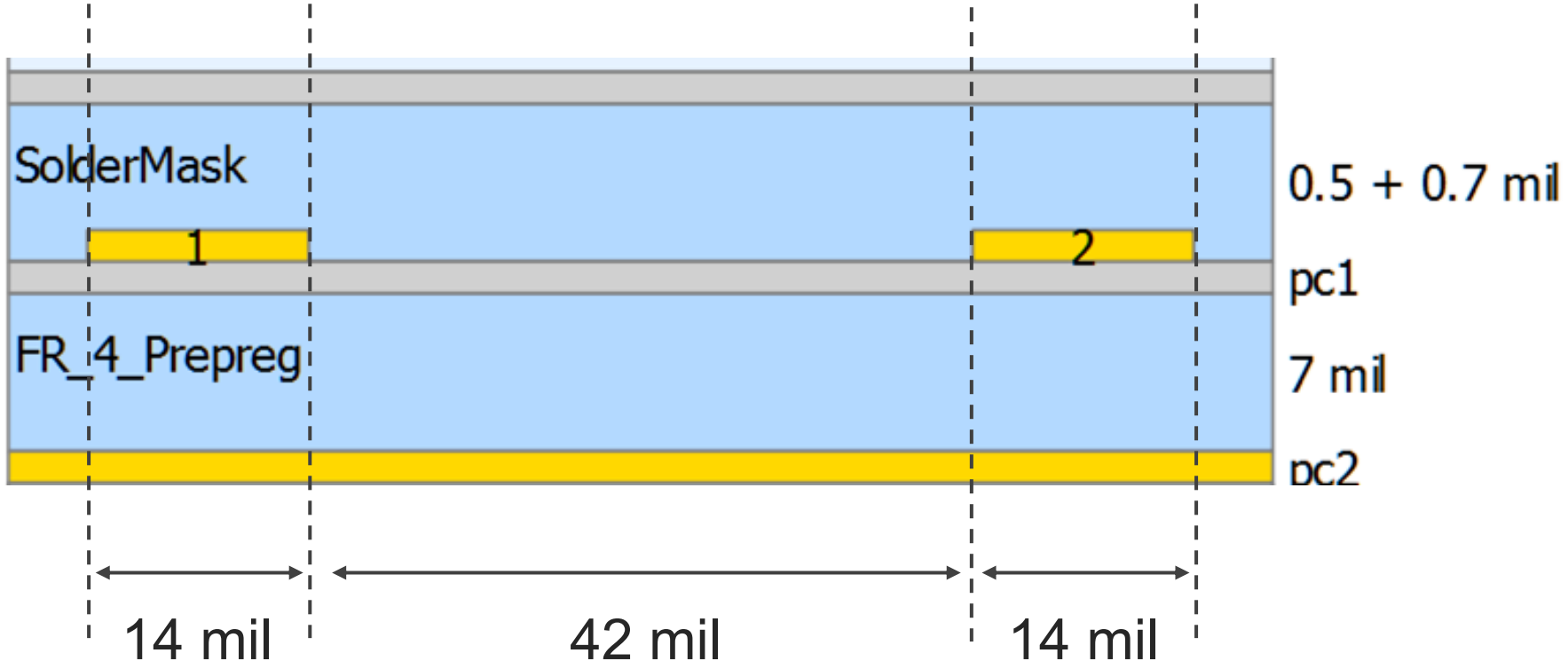
3-inch microstrip differential pair



Differential Via structure

3-inch stripline differential pair

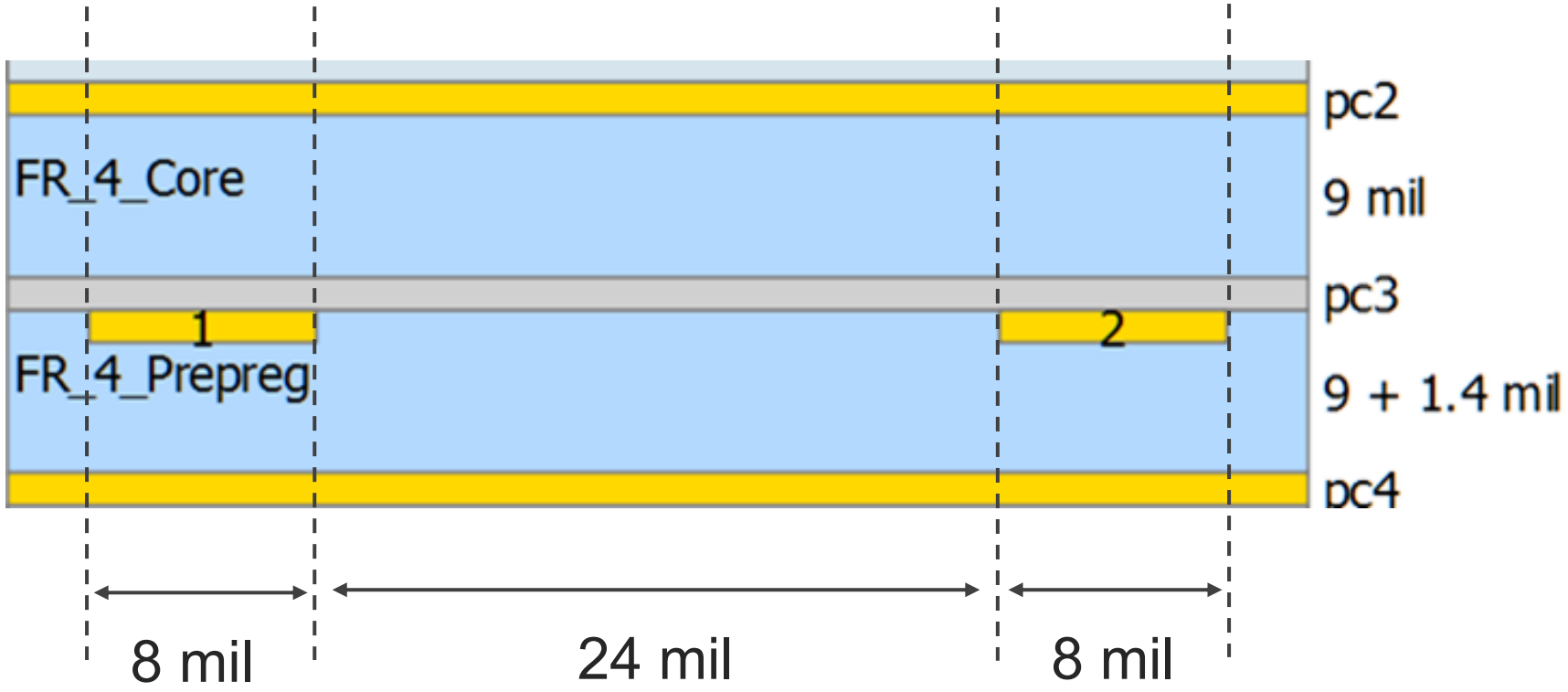
Estimate Z with the Cross-section of the Microstrip Diff Pair



Single-ended Microstrip Impedance
Rule of Thumb: W/H = 2 → Z = 50 Ohm

Because of solder mask, we expect:
differential impedance <100 Ohm

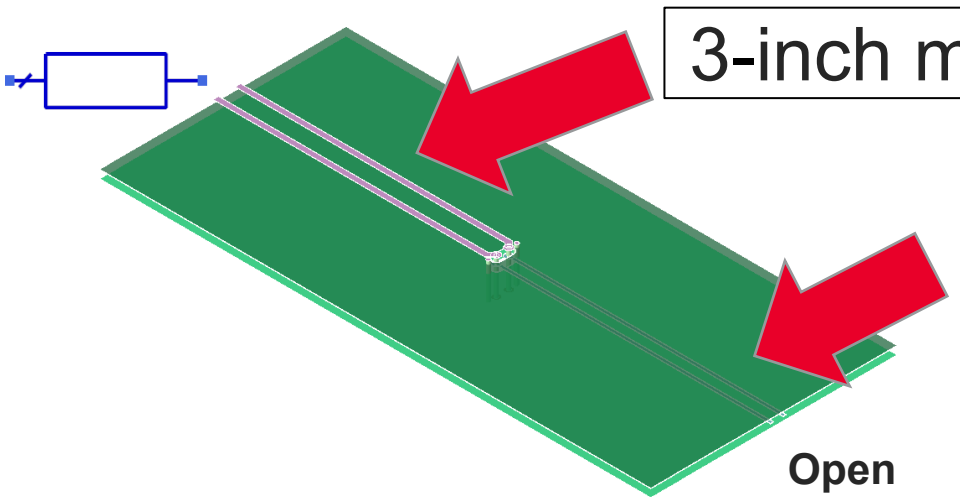
Estimate Z with the Cross-section of the Stripline Differential Pair



Single-ended Stripline Impedance
Rule of Thumb:
0.8 < W/min(H) < 1 → Z ~ 50 Ohm

We expect:
differential impedance ~100 Ohm

Expectation of Impedance Profile Before Simulation



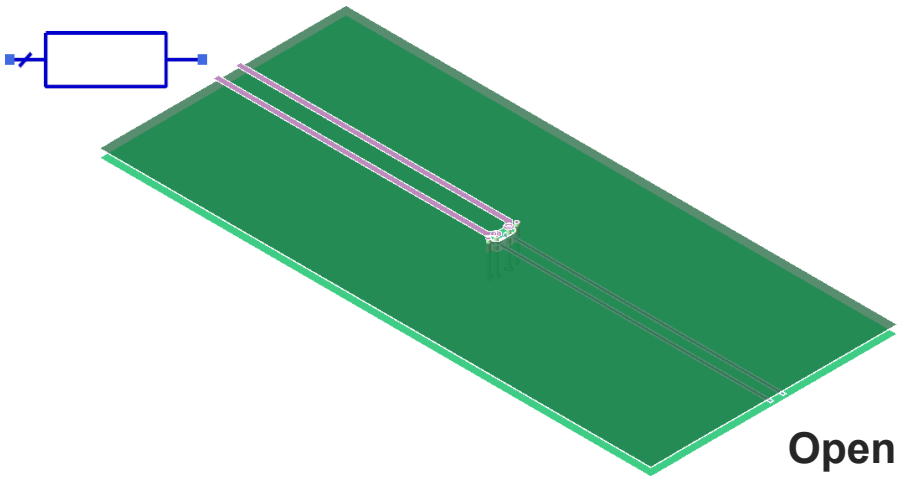
3-inch microstrip differential pair

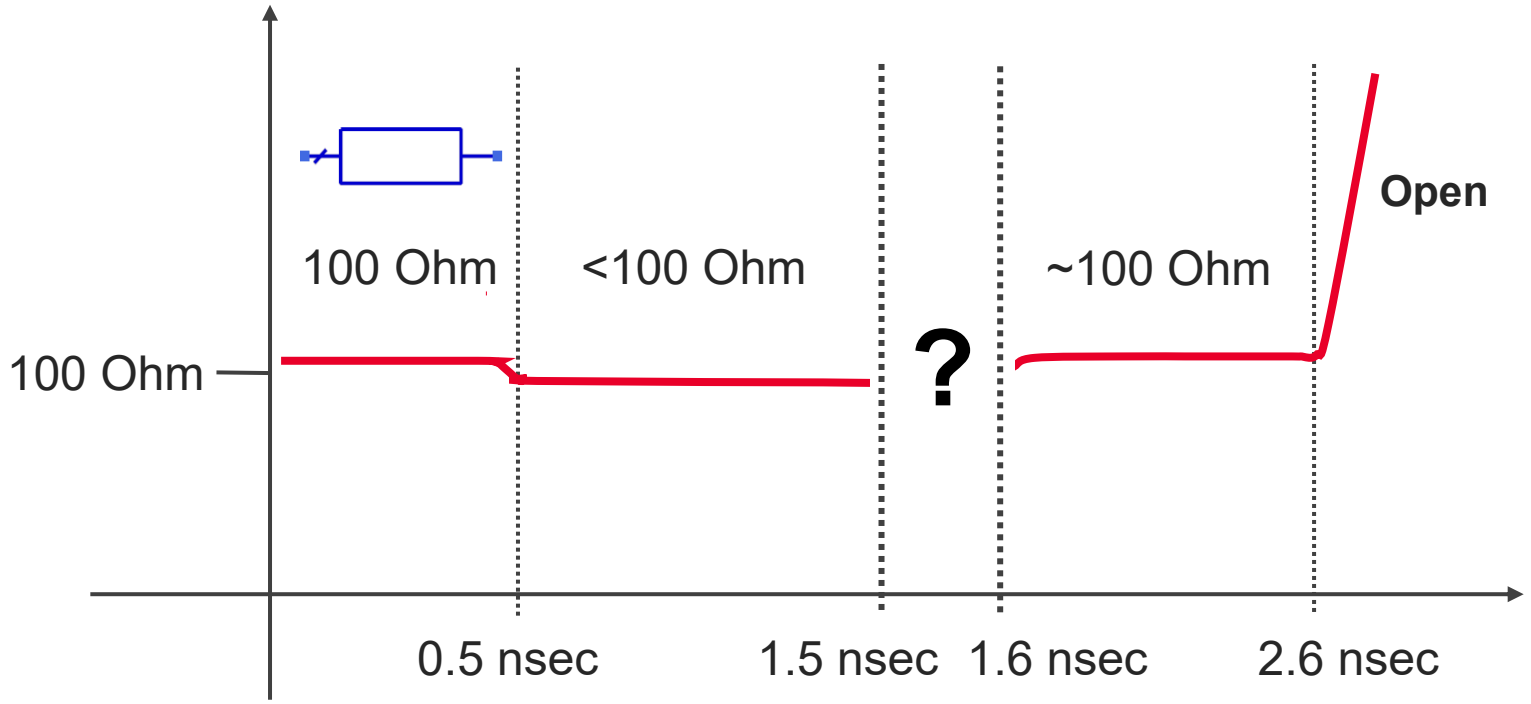
3-inch stripline differential pair

Estimated Delay (FR4): 6 in/nsec

Structure	3-inch microstrip	Via	3-inch stripline
Round Trip Delay (nsec)		Small	
Impedance (Ohm)	<100	?	~100

Expectation of Impedance Profile Before Simulation

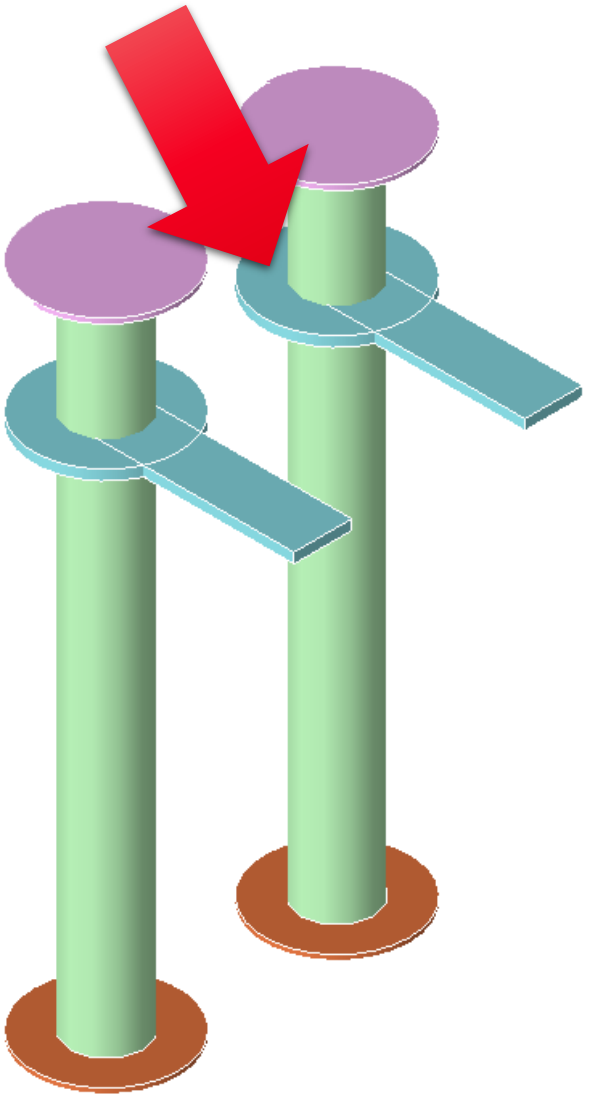


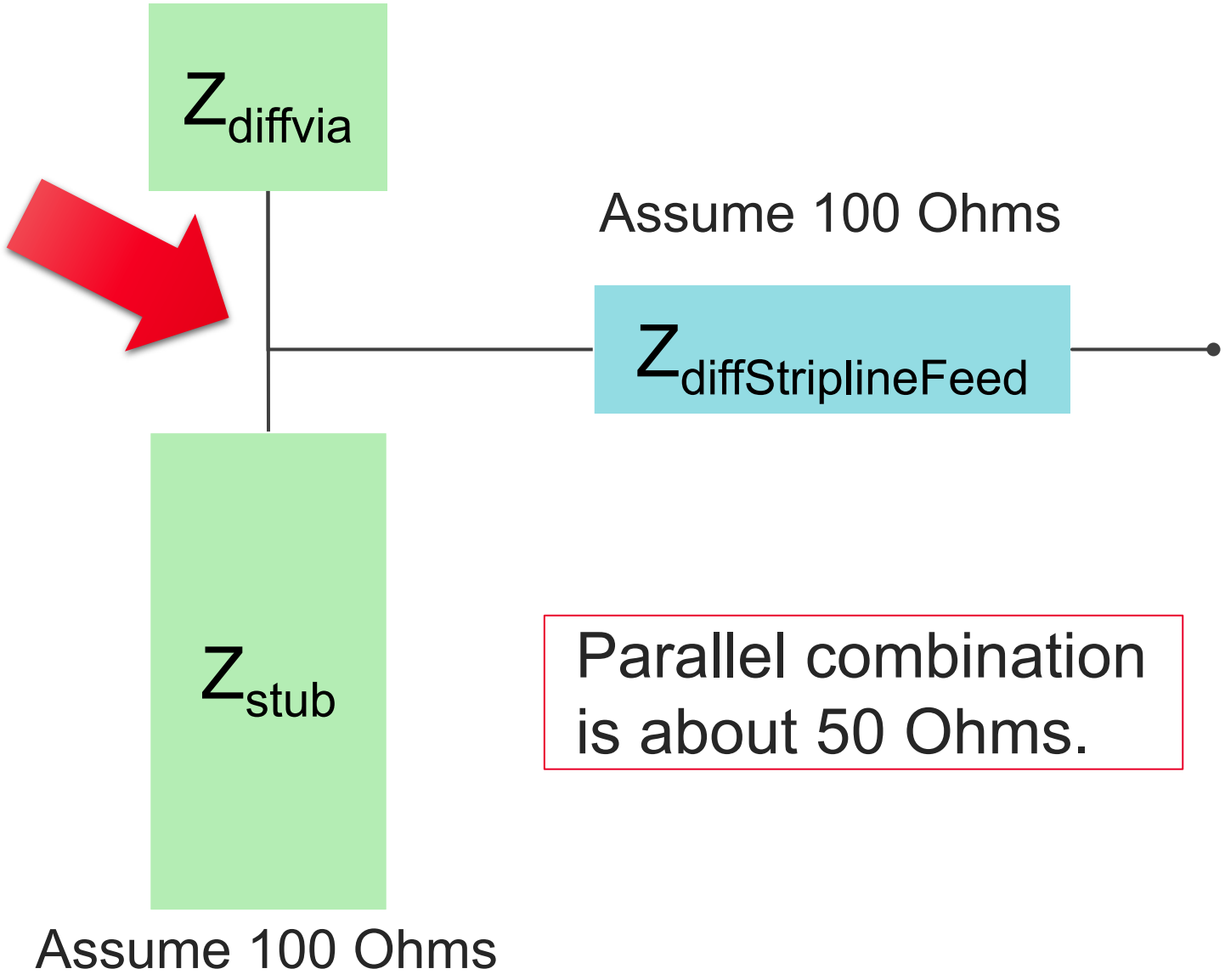


Estimated Delay (FR4): 6 in/nsec

Structure	3-inch microstrip	Via	3-inch stripline
Round Trip Delay (nsec)	1	Small	1
Impedance (Ohm)	<100	?	~100

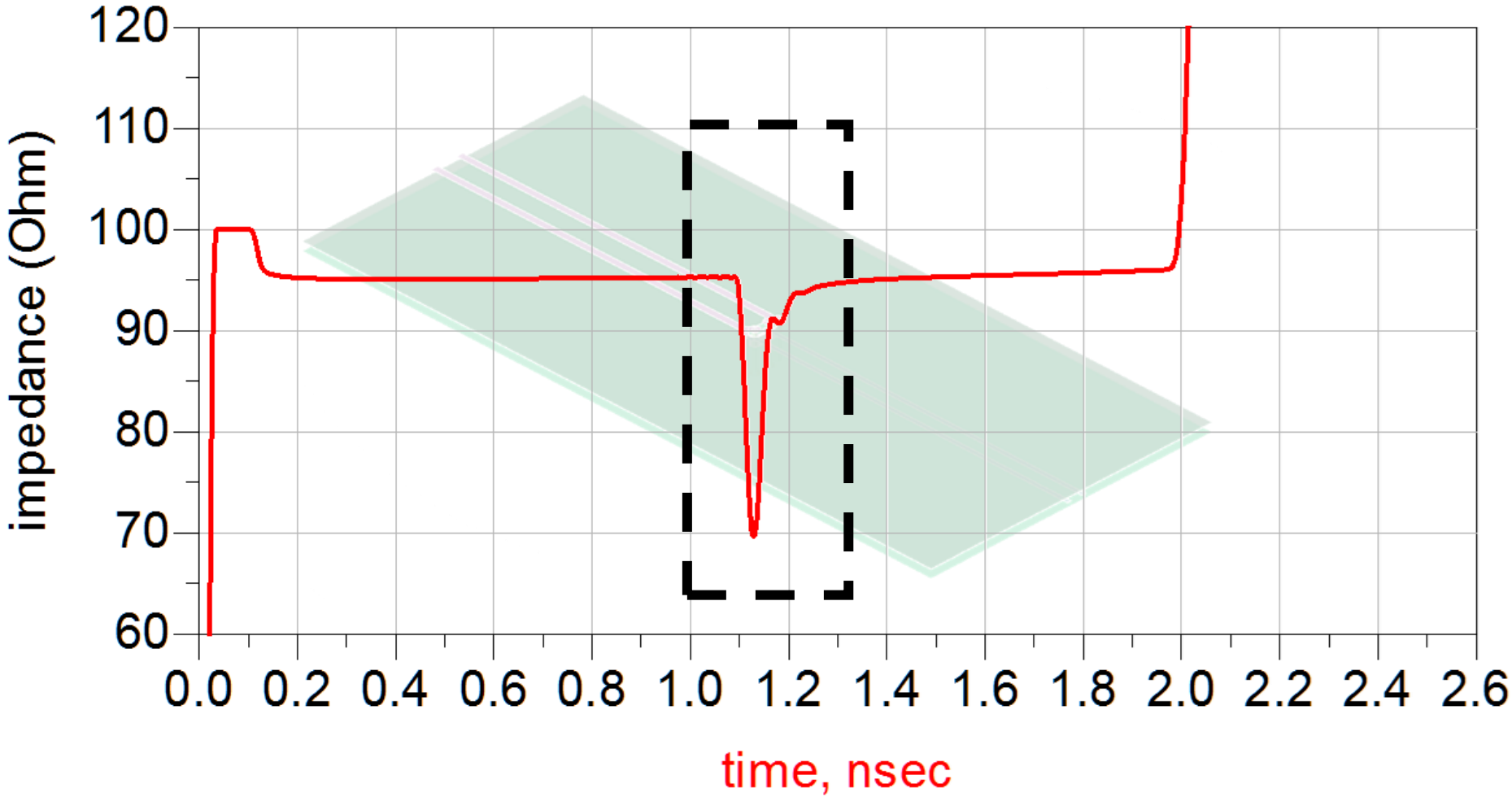
Examine Via Structure to Estimate Impedance





Parallel combination is about 50 Ohms.

Low Impedance Shown in TDR is Consistent

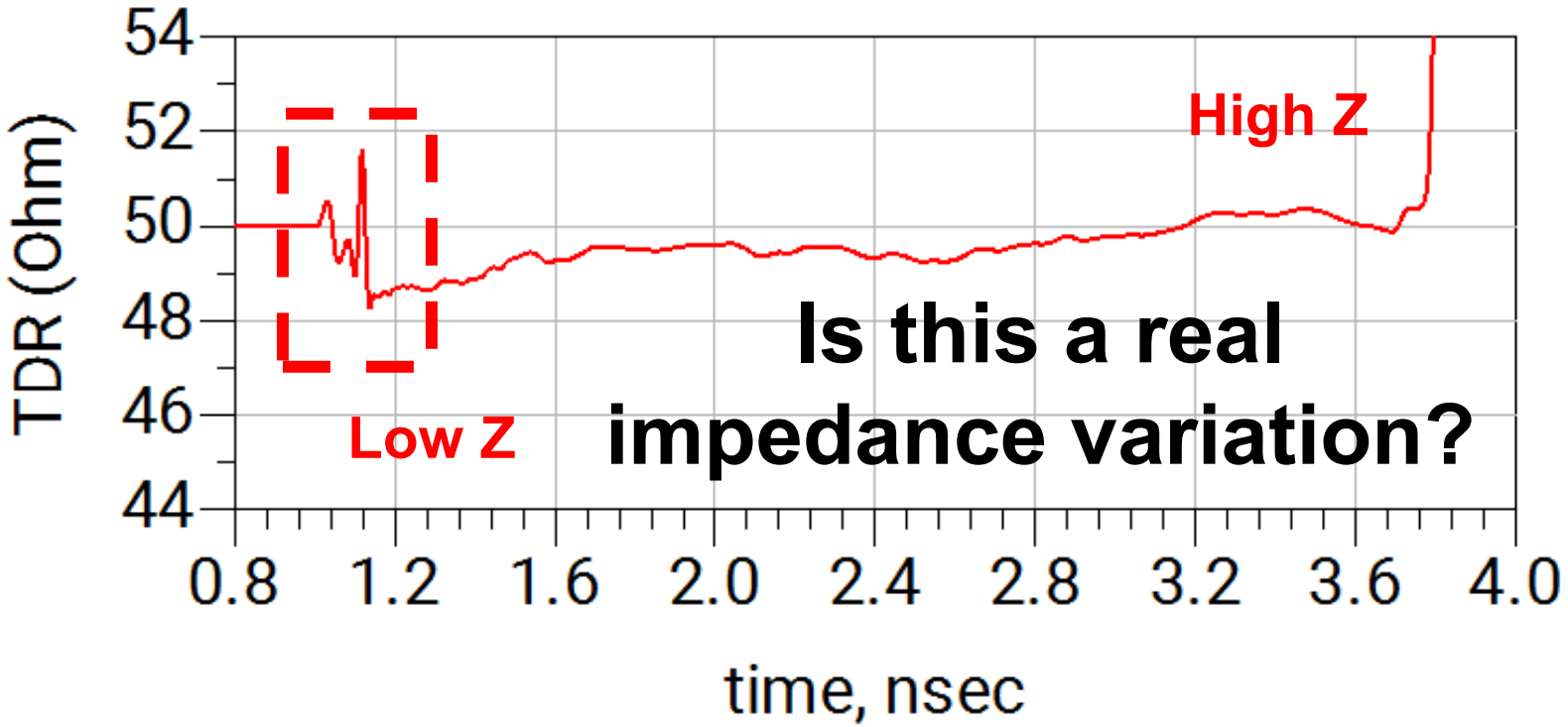


KEYSIGHT

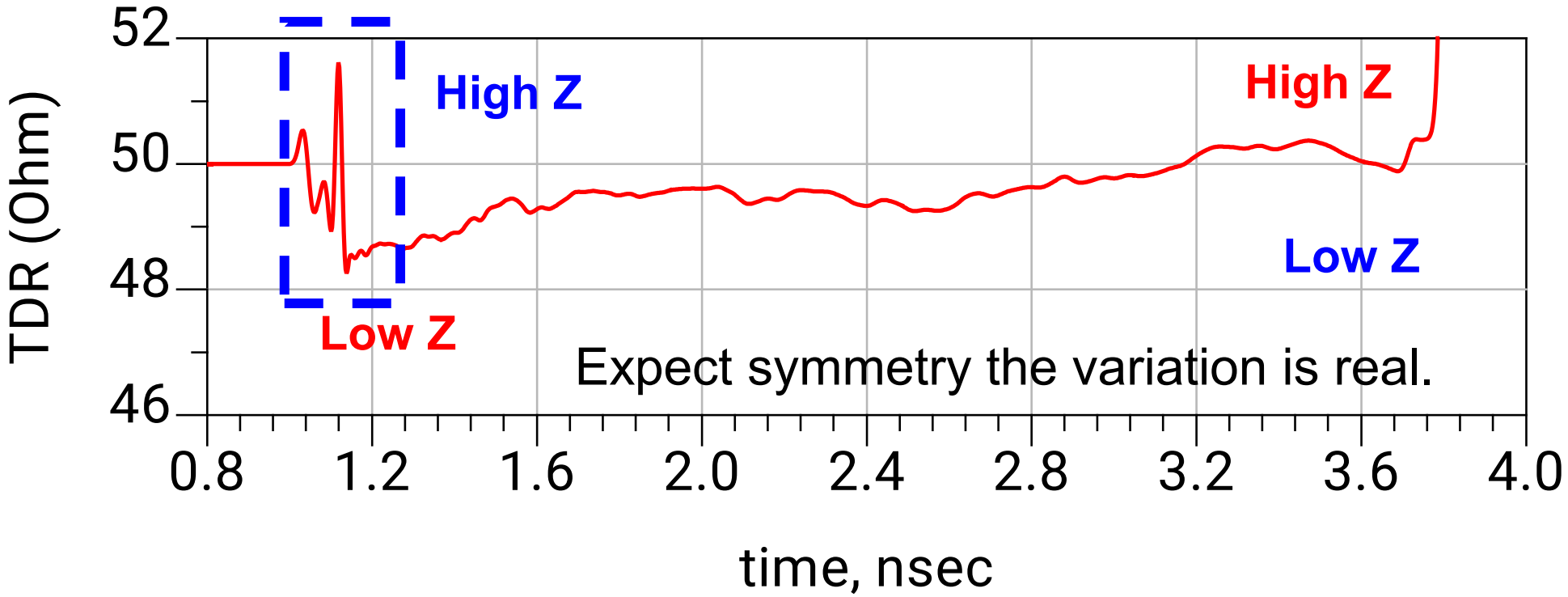
ADS TDR Demo with a measurement from the WRT Board

TDR Anatomy: Fixture, Trace and Impedance Variation TDR11

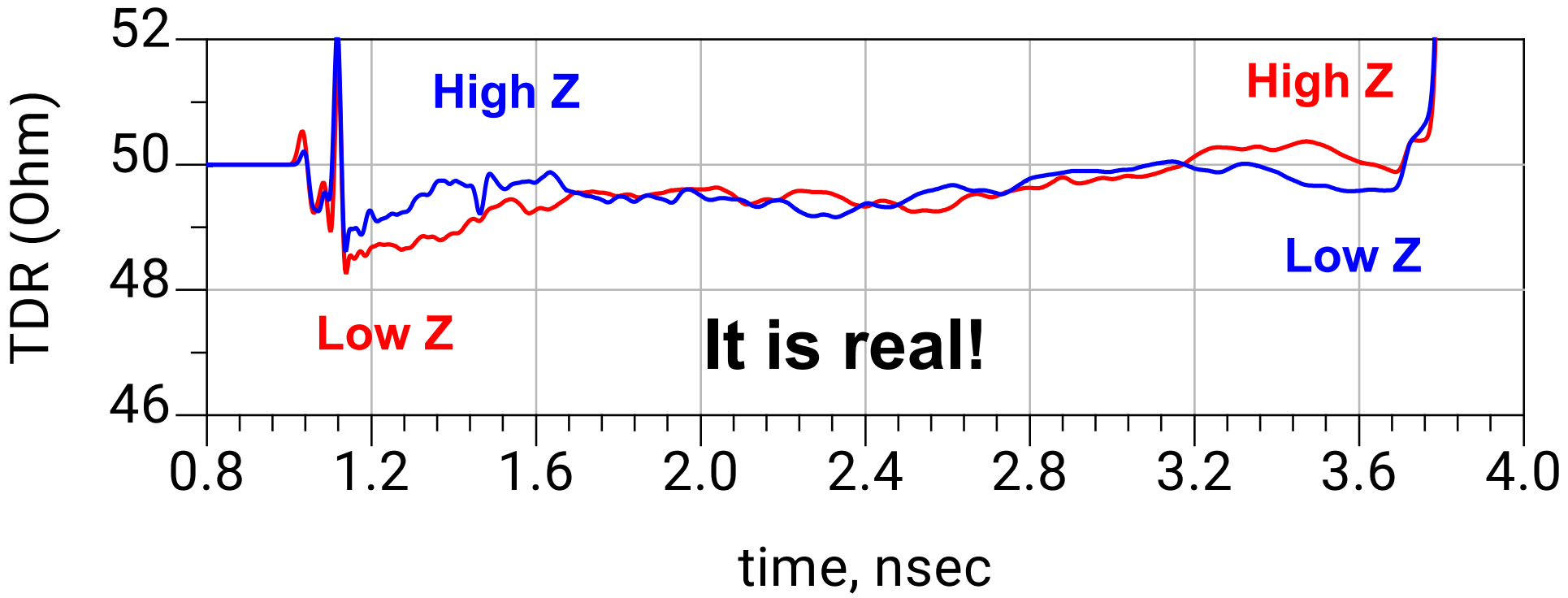
Impedance starts lower than 50 Ohm and reaches higher than 50 Ohm



Plot TDR11 and TDR22 to Determine Impedance Variation

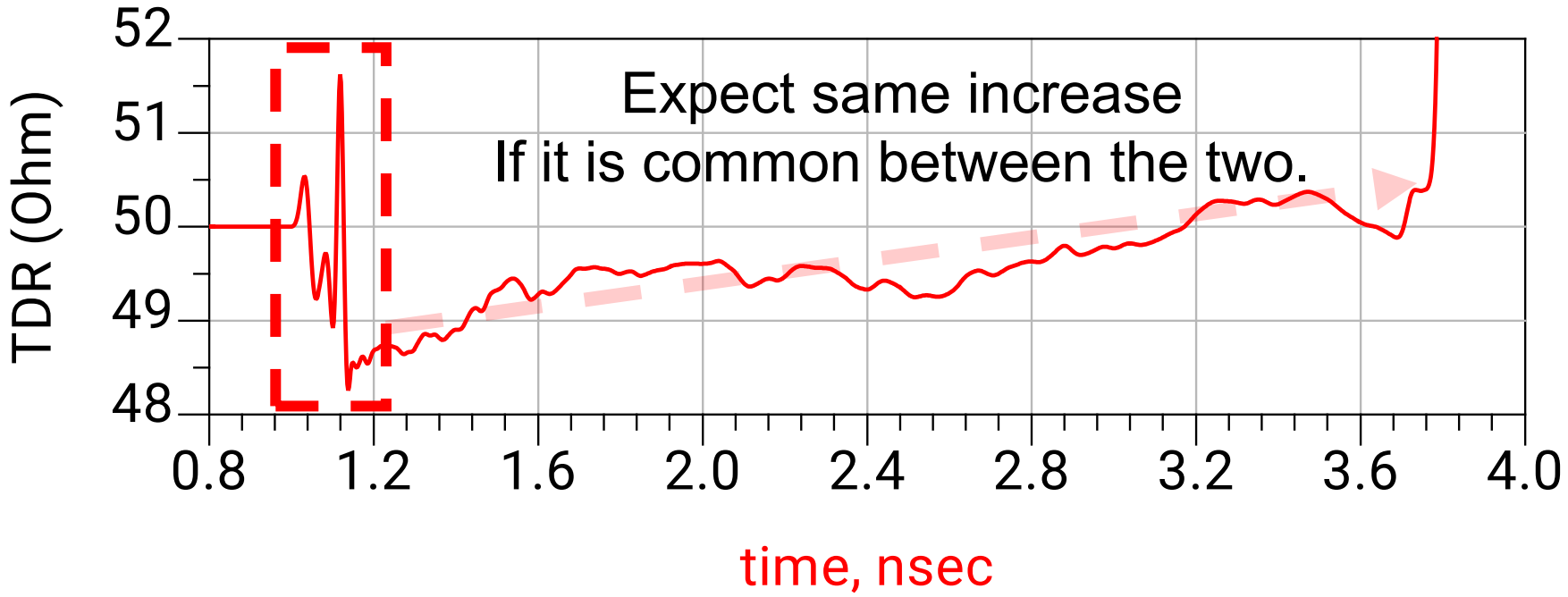


Plot TDR11 and TDR22 to Determine Impedance Variation

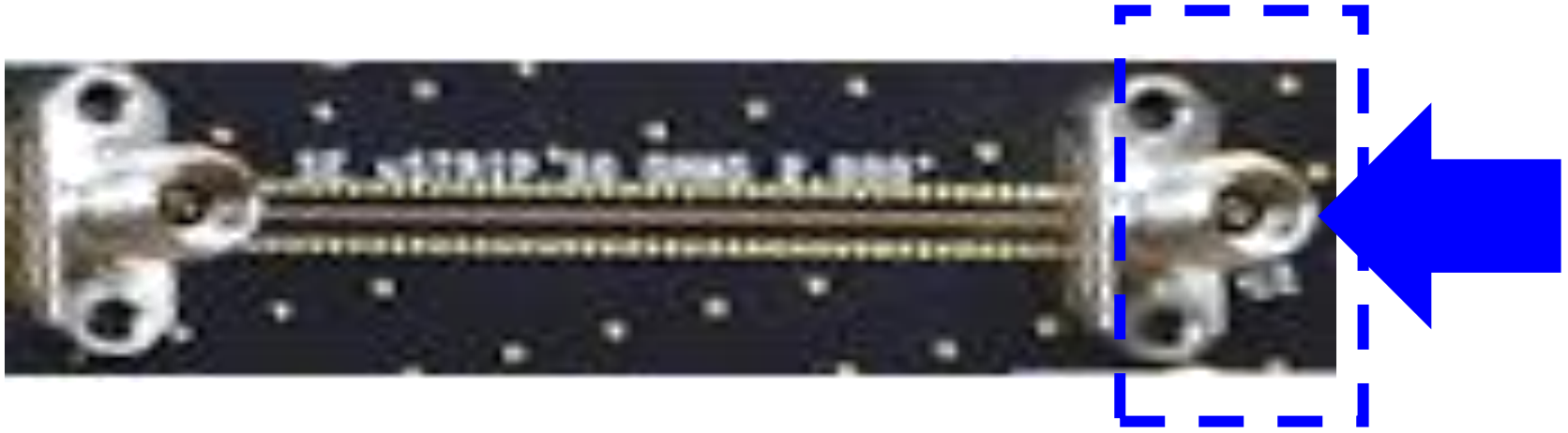


TDR Anatomy: Fixture, Trace and Impedance Variation TDR11

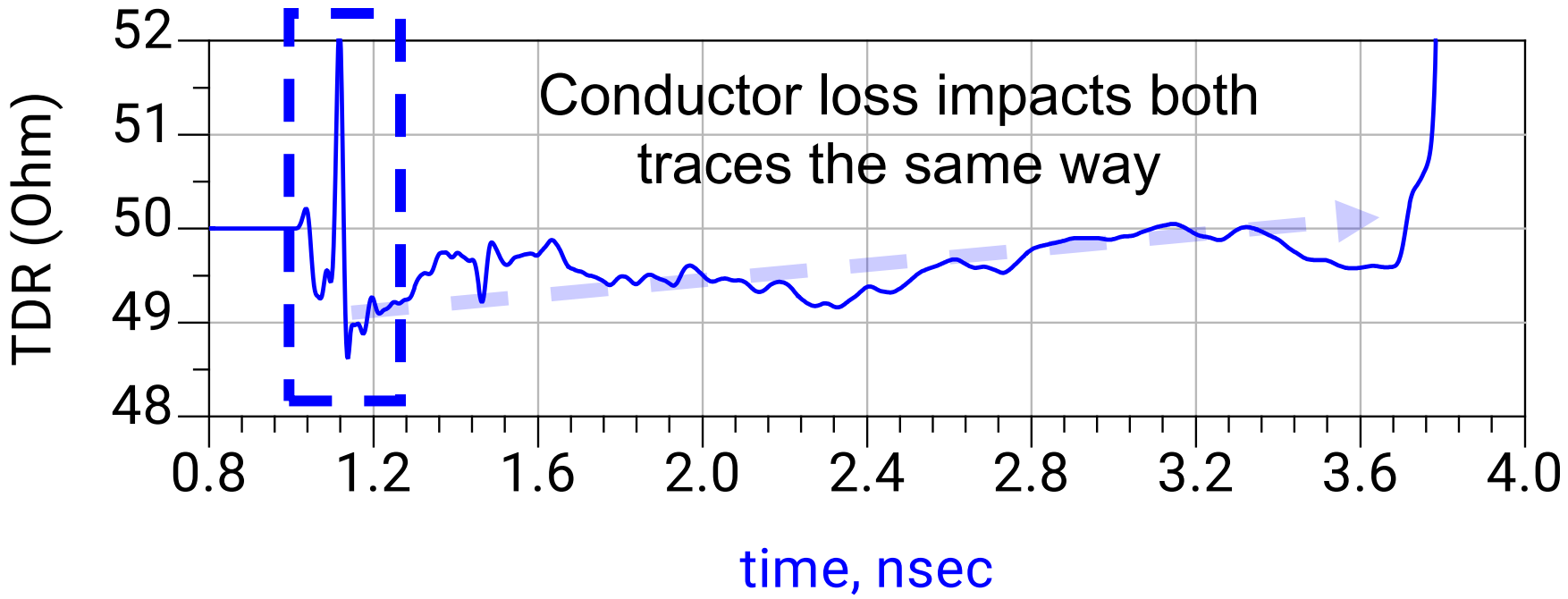
Impedance gradually go from low to high for TDR11



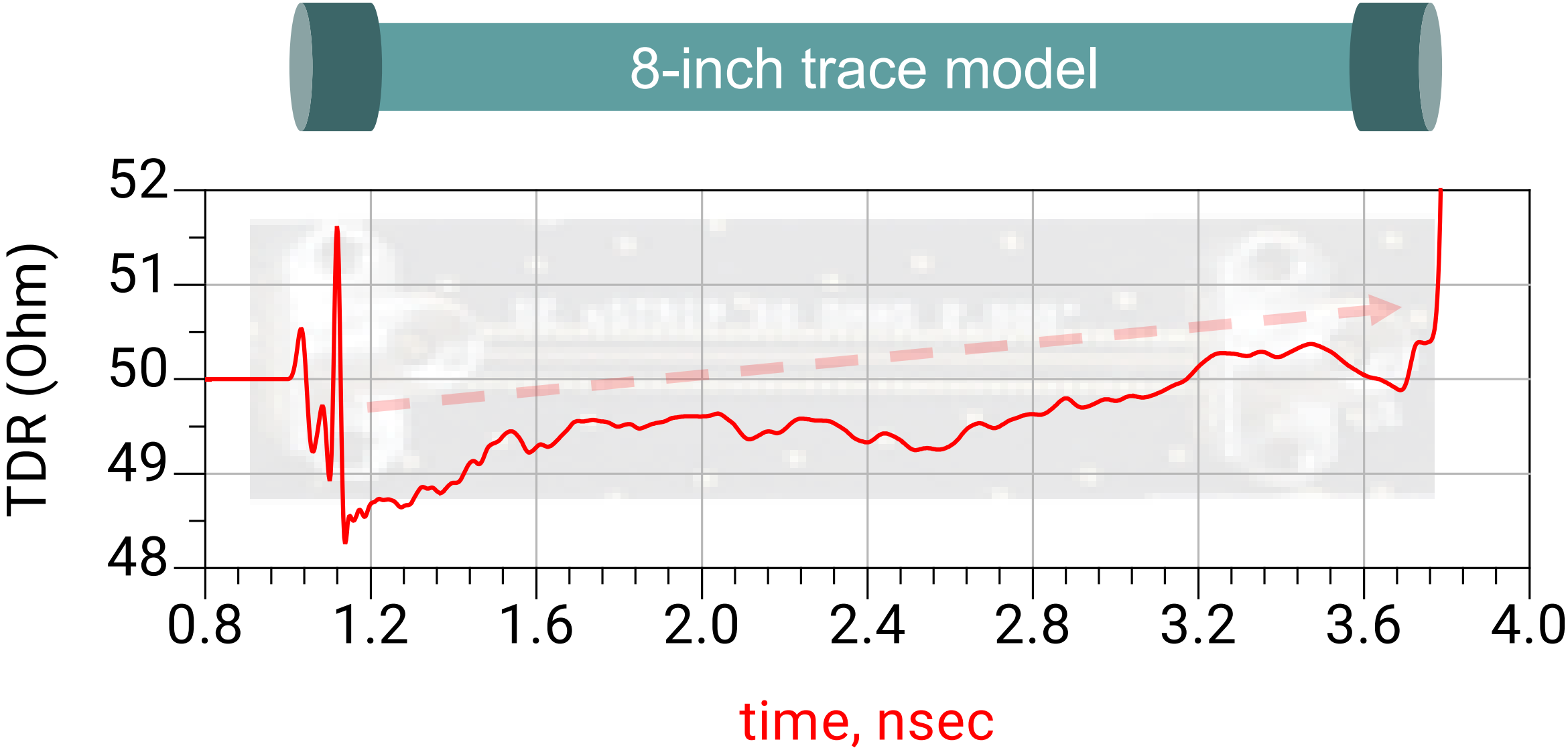
TDR Anatomy: Fixture, Trace and Impedance Variation TDR22



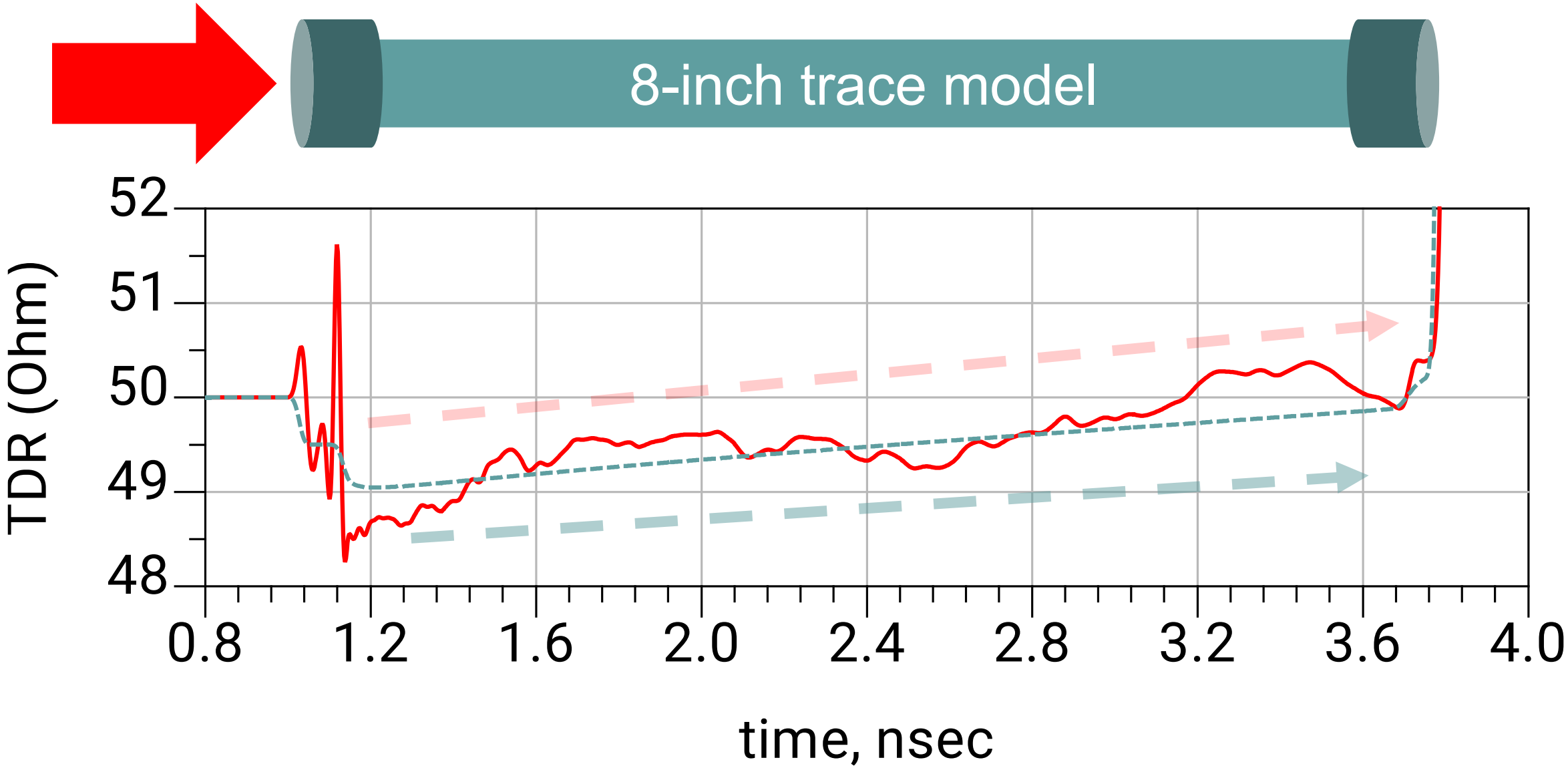
Impedance gradually go from low to high for TDR22



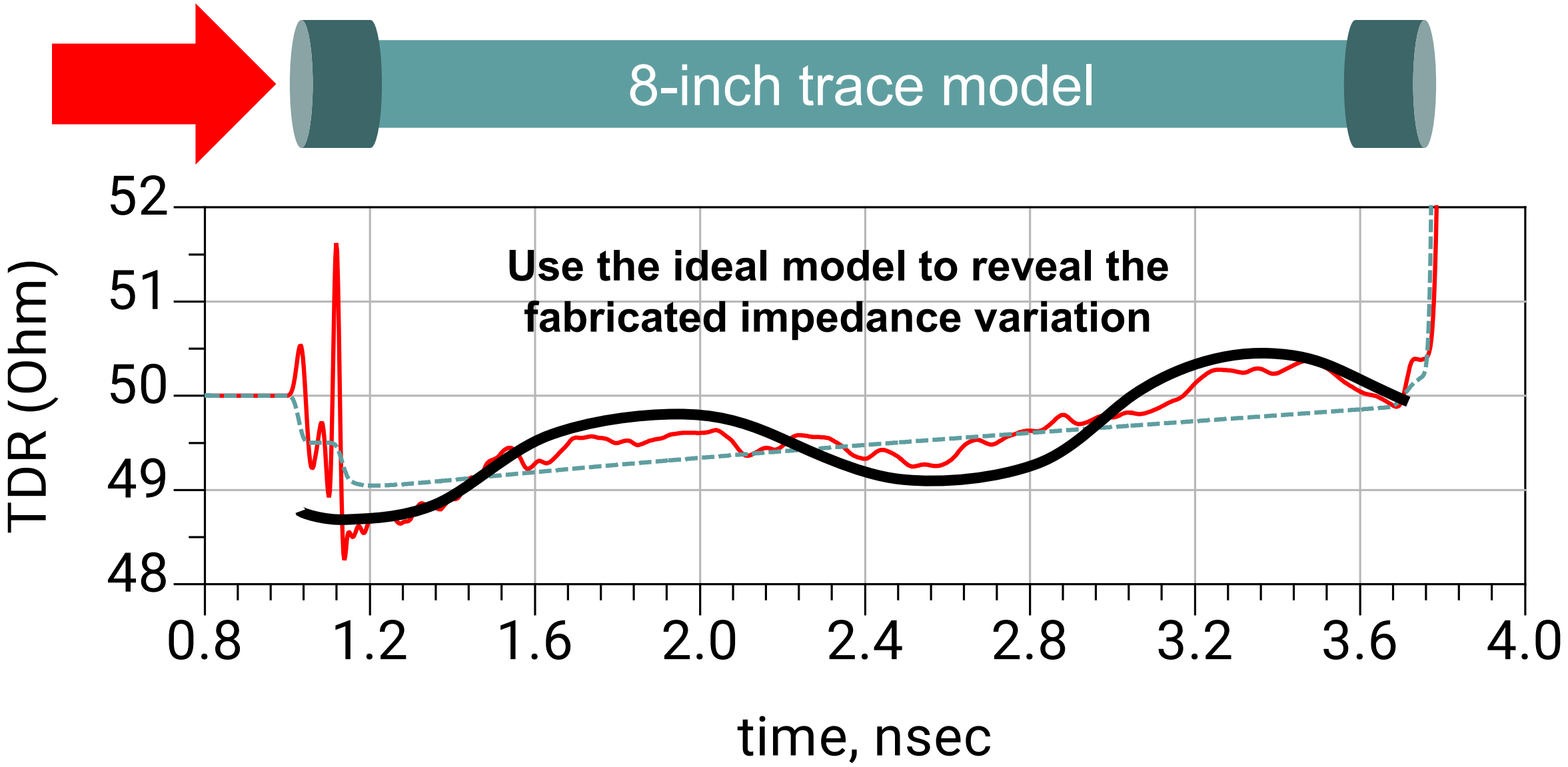
Transmission Line Model Confirms Conductor Loss



Transmission Line Model Confirms Conductor Loss

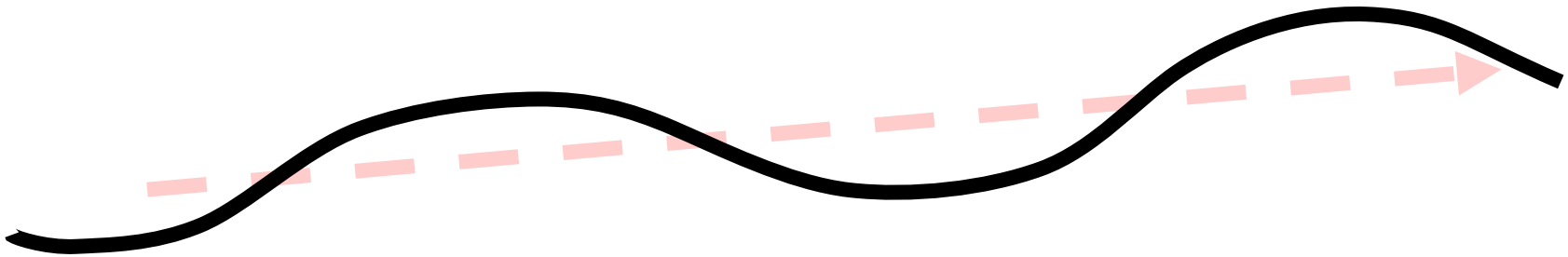


Comparison Shows Impedance change over Trace length



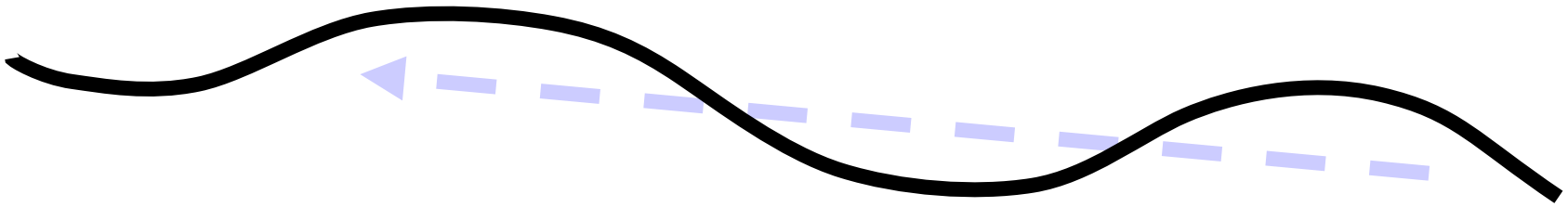
Comparison Shows Impedance change over Trace length

Expect the same pattern
If it is common between the two traces.



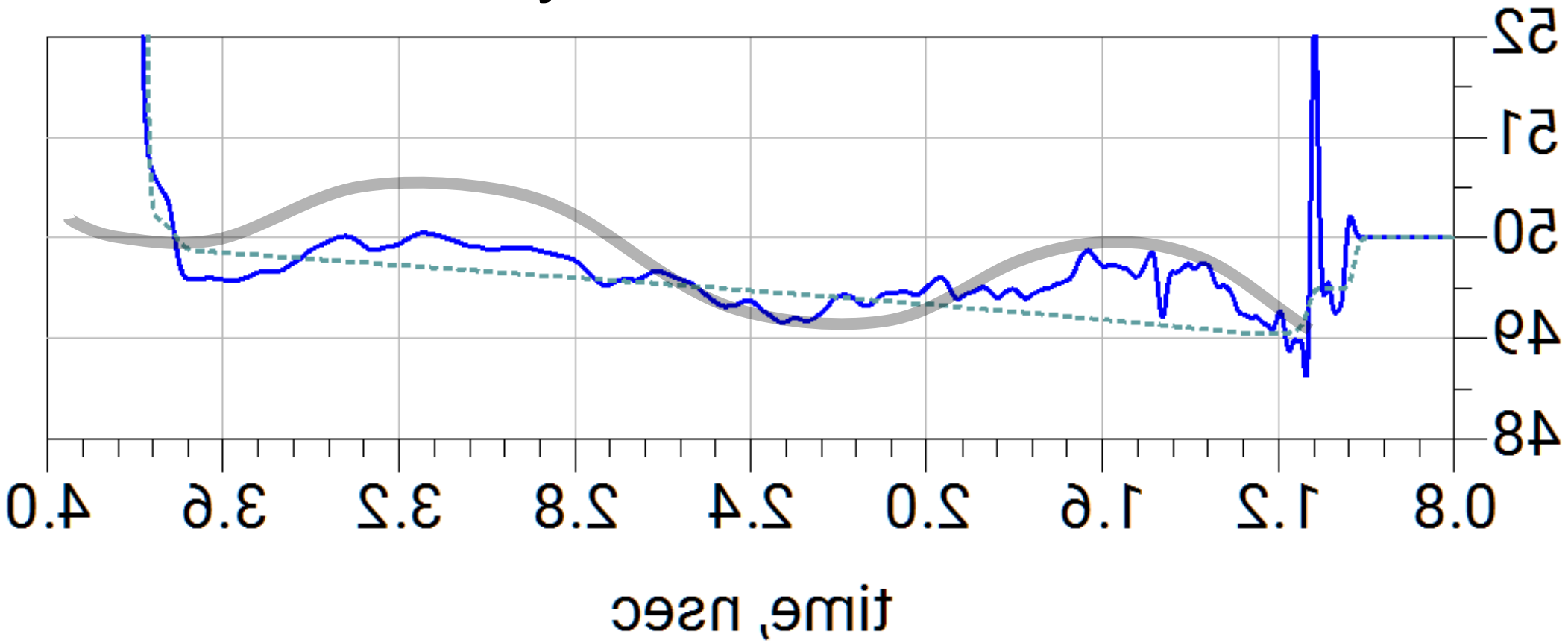
Comparison Shows Impedance change over Trace length

Expect the same impedance variation pattern in addition to conductor loss increase

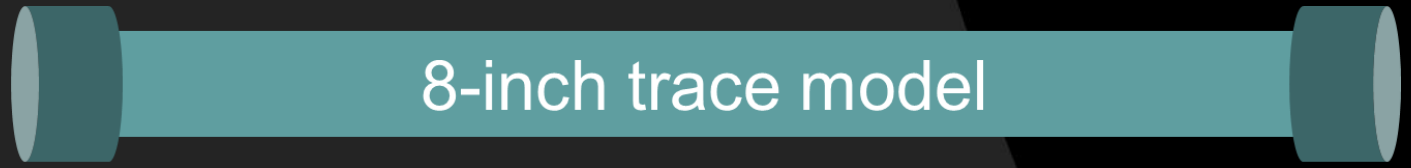


Comparison Shows Impedance change over Trace length

Good TDR can tell you a lot about the interconnect

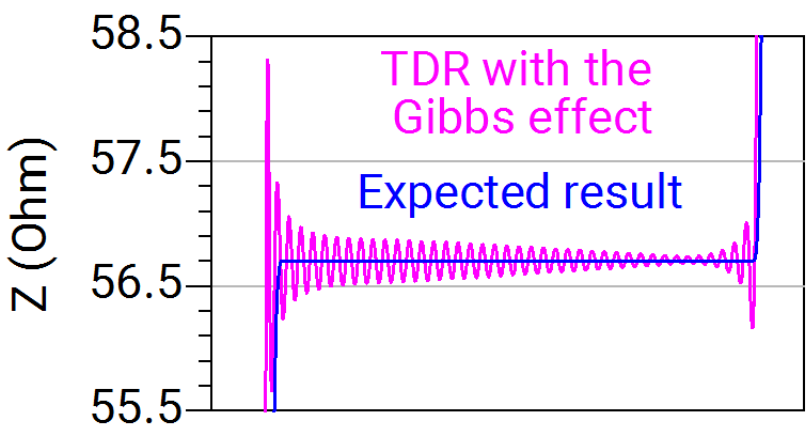


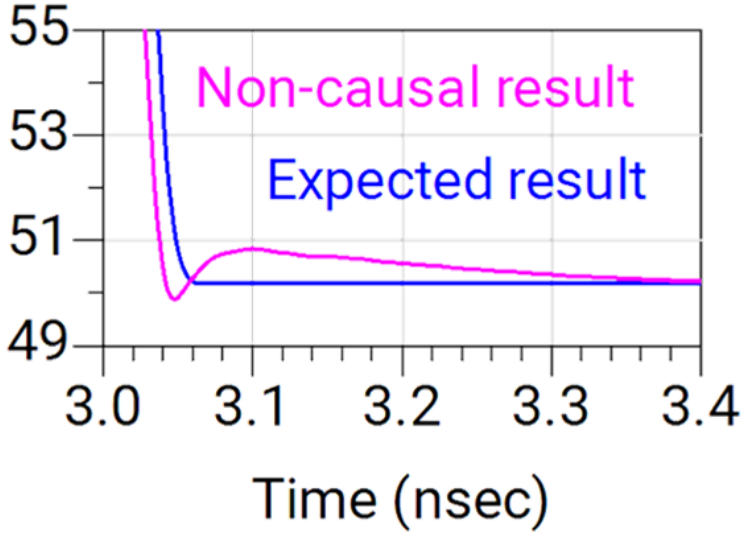
KEYSIGHT

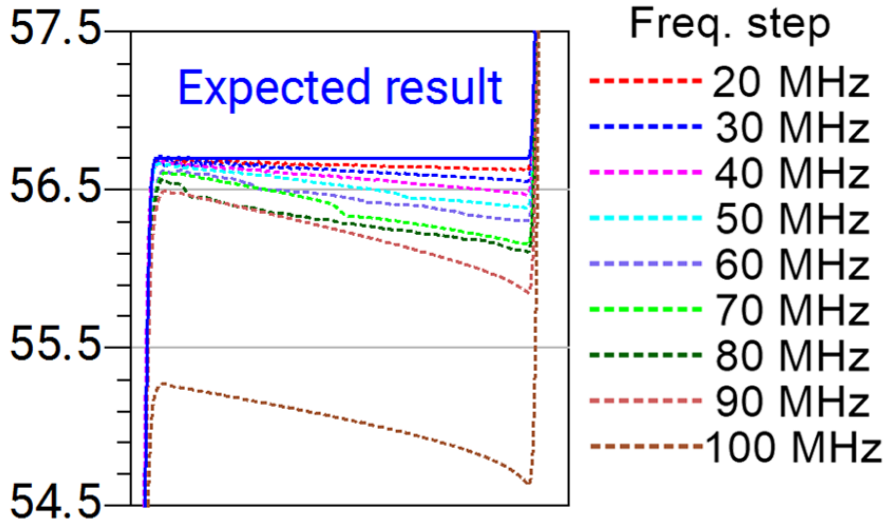


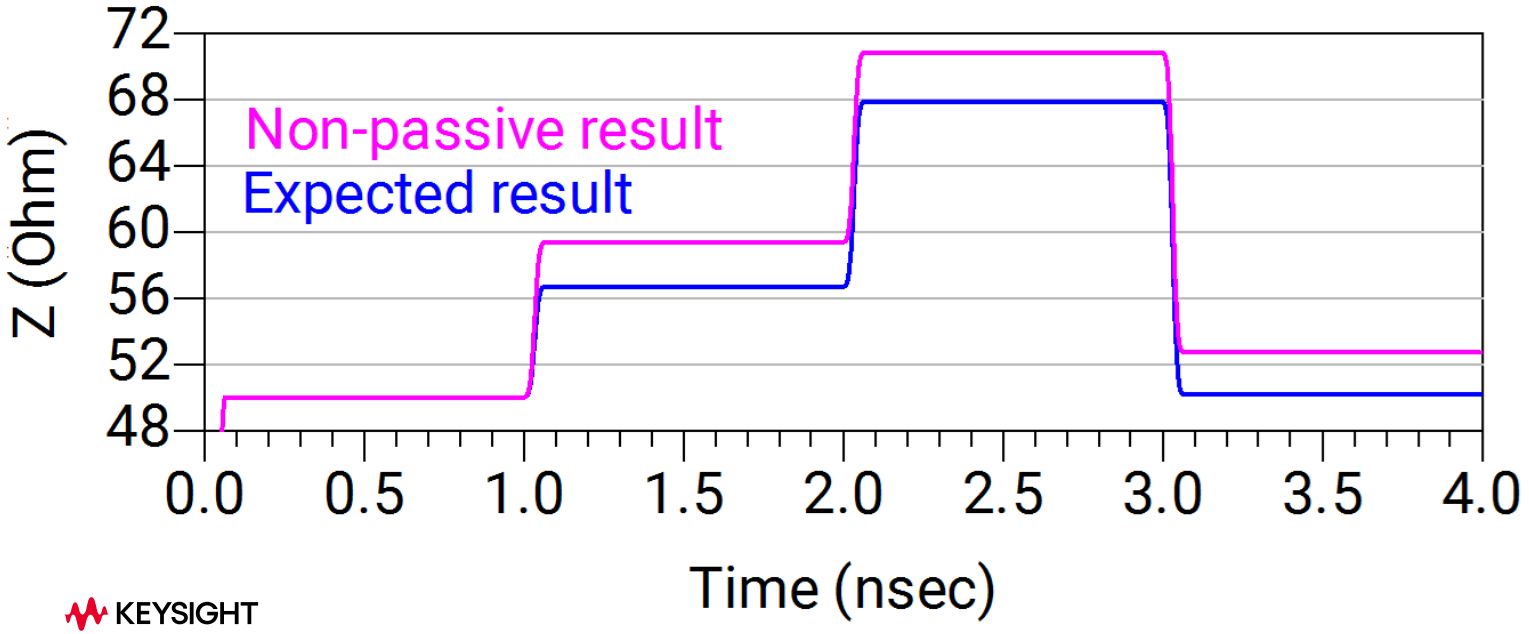
ADS TDR Demo with the measurement and simulation model

What Happens If You Don't Follow the Best Practices





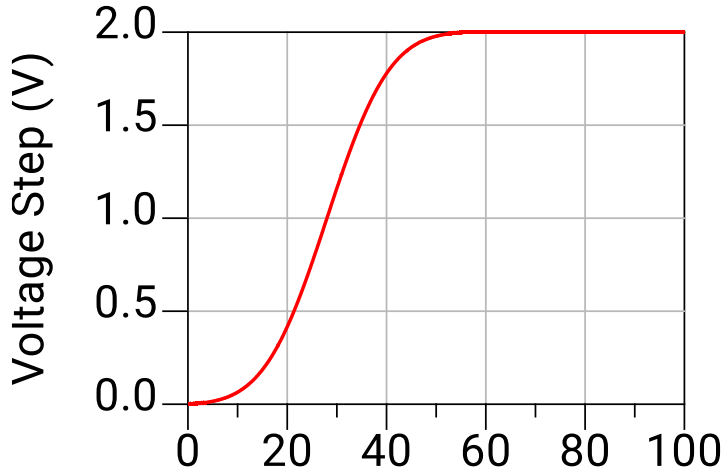




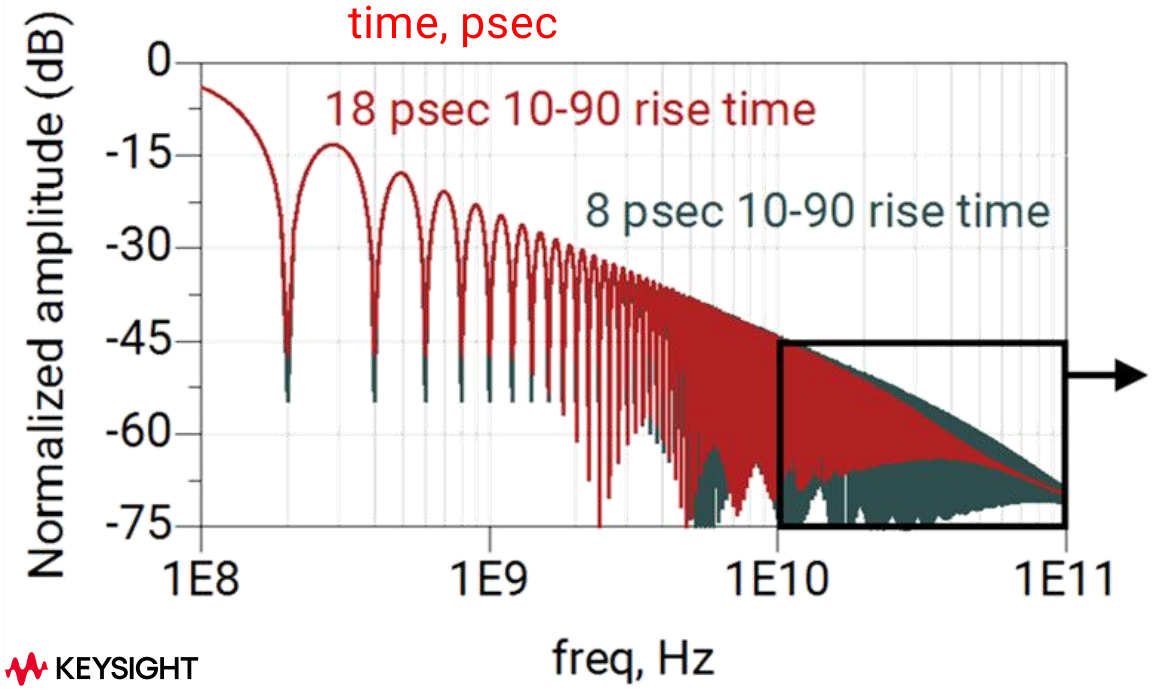
Unsafe TDR can confuse you and give you erroneous results and conclusions.

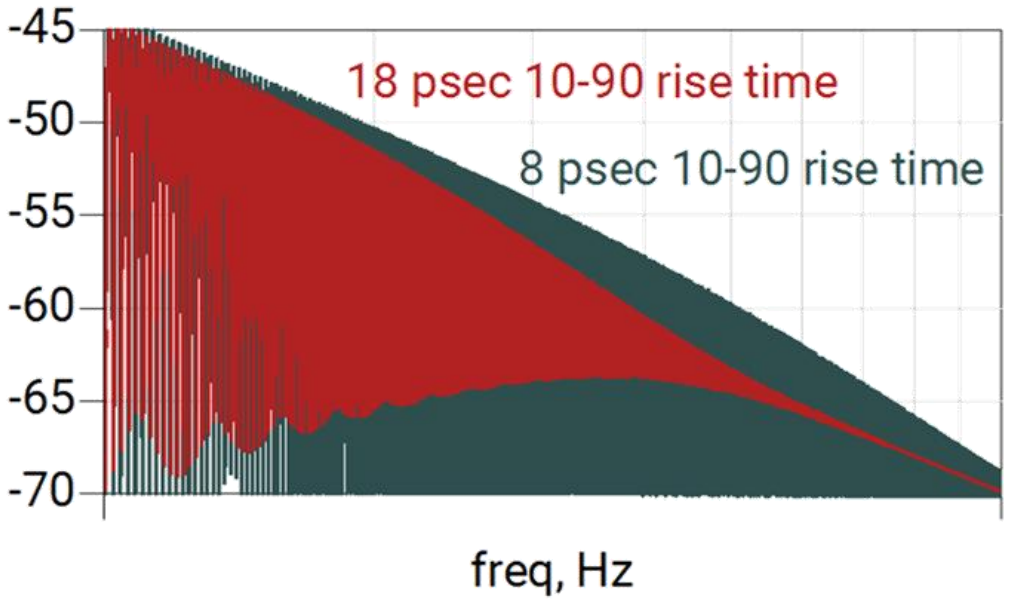
KEYSIGHT

Best Practices for Good TDR Results

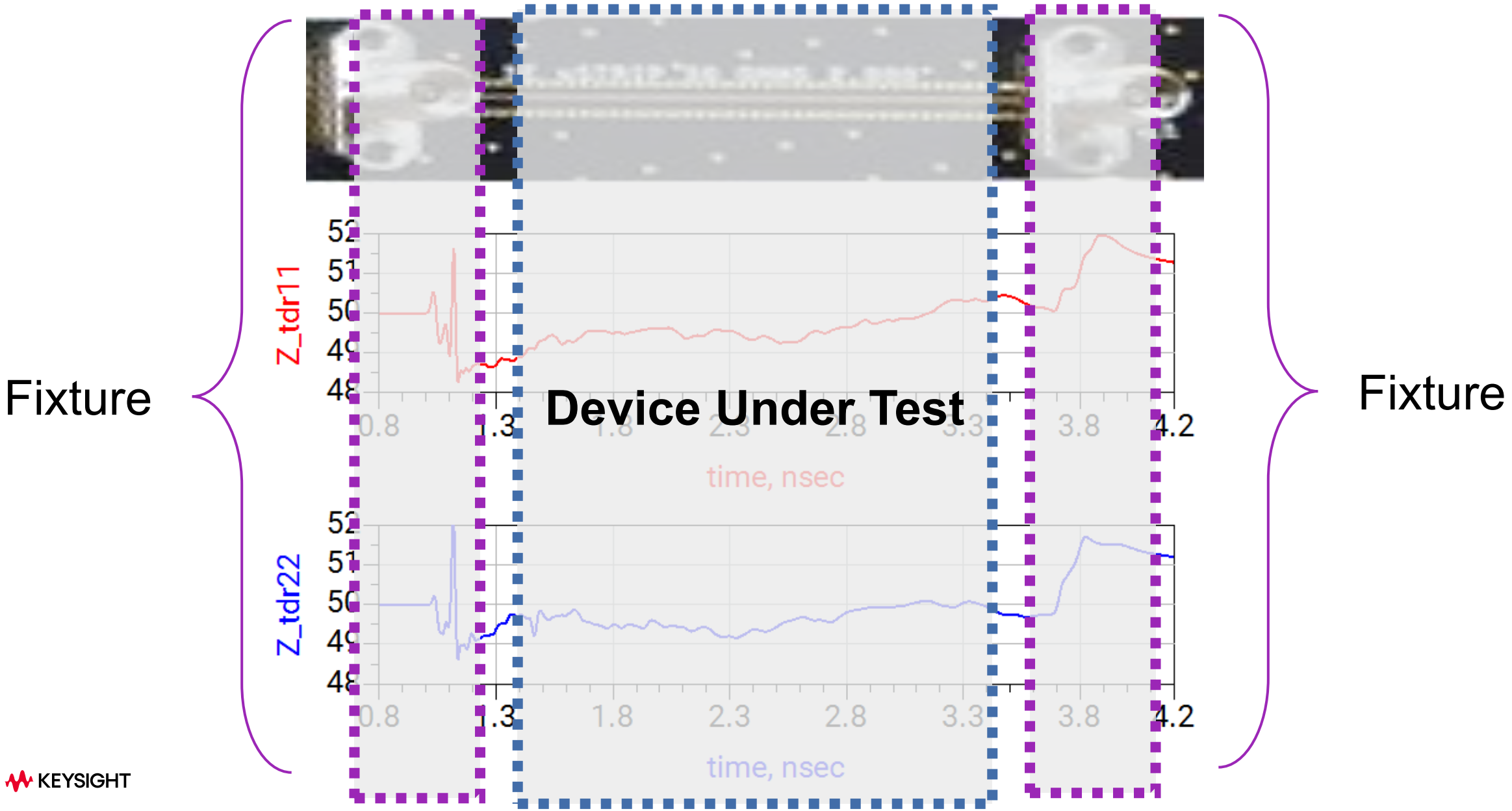


- Use an appropriate step edge
- Match the rise time to the available bandwidth
- Validate S-parameter integrity





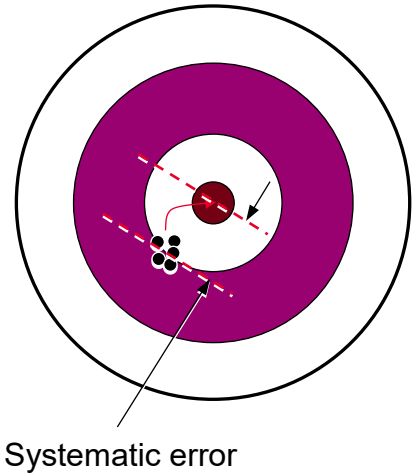
Using De-embedding to Get to the DUT



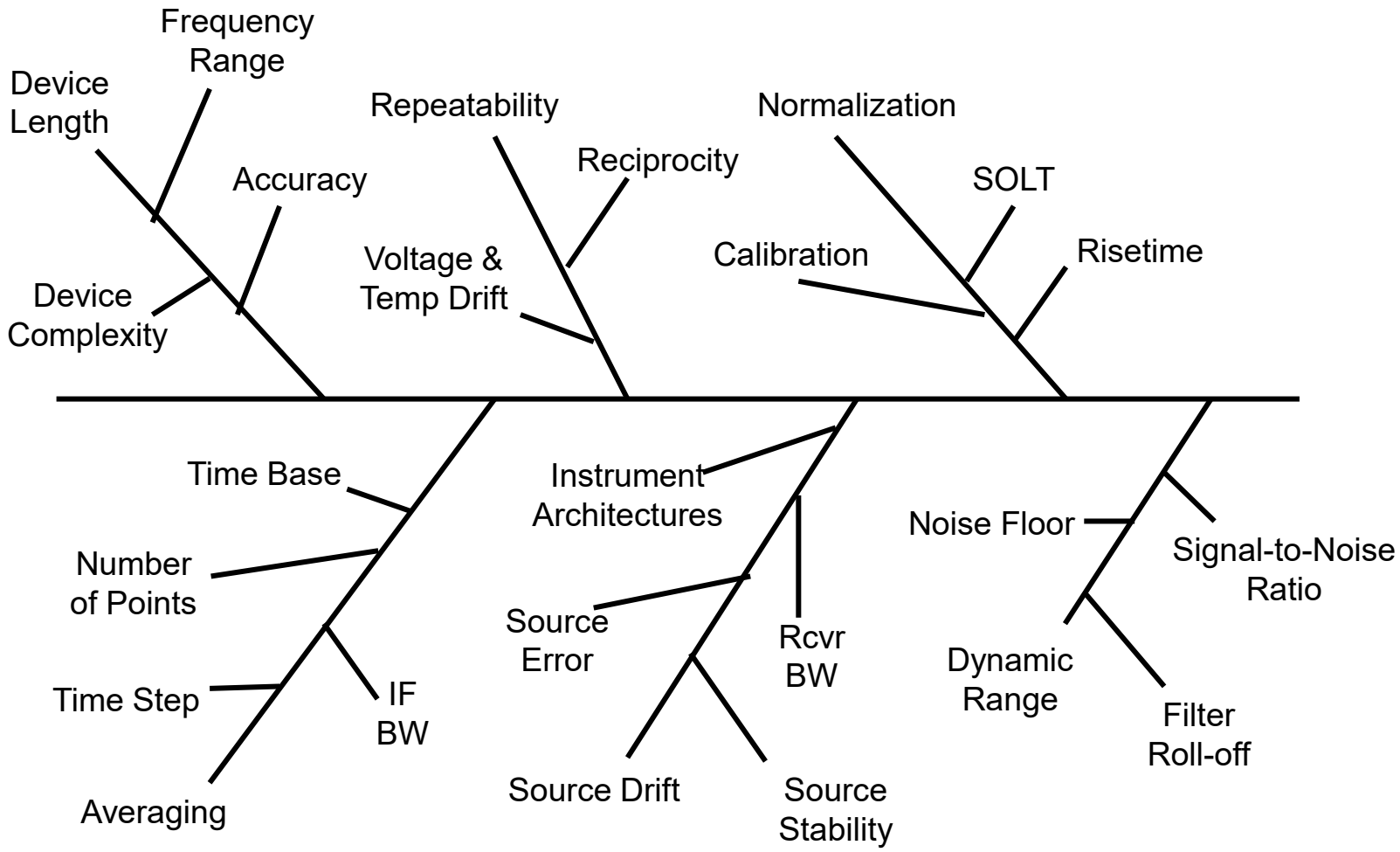
The Need For Calibration

- **Why do we have to calibrate?**
  - It is impossible to make perfect hardware
  - It would be extremely difficult and expensive to make hardware good enough to entirely eliminate the need for error correction

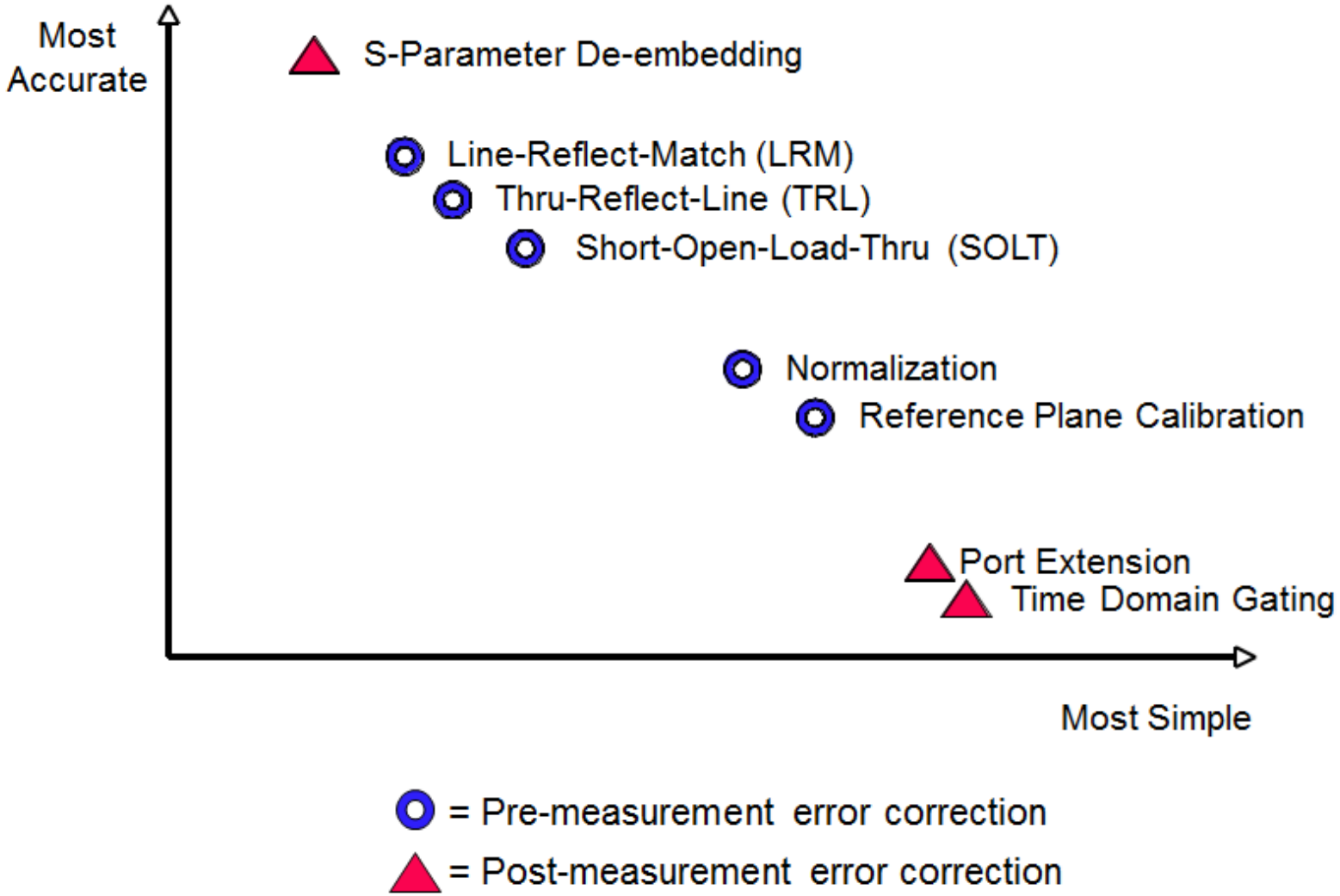
- **How do we get accuracy?**
  - With vector-error-corrected calibration
  - Not the same as the yearly instrument calibration
- **What does calibration do for us?**
  - Removes the largest contributor to measurement uncertainty: systematic errors
  - Provides best picture of true performance of DUT



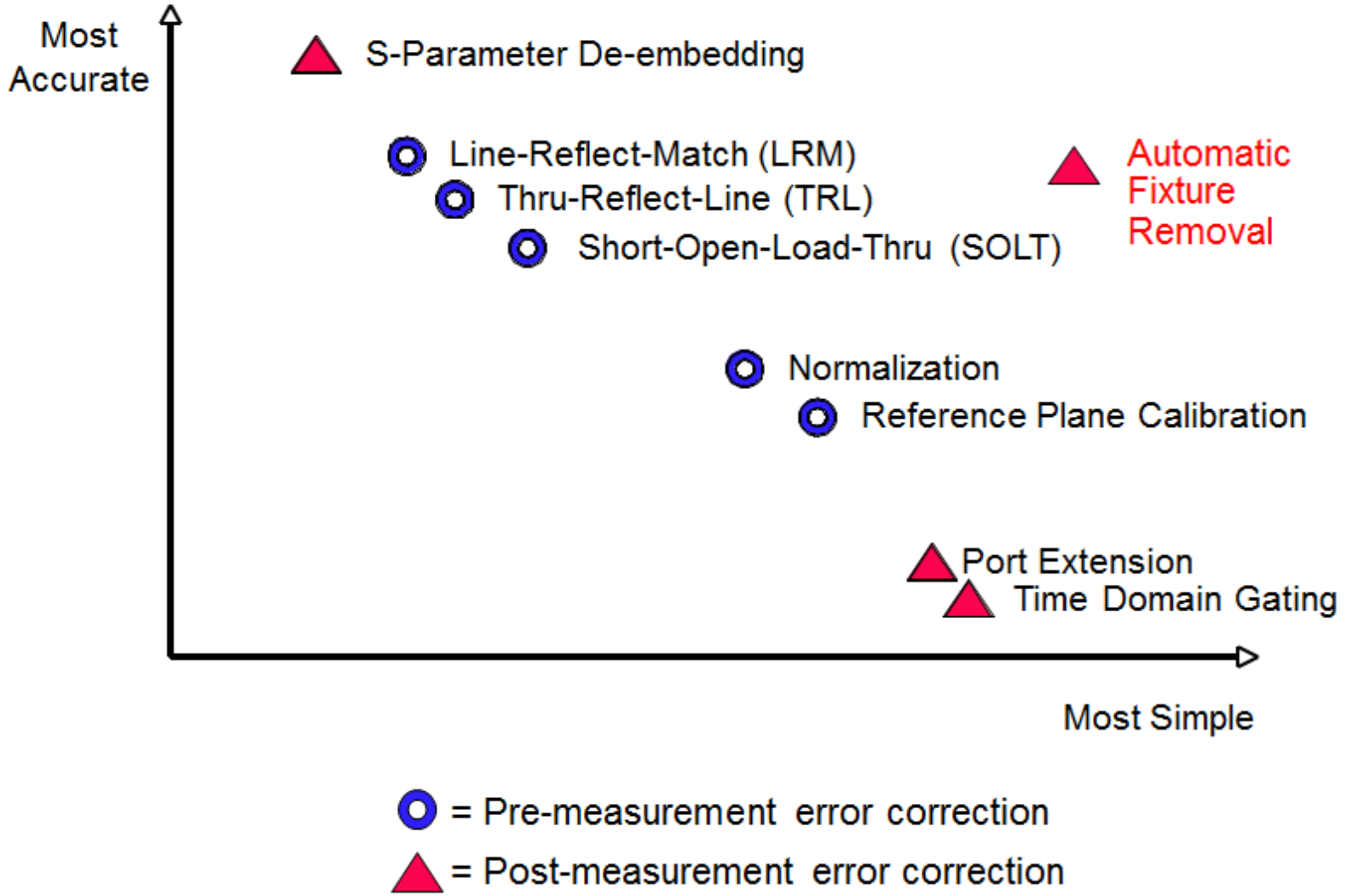
Appreciating the Complexity of it All



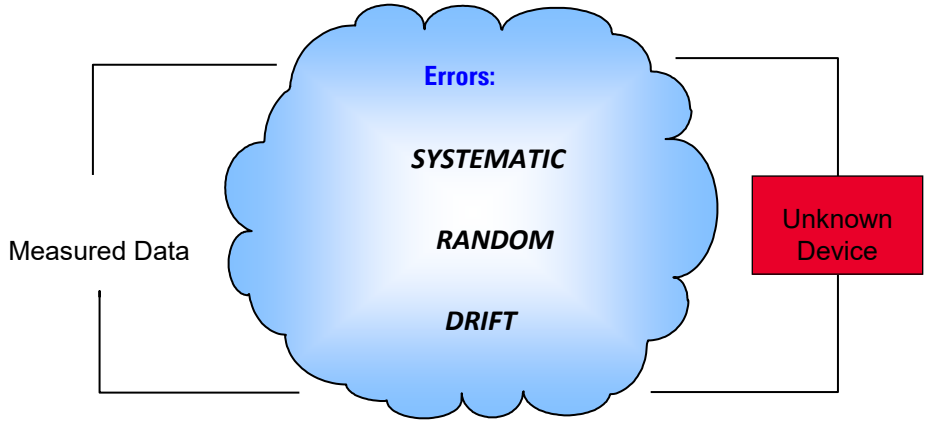
Error Correction Techniques



Error Correction Techniques



Measurement Error Modeling



Systematic errors

- Due to **imperfections** in the analyzer and test setup
- Assumed to be **time invariant** (predictable)
- Generally, are largest sources or error

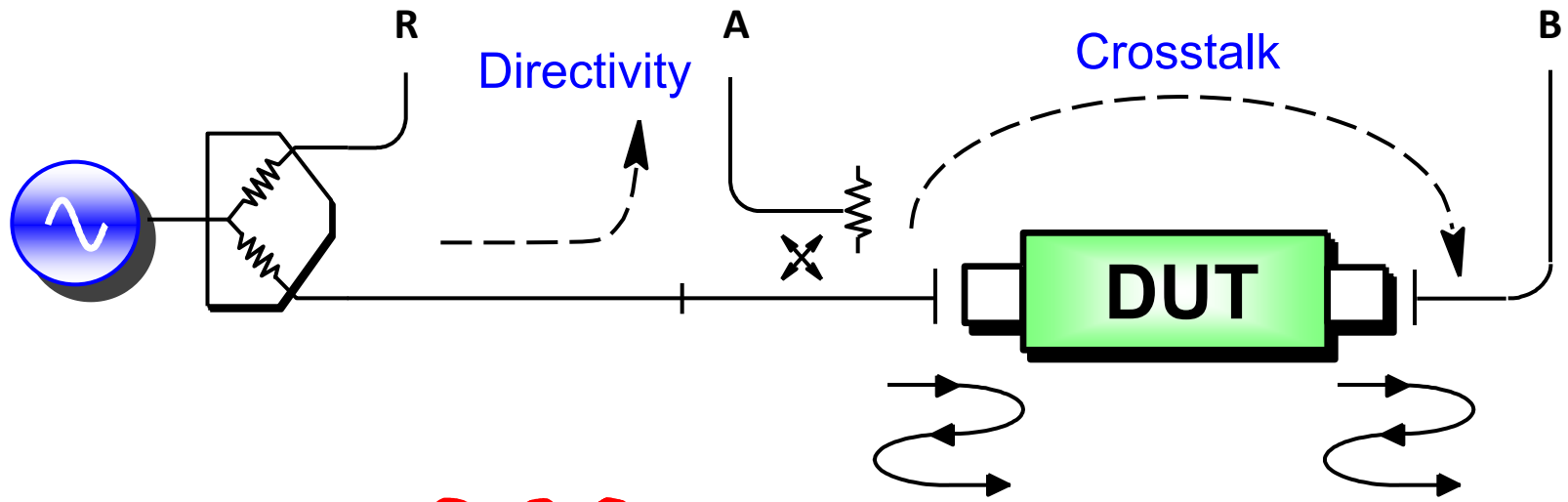
Random errors

- **Vary** with time in random fashion (unpredictable)
- Main contributors: instrument **noise,** switch and connector **repeatability**

Drift errors

- Due to system performance changing ***after*** a calibration has been done
- Primarily caused by **temperature variation**

Systematic Measurement Errors

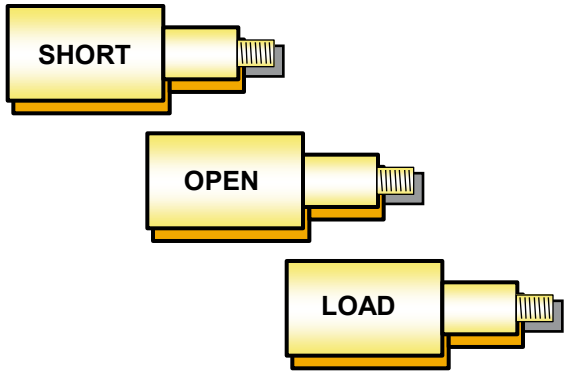


Frequency response

- Reflection tracking (A/R)
- Transmission tracking (B/R)

Six forward and six reverse error terms yields 12 error terms for two-port devices

Calibration Summary



Reflection

	Test Set (cal type) T/R (one-port)	S-parameter (two-port)
Reflection tracking	✓	✓
Directivity	✓	✓
Source match	✓	✓
Load match	✗	✓

Transmission

	Test Set (cal type) T/R (response, isolation)	S-parameter (two-port)
Transmission Tracking	✓	✓
Crosstalk	✓	✓
Source match	(✓*) ✗	✓
Load match	✗	✓

✓ *error can be corrected*

✗ *error cannot be corrected*

✓* *enhanced response cal* corrects for source match during transmission measurements

SOLT Calibration: Mechanical vs. E-Cal Module

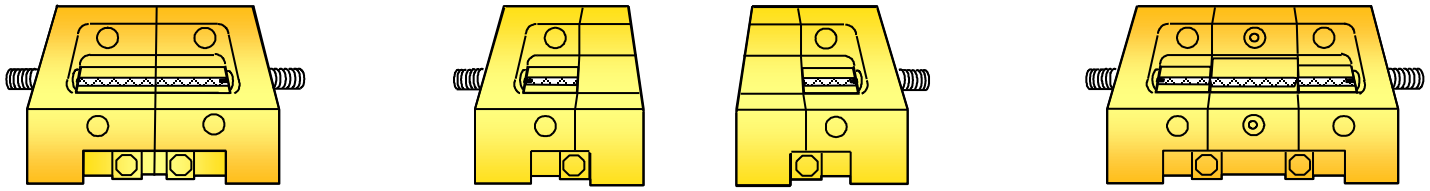
	Advantages	Disadvantages
Electronic Calibration Module	Easy, prevents cable/connector wear and SAVES TIME	Less accurate
Mechanical Calibration Kit	More accurate	Slow and tedious especially for multiport applications

Thru-Reflect-Line (TRL) Calibration

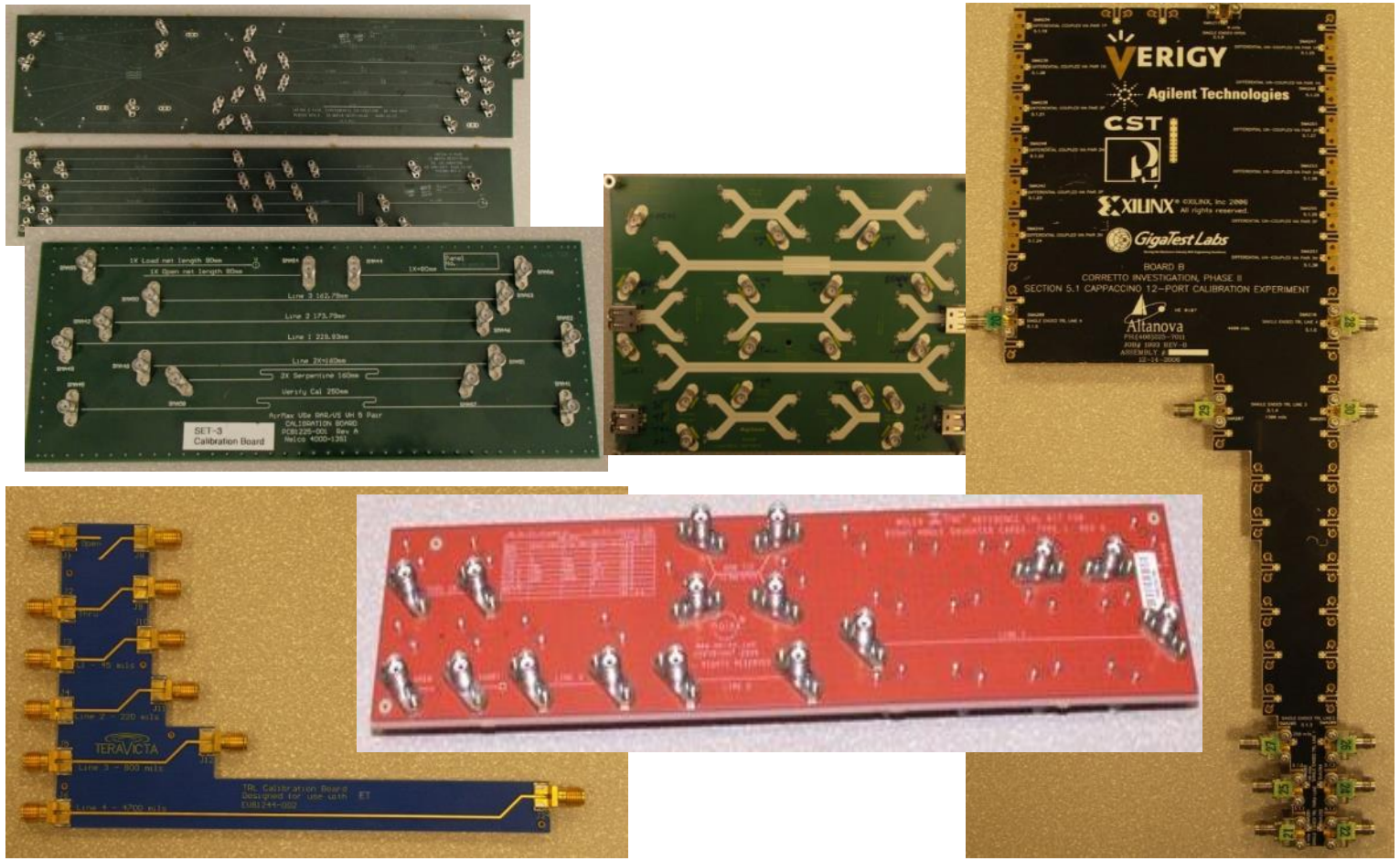
We know about Short-Open-Load-Thru (SOLT) calibration... What is TRL?

- A two-port calibration technique
- Good for non-coaxial environments (PCBs, fixtures, wafer probing)
- Characterizes same 12 systematic errors as the more common SOLT cal
- Uses practical calibration standards that are easily fabricated and characterized
- Other variations: Line-Reflect-Match (LRM), Thru-Reflect-Match (TRM), plus many others

TRL was developed for **non-coaxial microwave** measurements



PCB TRL Calibration Kits (Single Ended)



A good TRL cal kit is difficult to design and fabricate due to launch repeatability, PCB impedance variations, and typical PCB manufacturing tolerances

Comparison Between Calibration and De-embedding

	Calibration	De-embedding
Objective		
Target		
Reference Structures		
Techniques		

Comparison Between Calibration and De-embedding

	Calibration	De-embedding
Objective	Move reference plane	
Target		
Reference Structures		
Techniques		

Comparison Between Calibration and De-embedding

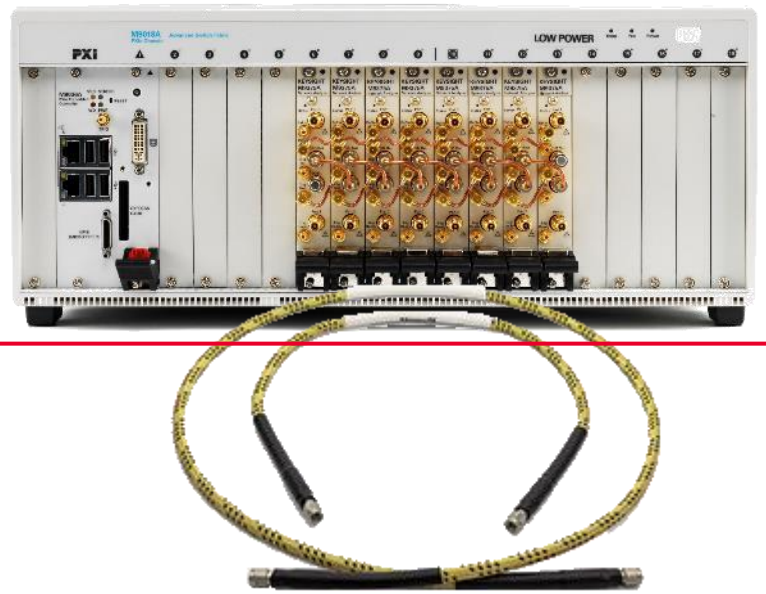
	Calibration	De-embedding
Objective	**Move reference plane**	
Target	Instrument	Measurement
Reference Structures		
Techniques		

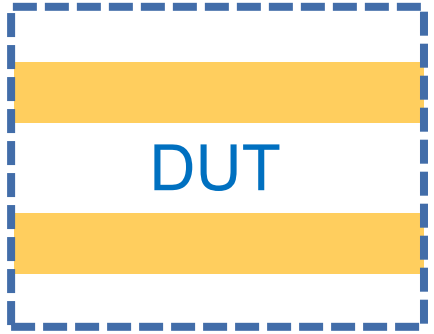
Comparison Between Calibration and De-embedding

	Calibration	De-embedding
Objective	**Move reference plane**	
Target	Instrument	Measurement
Reference Structures	• Short, Open, Load, Thru (SOLT) • Thru, Reflect, Line (TRL) • Thru, Reflect, Match (TRM)	• 2x Thru • 1x Open, 1x Short
Techniques	• Mechanical Calibration • Electronic Calibration	• Automatic Fixture Removal • Measurement-based Model

Measurement Setup and Default Reference Plane

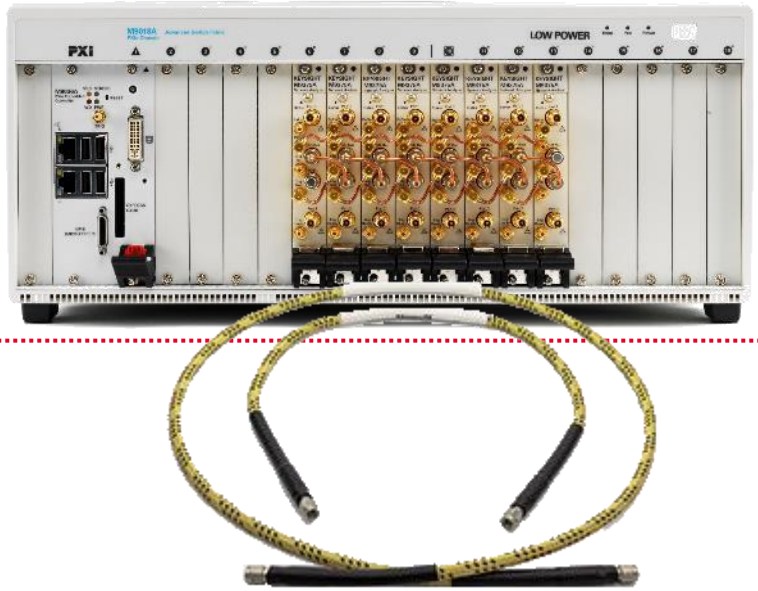
Reference Plane



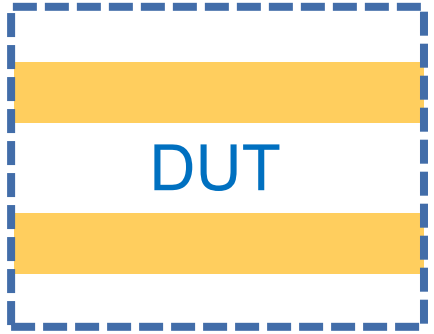


Calibration Moves the Instrument Reference Plane

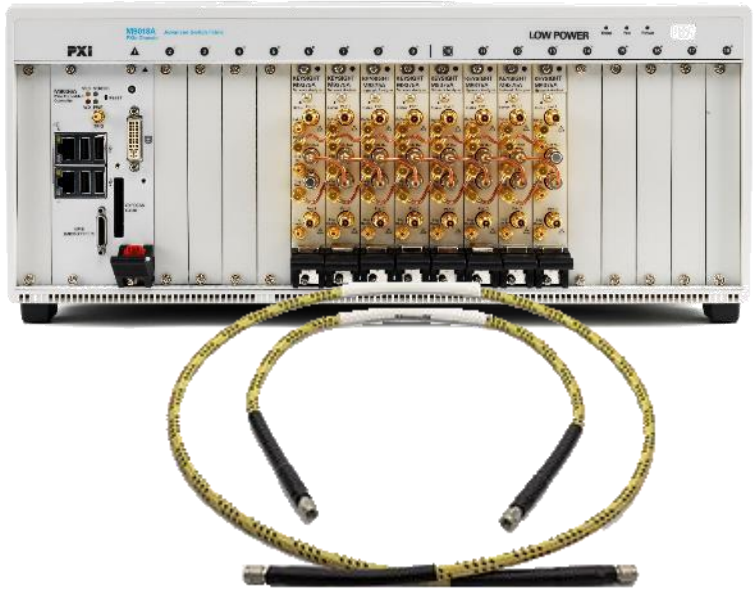
Calibration



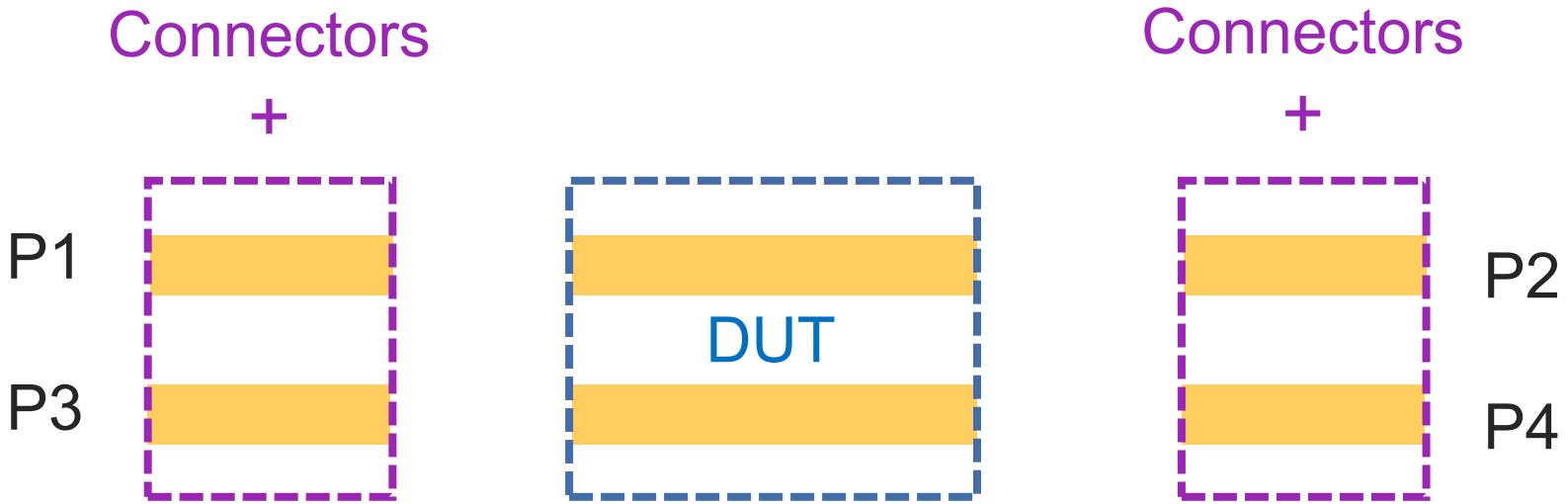
Reference Plane



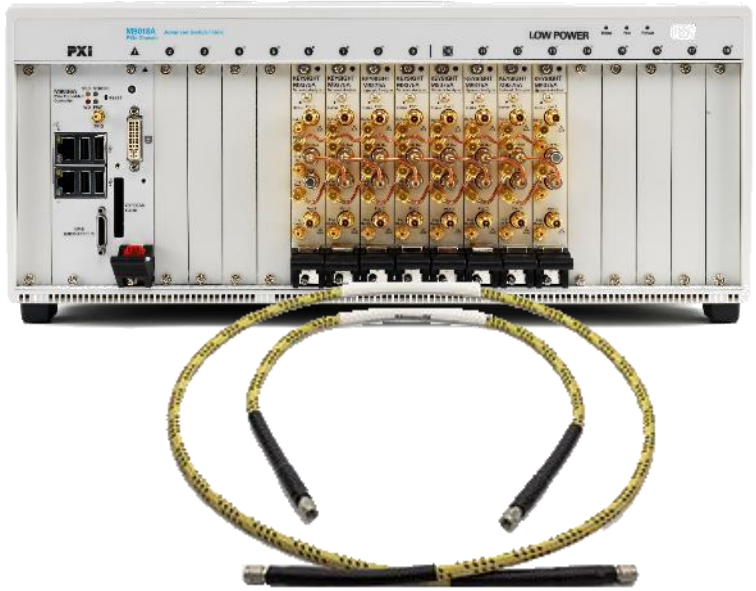
Measure Device Under Test Through Fixtures



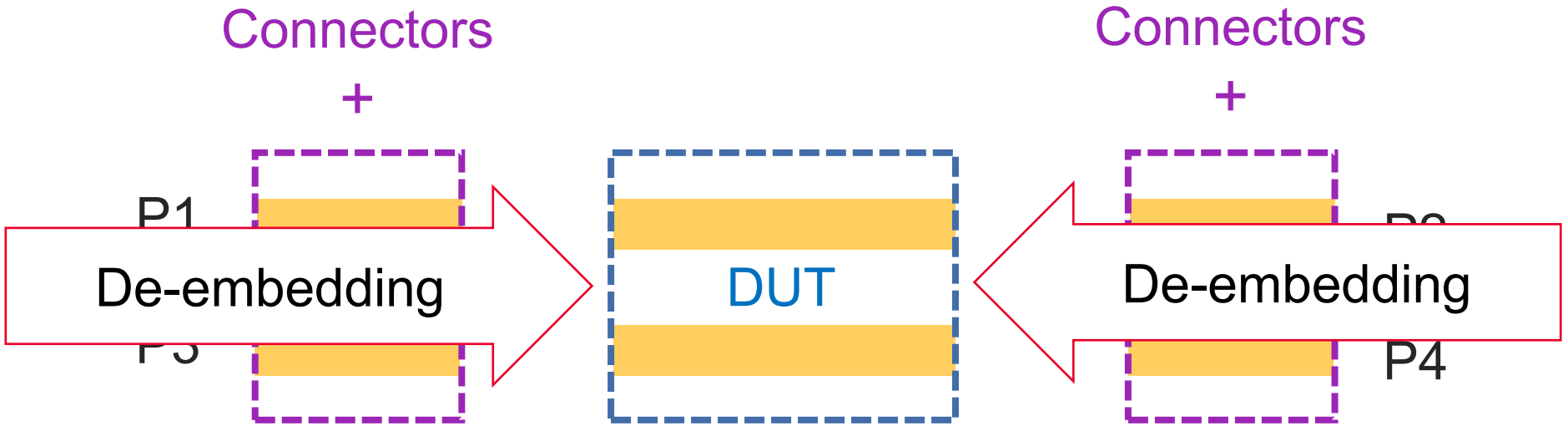
Reference Plane



De-embedding Moves the Measurement Reference Plane



Reference Plane

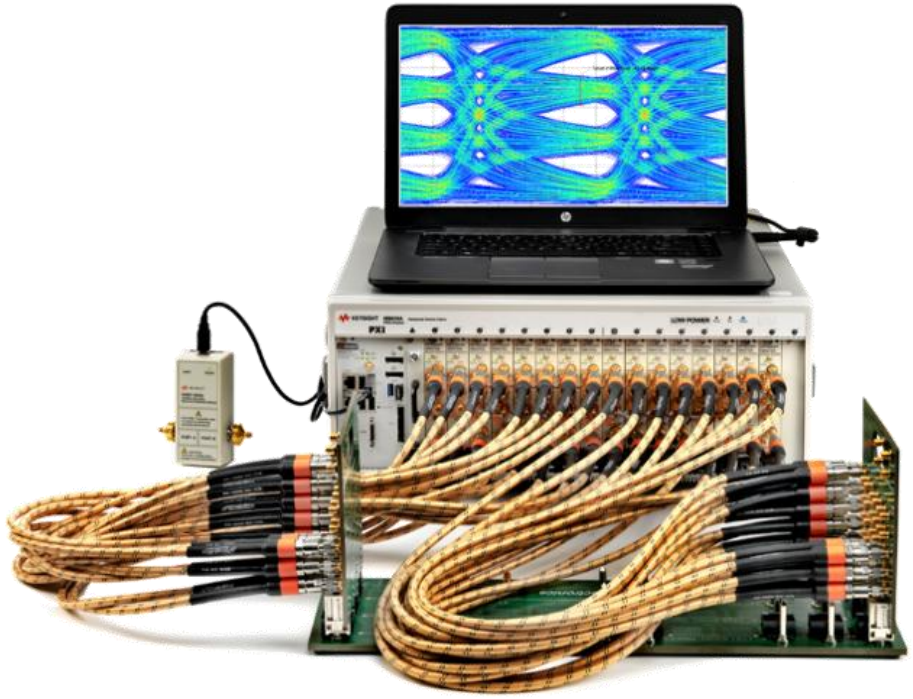


A Day in the Life of an SI Engineer…What Now??

- Determine VNA testing requirements
  - Frequency Range?
  - Number of Ports?
- Active or Passive device test?
- Probing system or fixturing?
- Accessories and specialist software tools? (aka…here are some really cool PLTS features that allow you to play with data…)

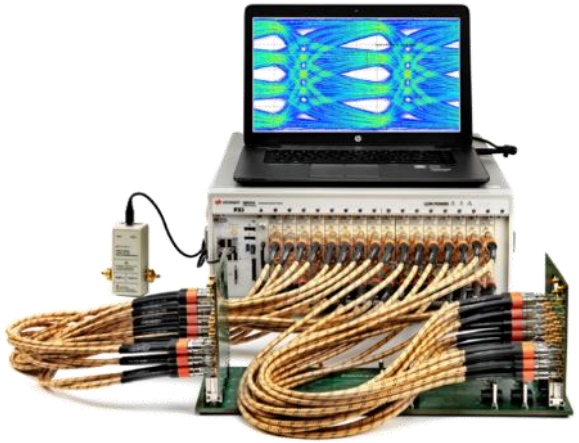
Frequency Range and Number of Ports Needed?

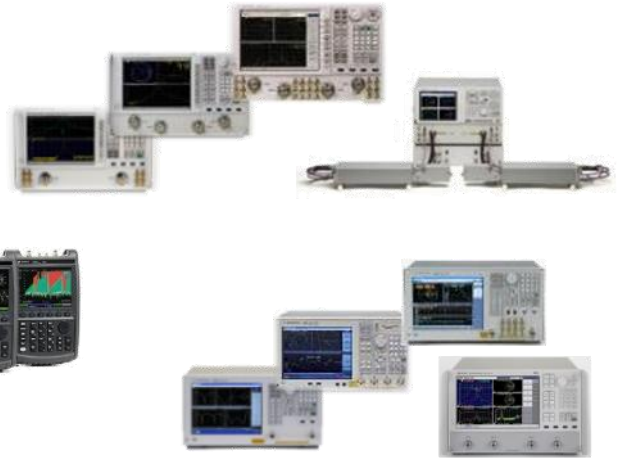
4-port 120GHz PNA+PLTS System



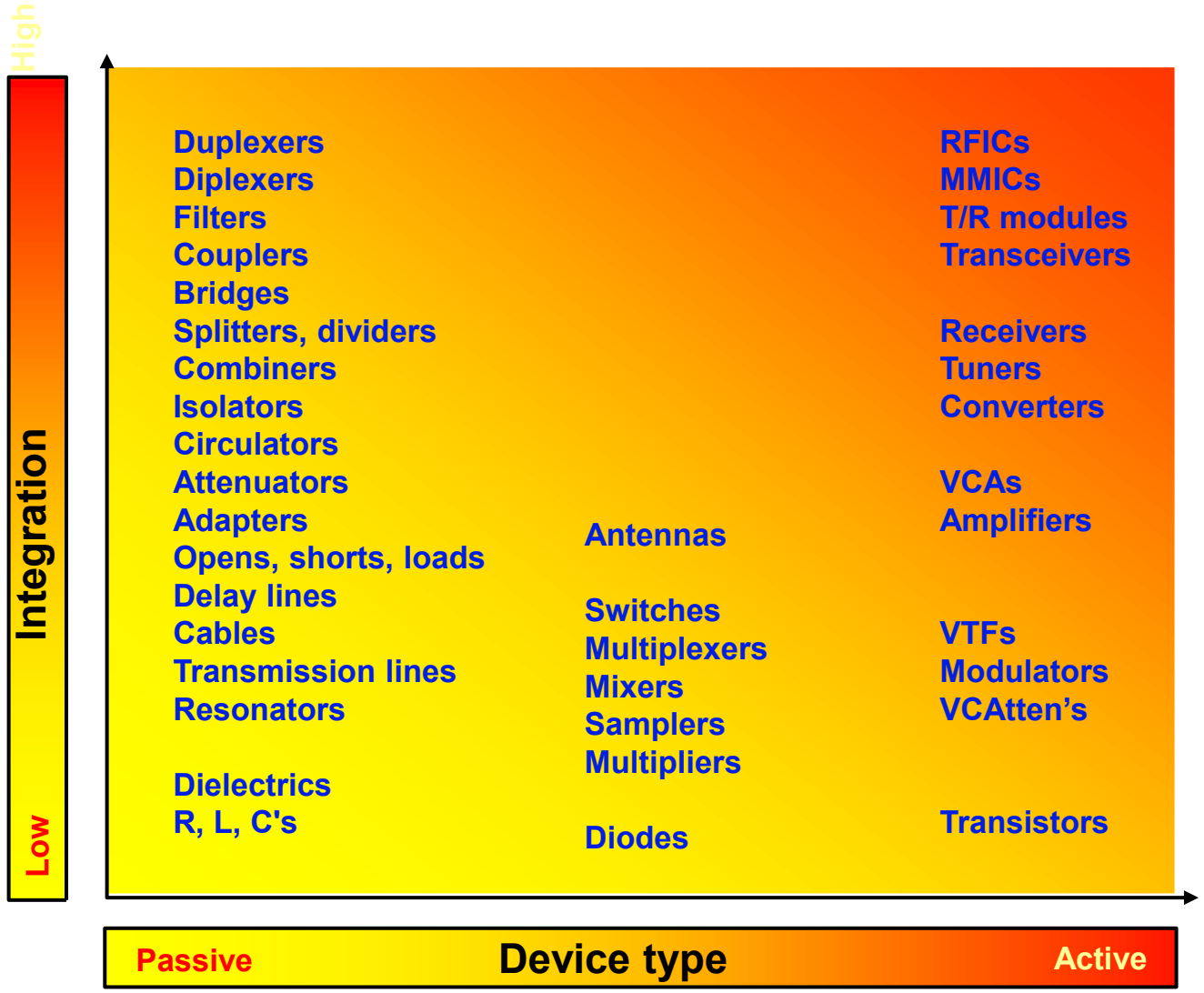
32-port 26.5GHz PXI-based PNA+PLTS System

Frequency Range and Number of Ports Needed?

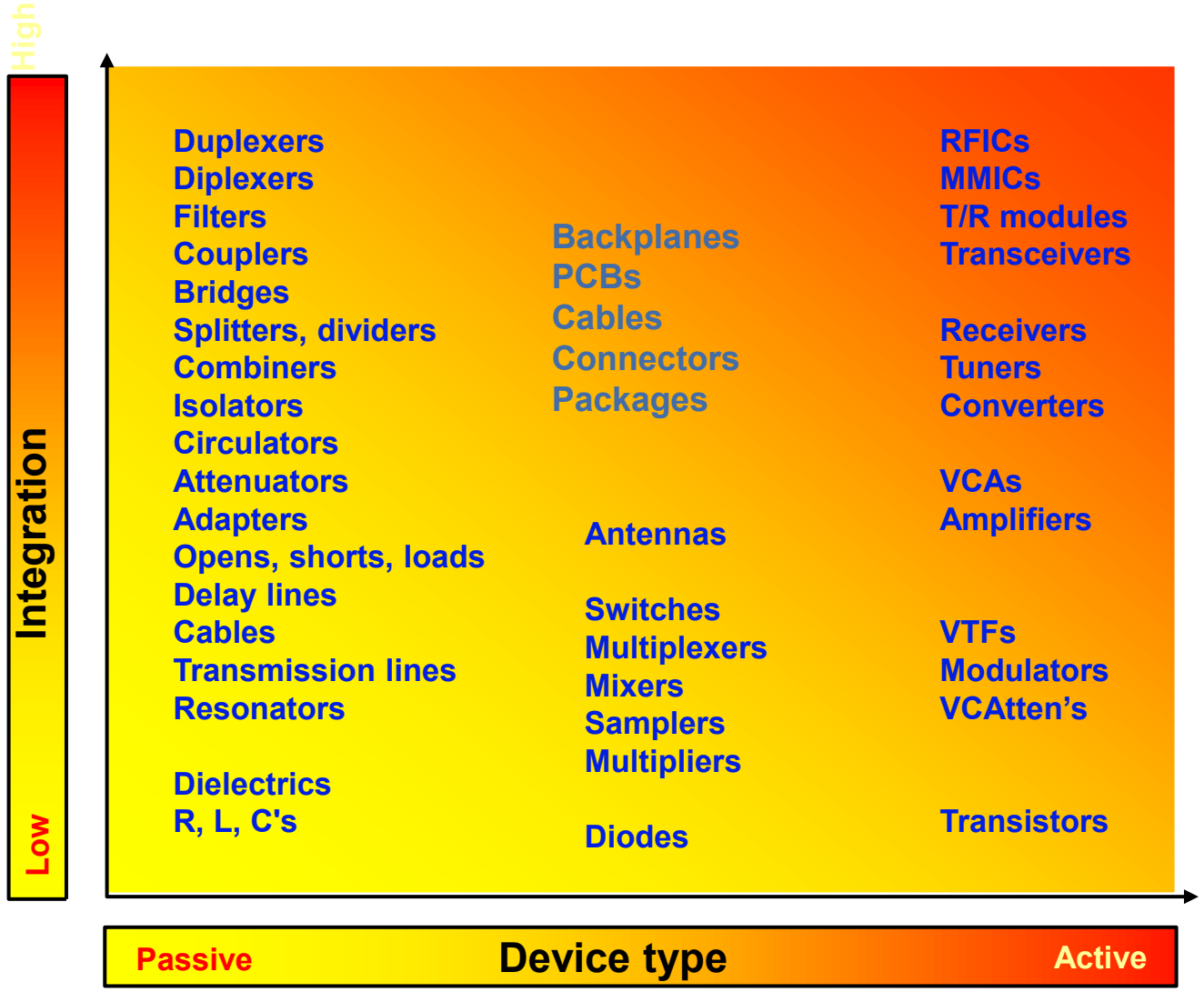




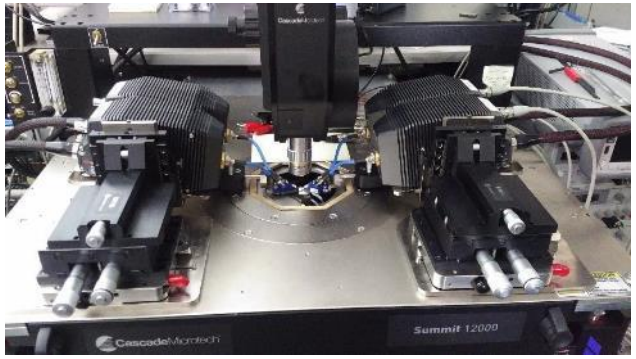
Active or Passive Device Test?

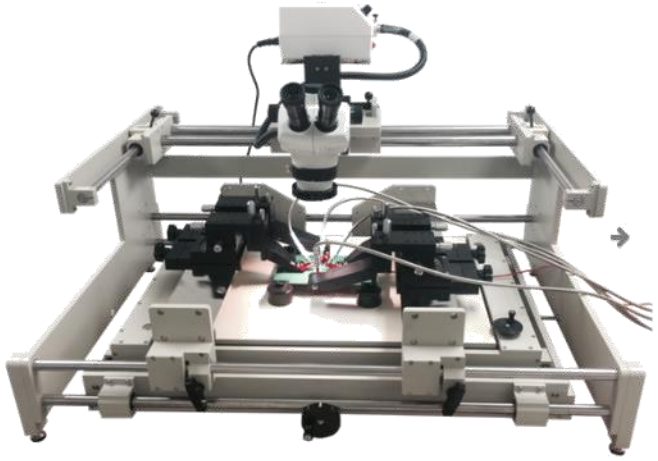


Active or Passive Device Test?



Probing or Fixturing?

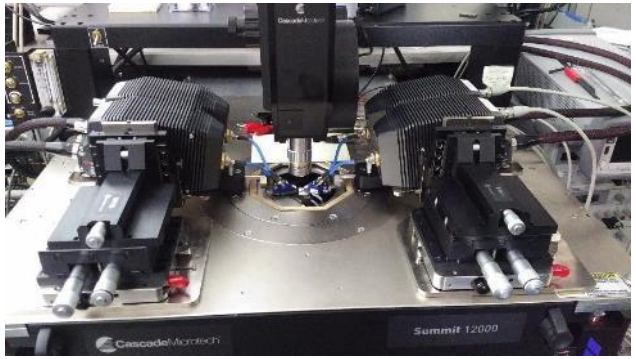




Probing

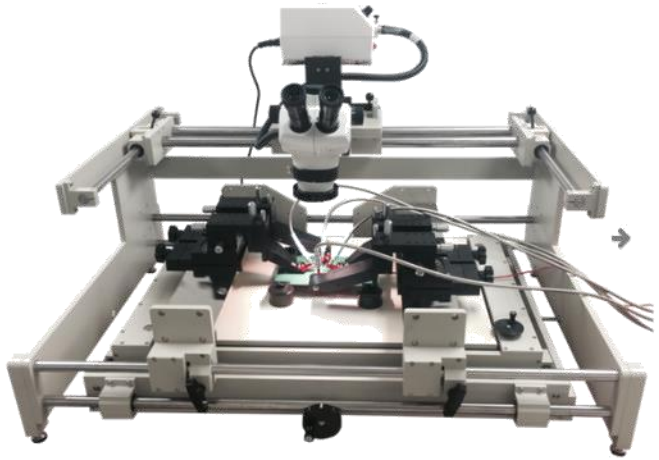
- Advantage
- Flexibility
- Disadvantage
- Expensive
- Need probe cal kit and models for probe calibration

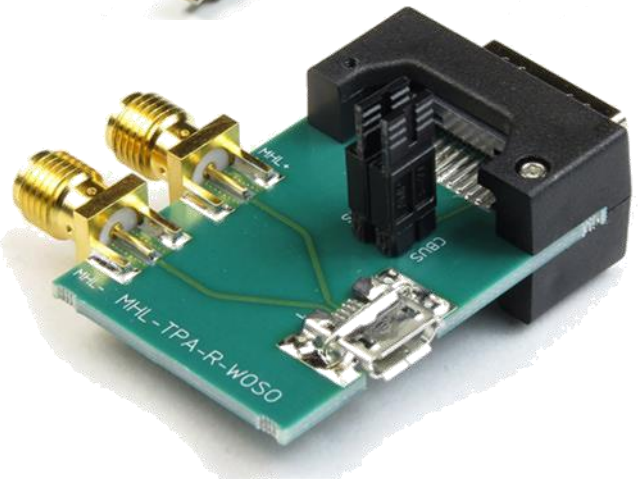
Probing or Fixturing?



Probing

- Advantage
- Flexibility
- Disadvantage
- Expensive
- Need probe cal kit and models for probe calibration





Fixtures

- Advantage
- Easy to Use
- Disadvantage
- Each application requires different fixture
- Not electrically transparent, they have mismatch, loss and delay that must be characterized and removed from the DUT measurement (de-embed)

Accessories and Specialist Software Tools?

- Switches
- Attenuators
- Amplifier

Core

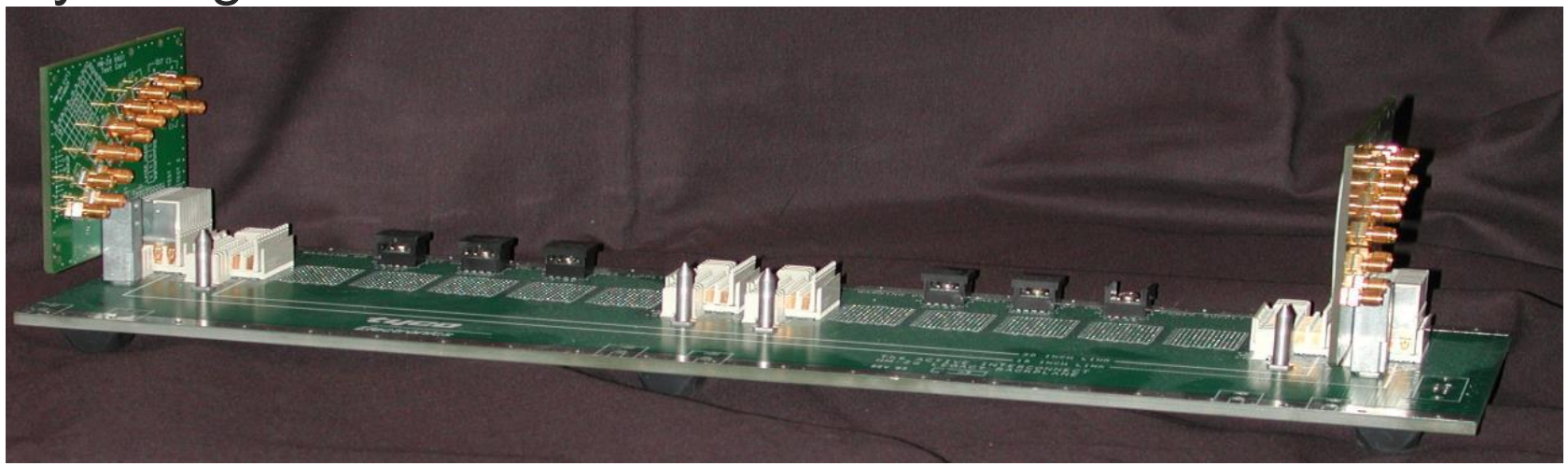
- Adapters &Connectors
- Attenuator/Switch Driver
- DC Block
- Detector
- Directional Bridge
- Directional Coupler
- Frequency Meter
- Power Divider
- Power Limiter
- Power Splitter
- RF Probes
- Noise Source

PLTS 2018

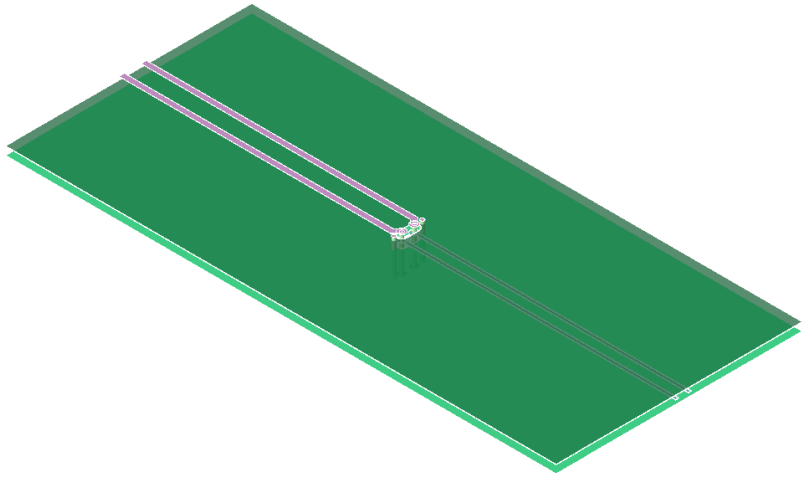
- Sub-millimeter spatial resolution for micro-structure characterization (6ps)
- Python applications programming interface for factory automation
- 64-port Automatic Fixture Removal (AFR) for powerful multiport analysis

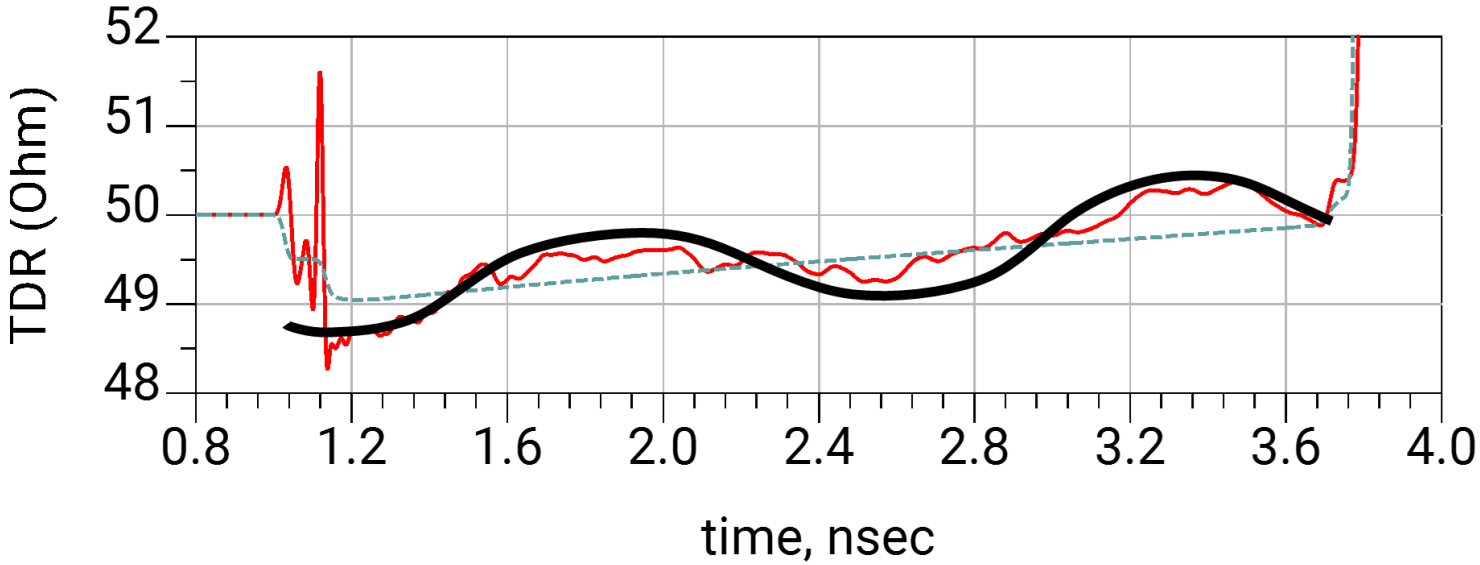
Analyze Channel Performance

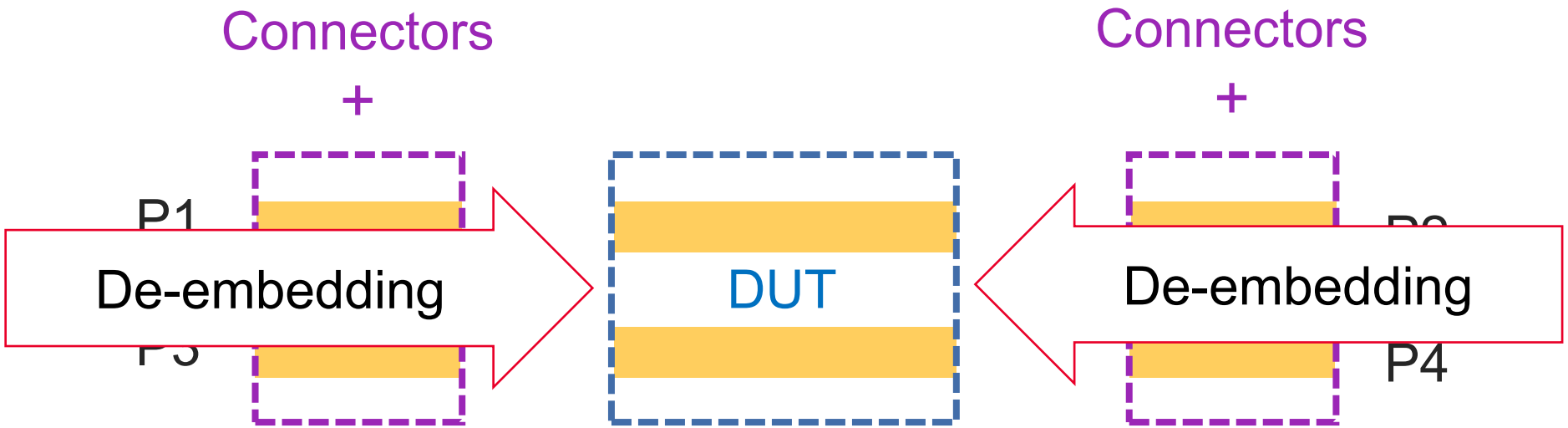
- New Figures of Merit are creating measurement challenges
- Along with more powerful metrics comes testing complexity
- Software tools can minimize the learning curve
- Examples
  - Channel Operating Margin (COM)
  - PAM4 eye diagram



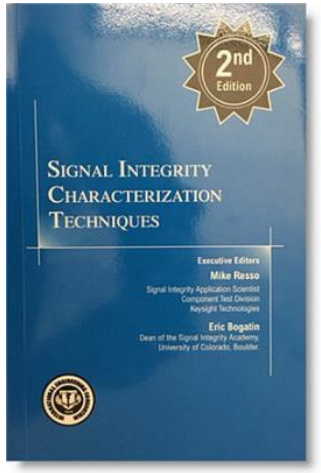
TDR simulation and measurement Workflow is Useful



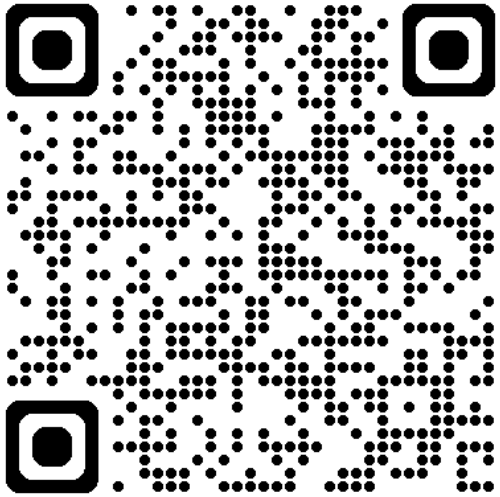


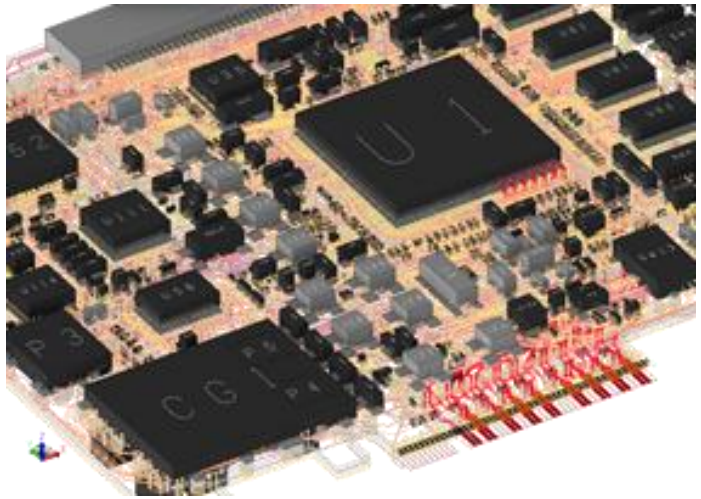


Resources



- Physical Layer Test System Home: www.keysight.com/find/plts
- Digital Interconnect Test System: www.keysight.com/find/diref
- Free Signal Integrity Book: www.keysight.com/find/RessoBook





Signal Integrity Hands-on Workshop:
https://keysight.com/find/ads-si-workshop

Download Latest ADS:
www.keysight.com/find/eesof-ads-latest-downloads

ADS Free Trial:
https://www.keysight.com/find/mytrial.si.web