APPLICATION NOTE

Design of Transmon Qubit and CPW Resonator in Flip-Chip Technology with ADS, Quantum Pro

KEYSIGHT

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Introduction

Scaling up the number of superconducting qubits on a chip results in routing problems. To ease the routing and make the best use of the available chip area, going to the third dimension is a viable option. Among different methods, flip-chip technology is a promising 3D integration technique for many superconducting qubits. This adds flexibility in design, routing, and planning of the signal paths to reduce the cross talk. Here we review how a coplanar waveguide (CPW) transmission line can be designed in a generic quantum multilayer (**Flip-Chip)** technology using the **Controlled Impedance Line Designer (CILD)** in Keysight ADS. The main characteristics of CPW e.g., characteristics impedance, capacitance and inductance per unit length, effective dielectric constant, loss, among others are calculated. The CPW line can be utilized as a qubit readout resonator, feedline, Purcell filter, or quantum bus to directly couple the qubits. We demonstrate how a transmon qubit layout in flip-chip technology can be designed and simulated. The technology used in this application is based on a metal layer (e.g., Aluminum. Niobium) deposited on a semiconductor layer (e.g., Silicon, Sapphire). Additional layers include airbridges, vias for airbridges, and air under airbridges and air between the two chips. For example, if airbridges on each chip are 5 µm tall, and the air between the chips is 2 µm thick, then the ground planes of both chips are 2+ 5 + 5 = 12 µm apart.

The properties of the CPW resonator in flip-chip technology depend on if the resonator is facing the opposite silicon layer or the metal layer. This will be discussed in this application note. For designing CPW resonators in a single-layer quantum technology please refer to the application note, Calculation of CPW Resonator Properties Using the Quantum Technology File | Keysight.

Setting Up the Flip-Chip Technology File

After executing Keysight ADS and creating a new workspace in your preferred path, you are asked to select the technology for the library of workspace. Figure 1 shows the list of available technologies in ADS 2025 from which you choose **Quantum Multi-Layer Technology** shown by the red box.

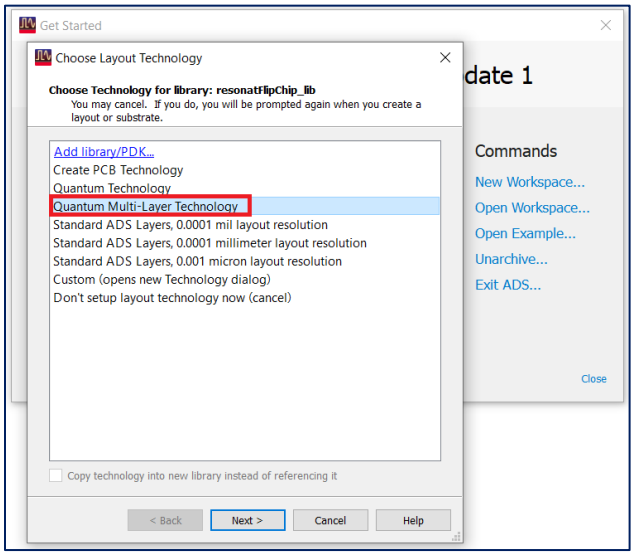


Figure 1. Choosing **quantum multi-layer technology** for library after creating a workspace in ADS 2025.

In ADS 2026, the **Choose Layout Technology** panel is slightly different. In this version, instead of two quantum technologies, you have **Quantum Technology Library**. By selecting this and clicking **Next** you see a new list with three options: **Single-layer**, **Multi-Layer**, and **Coaxmon**. Select **Multi-Layer** and click **Next**. After this, the layer set-up windows in ADS 2025 and ADS 2026 look the same. Now you are asked to determine the number of layer sets (stacks) for the technology as shown in Figure 2. Here we choose 2 for the flip-chip technology. Pressing **Next** takes you to another page to set up the **layer set 1 of 2** (which is the same as defining the layer properties of a single chip technology) as shown in Figure 3(a). Note that at this point you can change the layer thicknesses. For examples of this application note we change the height (or thickness) of dielectric substrate from 250 µm to 280 µm. The Airbridge dielectric (air) is 1 µm and the thickness of all metal layers is changed from 200 nm to 0 nm to assume a perfect conductor. The thickness (height) of air between the two chips (**called Top Dielectric**) is 6 µm. Press **Next** to get to the next window to set up the properties of the **layer set 2 of 2** as shown in Figure 3(b). Here you can change the thickness to the ones shown in the figure. Also, at the very bottom you can click (**Flip the layer set upside down**) to flip the top chip (Stack 2).

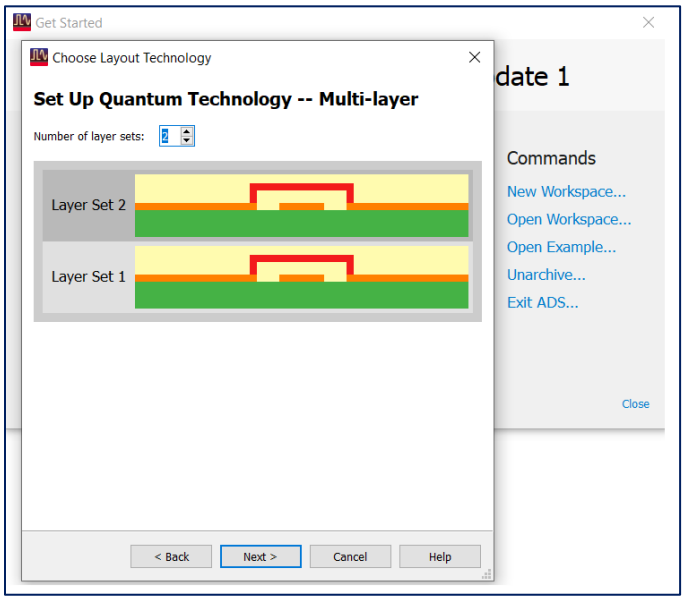


Figure 2. Setting up the number of stacks for the multi-layer technology. Here we select 2 for flip-chip technology.

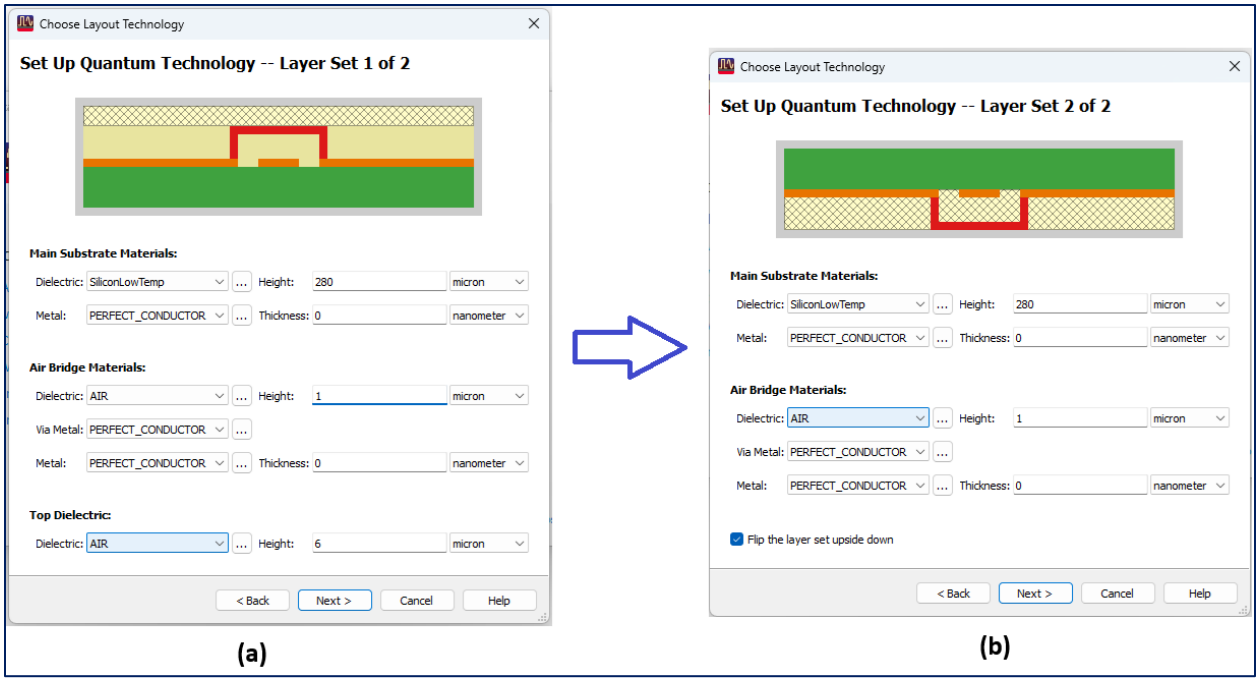


Figure 3. The menu to set up the layer materials and thicknesses. (a) Layer set 1 of 2, (b) Layer set 2 of 2. For this layer, click the (**Flip the layer set upside down**) to flip the top chip.

Pressing **Next** one more time takes you to the next set up page to define the parameters of vias (which makes the connection of signal paths of two chips possible). See Figure 4. After this the **tech:subst** icon appears under the path of your workspace in the main Keysight ADS window. By clicking on the **tech:subst** icon, the **tech** window appears. In this window you see the **Stack up** of the layers as already explained in Calculation of CPW Resonator Properties Using the Quantum Technology File | Keysight.

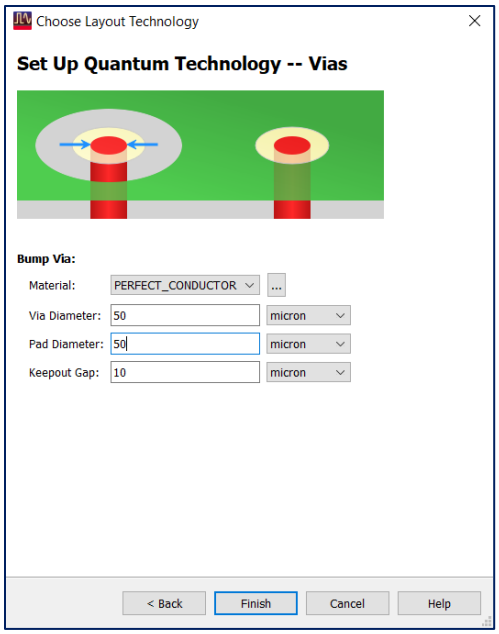


Figure 4. Filling the parameters for Vias and pressing **Finish** is the last step in setting up the flip-chip technology.

Controlled Impedance Line Designer (CILD)

In this section we explain CILD and show how the CPW is designed for flip-chip technology. If you have not yet worked with single-layer quantum technology and are not familiar with **Stackup** and using **CILD**, please study this application note first, Calculation of CPW Resonator Properties Using the Quantum Technology File | Keysight.

After clicking on the **tech:subst** icon, the **tech** window appears. In this window you see the **Stack up** of the layers. By clicking on the CILD icon (the icon with **Z=50** on it) on the top menu in **tech** window, a new CILD window appears as shown in Figure 5. We are going to design a single ended (not differential or edge coupled) CPW with 50 Ohm impedance using the main perfect conductor (metal) layer on silicon substrate. On the left side of the CILD panel, select the **Type** to be **Coplanar Single-Ended**. Afterwards the default layer names appear on the three selectable lines under the **Type** bar. Now you can change them to make the CPW that you want in flip-chip technology. There are two options when a CPW line is designed in the-chip technology: (A) a CPW facing a metal layer on top and (B) a CPW facing silicon (dielectric) substrate layer on top.

Type A: a CPW facing a metal layer on top:

For this type, change the **Top Plane** to **2_cond**, **Signal** to **cond**, and **Bottom Plane** to **<None>**. See the blue colored box at the bottom of Figure 5. The CPW is formed on the first silicon substrate (see the yellow-colored cross sections in Figure 5). You can press the **ViewAll** icon on the top left corner of the screen to enlarge the cross-section figure (see the red arrow in Figure 5).

Note that the layers which belong to the second chip (stack) have **2_** at the beginning of their names (for example **2_cond** vs. **cond**). We assume that the chip-to-chip distance is 8 µm in this flip-chip technology. To accommodate this, we reduce the airbridge heights to 1 µm and leave 6 µm air in between, such that the total chip to chip distance becomes 8 µm. Note that using 0 µm for the airbridge height leads to an error message. Therefore, the minimum of 1 µm is kept for airbridges, but it does not affect the simulation results if your desired total chip-to-chip distance includes this extra 2 µm. Look at **Thickness_2**, **Thickness_3**, and **Thickness_4** in the rightmost table under **Variables** (Figure 5).

Note that in the **Variables** section by default, you only see the frequency, length, width and clearance. To be able to see and change the material and substrate variables, check the boxes next to **Material Vars** and **Substrate Vars**, as shown by the blue arrow on the right side of Figure 5. If you want the change of material type and thickness done here take effect for all simulations in your workspace, find (**Update Substrate/Material Parameters …**) under the **Technology** and press it to save the changes.

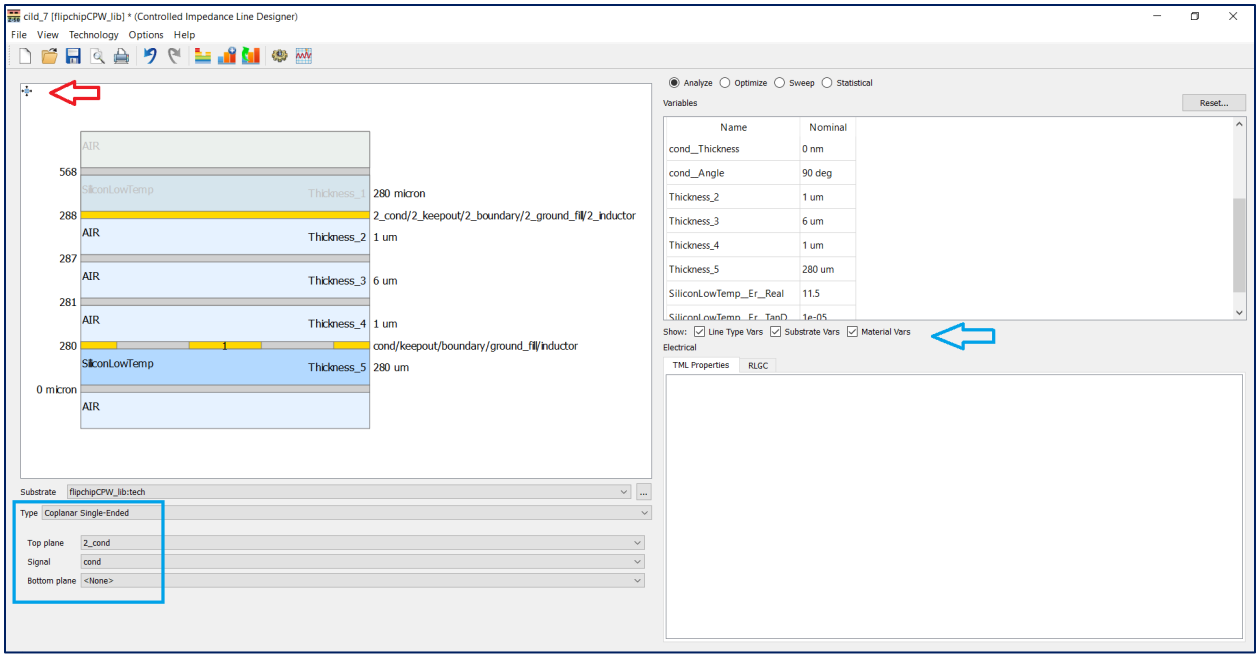


Figure 5. The **Controlled Impedance Line Designer** (CILD). The pop-down menus under **Substrate** (**Type, Top Plane, Singal, Bottom Plane**) are used to design the desired transmission line cross section using the **Width** and **Clerance** given in the top-right table under **Variables**. The CPW cross section is shown in yellow color.

Type B: a CPW facing a silicon (dielectric) substrate layer on top:

For this type of CPW, we change the **Top Plane** to **<None>**, the **Signal** to **cond**, and **Bottom Plane** to **<None>** as shown by the green box in Figure 6. As a result of this, the CPW is formed on the silicon substrate of the bottom chip, and it faces the silicon substrate of the top chip (see the green arrow in Figure 6).

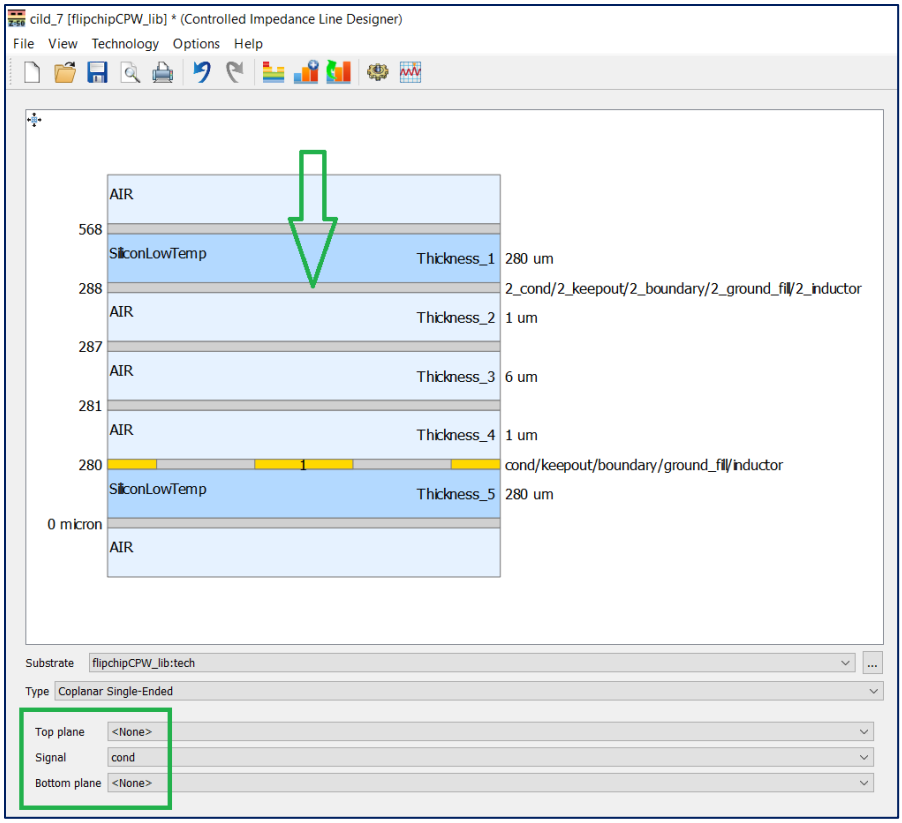


Figure 6. Building a CPW with silicon substrate on top in flip-chip technology (called Type B in this note), by selecting **<None>** as the **Top plane** (see the green arrow).

Calculation of CPW Characteristics

We go back to figure 5 and Type A design, which is a CPW line facing a metal layer on top. On the right section of the CILD panel (under **Variables**) select the typical frequency (**freq**) (e.g., 6 GHz), **Length**, **Width,** and **Clearance** of the CPW to be 1000 µm, 12 µm, and 12 µm, respectively. Width and Clearance are the same as CPW width (W) and gap (g) or spacing (s) in other textbooks. Note that the Length here does not matter as the length of the resonator or feedline will be decided after finding out the effective dielectric constant. The silicon substrate is 280 µm thick and its dielectric constant is 11.5 (that of low temperature silicon). After running the **Analysis,** the results appear in **TML properties** and **RGCL** (see Figure 7).

As you see for this CPW line with (g, W, g) = (12 µm, 12 µm, 12 µm), the characteristic impedance is 47.05478 Ohm**,** and the effective dielectric constant is $\varepsilon_{eff} = 4.5517$. The inductance and capacitance per unit length (shown in the blue box) are L = 334.865 nH/m and C = 151.238 pF/m, respectively. From this the length of a quarter wavelength resonator for a resonance frequency of $f = 6\ GHz$ can be calculated as follows:

$$l = \frac{\lambda}{4} = \frac{v}{4f} = \frac{1}{4f}\frac{c}{\sqrt{\varepsilon_{eff}}} = \frac{3\times10^8\ mHz}{4\times6\times10^9 Hz\sqrt{4.5517}} = 5859\ \mu m \quad (1)$$

Where v is the velocity of the electromagnetic wave (light) in transmission line and it is found from $v = c/\sqrt{\varepsilon_{eff}}$, and c is the same quantity in vacuum. Another way of finding the resonator length is looking at effective electrical length (deg) at the bottom of Figure 7. This quantity says how much the phase of the wave is shifted when it travels along the 1000 µm CPW line. This is 15.3716 degrees. That means to obtain 90-degree phase shift (for a quarter-wavelength resonator), we must increase the 1000 µm by a factor of 90/15.31716 = 5.8758 which gives 5.8758 x 1000 µm = 5875.8 µm, which is very close to what we found in equation (1).

Note that compared to a single chip CPW (the one with Air on top, 5004.1 µm long, the same silicon and metal thickness as here), the flip-chip resonator is 855 µm longer. This is because in the flip-chip technology (with a metal layer over the resonator), the distribution of electric field is not fully concentrated in silicon and a part of that will be directed towards the top metal and air. This will lead to more contribution of the air to the CPW line electric field and reduced effective dielectric constant (from about 6.23983 to 4.5517 in this example). The ratio of single chip to flip chip resonator length is 5859/5004.1 = 1.1708 which is indeed $\sqrt{\frac{\varepsilon_{eff_singlechip}}{\varepsilon_{eff_flipchip}}} = \frac{6.23983}{4.5517} = 1.1708$

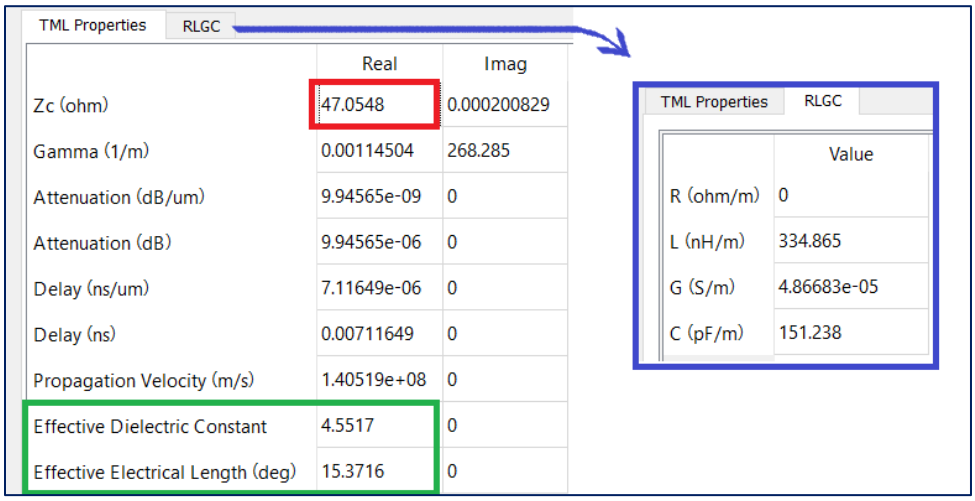


Figure 7. The electrical characteristics of (g, W, g) = (12 µm,12 µm, 12 µm) CPW line facing a metal layer on top.

To make the impedance closer to 50 Ohm (if it is necessary for your design), you can select **Optimize** above the **Variables** table, and then select either **width** or **clearance** for optimization, press **Run** icon on the top menu of **CILD** window (gear-spared icon in Figure 5) to obtain 50 Ohm. We continue with (g, W, g) = (12 µm,12 µm, 12 µm) though for the rest of the calculations in this application note.

Transmon Qubit Capacitance

The calculated capacitance per unit length of a CPW (either single-chip or flip-chip) is a useful number to design the transmon (cross-shaped) qubit capacitance. From this number the approximate (underestimated) value of anharmonicity can be extracted as will be shown later. Figure 8 shows the top view of a transmon qubit in which four arms of the cross are made of a CPW line with (g, W, g) = (12 µm,12 µm, 12 µm). Assuming that the length of each arm is $l_{arm} = 165\ \mu m$, the total capacitance of the transmon in flip-chip technology (with metal of the top chip facing the qubit on the bottom chip) is:

$$C_{qubit} \cong 4 \times l_{arm} \times C\left(\frac{pF}{m}\right) = 4 \times 165\ \mu m \times 151.238 \frac{pF}{m} = 99.82\ fF \quad (2)$$

Note that this an approximation as the fringing fields due to sharp corners of the cross and the contribution of the central square are not captured here. The approximate value of the anharmonicity or charging energy (E_C) is found from equation (1) where e is the charge of electron ($e = 1.602 \times 10^{-19}\ Coulomb$).

$$\frac{E_C}{h} = \frac{e^2}{2hC_{qubit}} \cong 194.2\ MHz \quad (3)$$

and h is Planck constant ($h = 6.626 \times 10^{-34}\ Joule.sec$). Therefore, this quick simulation in CILD allows you to decide about the shape of transmon (either in single-chip or flip-chip technology) and find a ballpark value for qubit frequencies and anharmonicities before running a more precise simulation e.g., Energy Participation Simulation using FEM in QuantumPro.

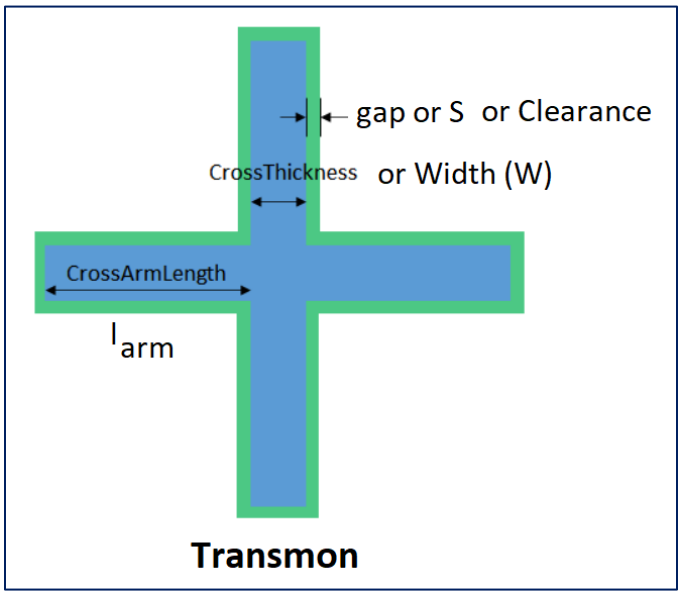


Figure 8. Top view of a transmon (Xmon) qubit and related design parameters. Green and blue mean exposed silicon surface (substrate) and aluminum (metal or **cond**), respectively.

Sensitivity to Chip-to-Chip Distance

To investigate the sensitivity of the CPW parameters on the chip-to-chip distance, we can use the **Sweep** option in the **CILD** menu on top of the **Variables** panel (see Figure 5). After selecting **Sweep**, the **Variables** table is changed and it gives longer rows allowing to enter the start and end values, number of steps and or the size of the step for sweeping (See Figure 9). Here we only select the **Thickness_3** for sweep analysis. It is swept from 1 µm to 30 µm in 1 µm steps, that means the chip-to-chip distance is changing from 3 µm to 32 µm. After running the sweep (gear-shaped icon on the top menu bar of CILD window), the data display panel is opened and multiple plots appear as shown in Figure 10. They are e.g., impedance, inductance and capacitance per unit length, effective dielectric constant, etc. versus **Thinkness_3**. It is possible to export these plots as .csv files, process and plot them in Python, MATLAB, or Octave.

Figure 11 shows the characteristic impedance (Z_c) of Type A CPW (metal on top) as a function of chip-to-chip distance which is **Thinkess_3** + 2 µm.

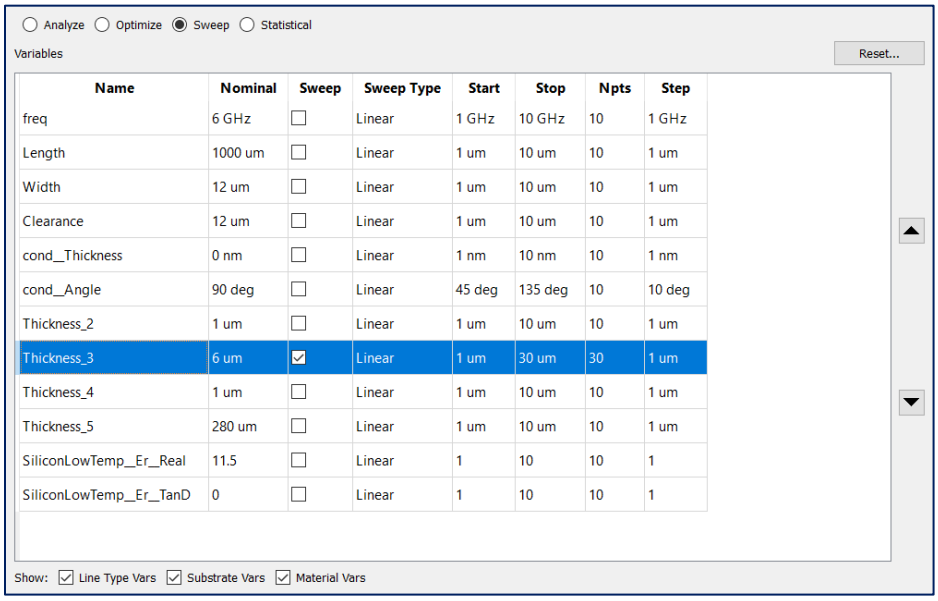


Figure 9. Selecting the **Sweep** to run a sweep analysis for **Thickness_3** in **Variables** from 1 µm to 30 µm. Note that a multitude of sweep options are available e.g., frequency sweep.

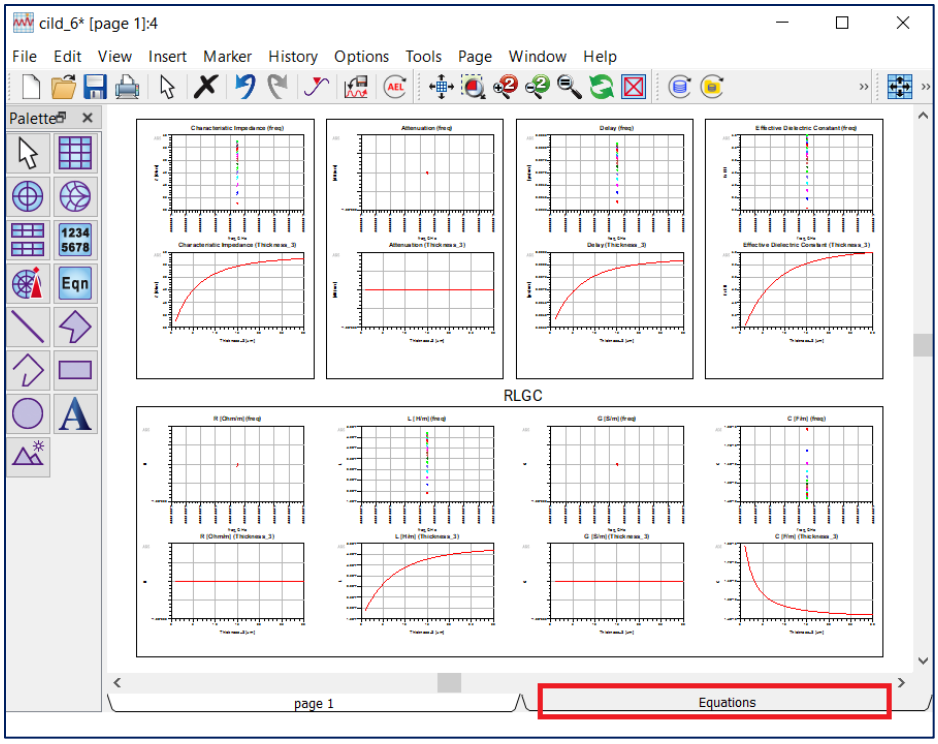


Figure 10. Results of running air thickness sweep for finding out the sensitivity of parameters to chip-to-chip distance. CPW faces a metal layer on top (Type A in the main text).

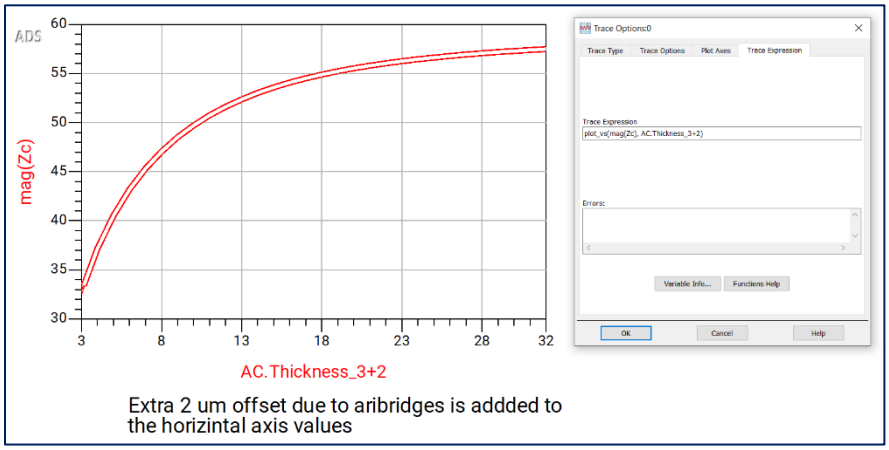


Figure 11. Characteristic impedance (Z_c) of Type A CPW (metal on top) as a function of chip-to-chip distance which is **Thinkess_3** + 2 µm.

Under the data display panel, you can see the page in which the necessary equations are listed (red box at the bottom of Figure 10). Select this page by clicking on it and you see Figure 12. As can be seen, parameters like group velocity and effective dielectric constant are calculated from the inductance and capacitance per unit length.

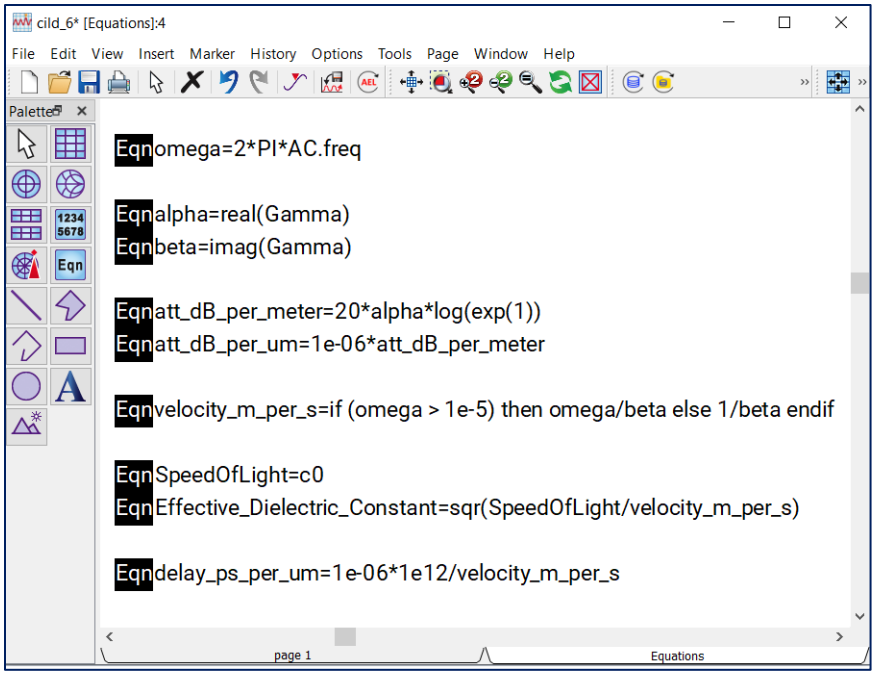


Figure 12. Equations listed in a separate page in data display. They are used for post-processing of CILD results.

The change of CPW line characteristics with chip-to-chip distance emanates from the change of capacitance an inductance per unit length. As can be seen in Figure 13, by lowering the top chip, the capacitance per unit length increases which is due to closeness of the top metal to the center line of CPW and more contribution to the capacitance as a result.

Bringing the top metal closer to the CPW, however, reduces the inductance per unit length drastically. This is due to the closeness of the return current on the top metal to the main current on the CPW central lines. As these currents are oppositely flowing, the total inductance is decreased. See Chapter 15 of Kaiser's book [1] for the total inductance formula of two parallel lines. This suggests that designers should be always aware of the return current and its effect on the resonance frequency of resonators, mutual inductance of flux lines, among others. One way of avoiding such an effect is making sure the resonators are not facing the metal layer of the top chip and instead they face silicon substrate. Alternatively, the top metal layers shadowing over a resonator or flux line can be lithographically etched and patterned such that return current path is interrupted [2].

Sensitivity to chip-to-chip distance is reduced if the top layer facing the resonator is silicon substrate. In this case by reducing the chip-to-chip distance, the capacitance per unit length is increased because the electric field can penetrate the top silicon layer as well and this increases the effective dielectric constant. On the other hand, the inductance per unit length remains constant as the return current does not flow inside the top silicon layer.

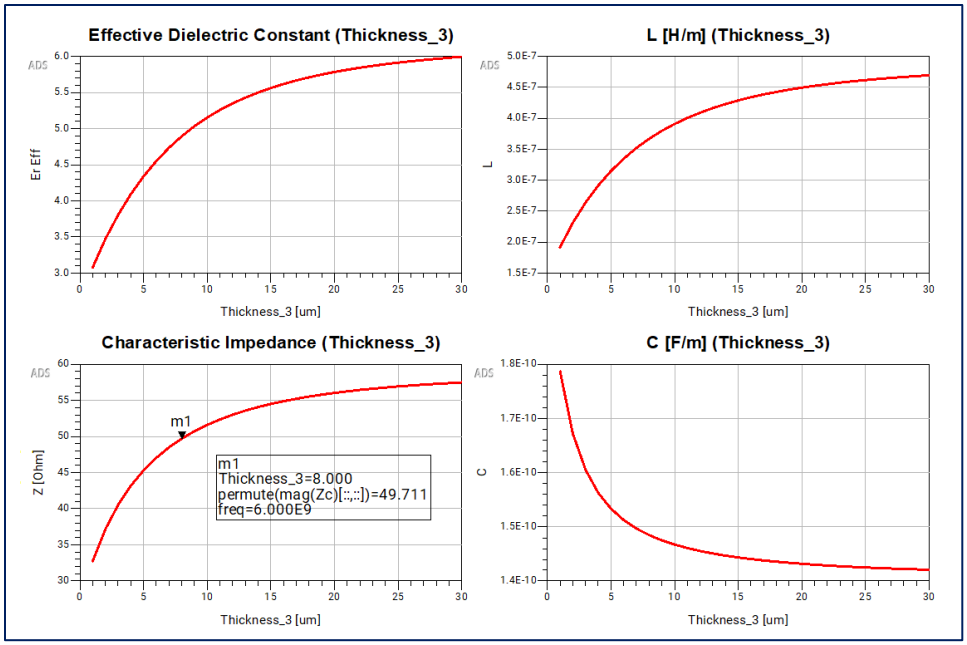


Figure 13. Characteristics of a Type (A) CPW with (g, W, g) = (12 µm, 12 µm, 12 µm) versus the chip-to-chip distance.

Design of a Single Transmon Qubit in Flip-Chip Technology

Now we are ready to design a qubit in flip-chip technology. In this example, a cross-shaped transmon qubit on the top chip is coupled to a quarter-wavelength readout resonator sitting on the bottom chip. Note that this is an example to show how the schematic, layout, and QuantumPro EM simulation setup is prepared for a multichip (flip-chip) design. The exact shape of your circuit and design parameter values always depends on your own design and application of choice, and they don't need to follow the numbers or geometries suggested here.

Open a new schematic window and place the components from **Quantum Artwork** library and connect them as shown in Figure 14. Note that all elements with (**Q_Cpw**) in their name are the same as those we did for a single layer quantum technology design. The geometrical parameters of CPW in this example are (g, W, g) = (12 µm,12 µm,12 µm). The radius of the bends is 100 µm. The horizontal and vertical CPW line sections which make the common feedline are 500 µm long. The coupling element (**Q_CpwCouplerT**) helps you to design the layout of the section where resonator is coupled to the feedline (readout line). It has the same CPW parameters for both the feedline part and the resonator parts. The **PrimeLeadLength** is 100 µm, the **SecondLeadLength** is 70 µm. The **SecondParallelLength** is 125 µm. The **Fillet** and **GroundBuffer** are 50 µm and 10 µm, respectively. To create a short circuit at the coupling end of the resonator, the **SecondOpenTerminal** must be set to (**no**) meaning that it will not be open.

For the meandering resonator leave everything as default value except the **width** and **clearance (gap)** which are W = 12 µm and g = 12 µm and set the length to be 4000 µm. With extra lines added to the resonator, this gives the resonance frequency of approximately 7.5 GHz. However, you can choose whichever resonance frequency you want and change this according to the effective dielectric constant you obtain from CILD calculation. So far, all elements belong to the Layer set 1 except the transmon qubit and its shunt inductor (model of Josephson junction).

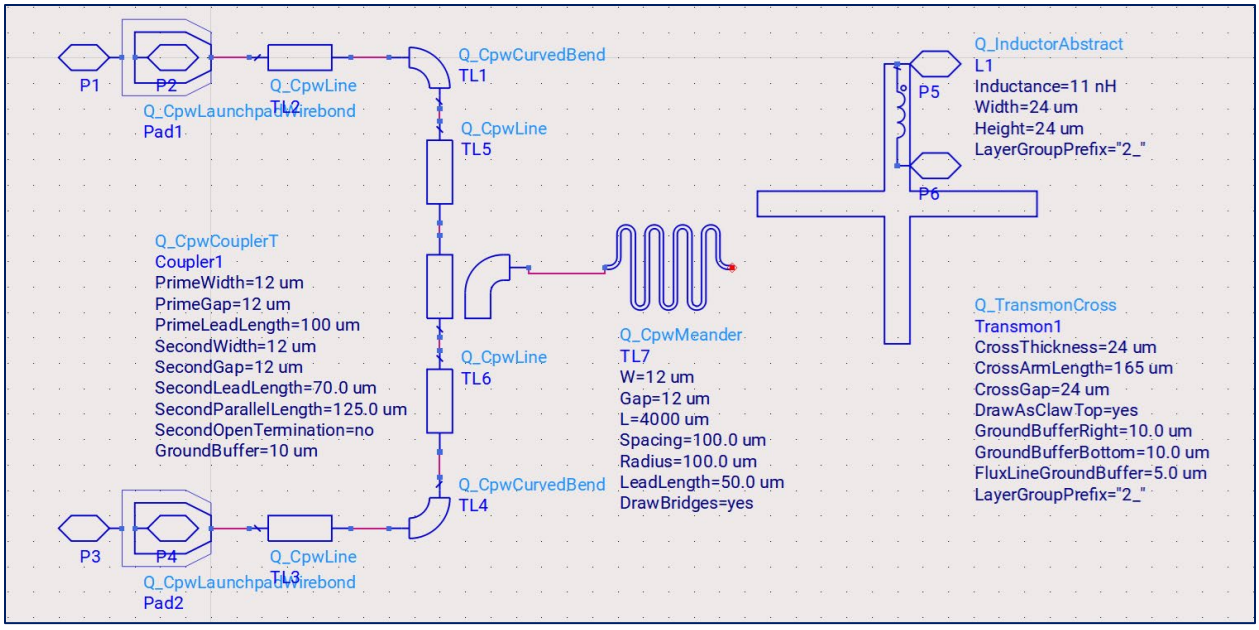


Figure 14. The schematic of a feedline, resonator and a transmon qubit for the flip-chip example.

Insert a transmon from **Quantum Artwork** and set all **Draw (Top, Bottom, Left, Right) Connector** options as (**no**). You don't need any **Claw** at the ends of each transmon arm (for coupling) as the qubit sits on the second chip and shadows over the resonator end and coupling is achieved this way. Hence make all **DrawAsClaw…** options to be (**no**). Let the **gap** and width (**CrossThickness**) of the transmon arm be 24 µm and the length (**CrossArmLength**) of each arm be 165 µm. Do not forget to change the **Height** of the **Q_InductorAbstract** to 24 µm, otherwise the inductor patch will not fit in the transmon gap, and it creates layout errors. As we will see, direct connection between qubit and resonator is not required in this flip-chip design. Just put the transmon somewhere close to the resonator in the schematic, as the real location will be fixed in the layout editor. Place a **Q_InductorAbstract** on the transmon top arm terminals and set its value to be 11 nH. This gives a qubit frequency of approximately 4.7 GHz (based on the underestimation of capacitance in equation (2)). Add ports to the schematics i.e., P1 to P6 as shown in Figure 14.

How to tell the Schematic/Layout editor that transmon and inductor belong to the top chip or Layer 2 of the Stack? For this, click on the transmon icon in the schematic and open the **Edit Instance Parameters** window as shown in Figure 15(a). Thereafter, go to the very bottom of the **Select Parameter**. Here you must change the prefix of the layers to be "**2_**" so that the layout editor knows the layers listed under the **LayerGroupPrefix** belong to the second chip. For this change **LayerGroupPrefix** to be "**2_**". Do this for the inductor as well [as shown in Figure 15(b)].

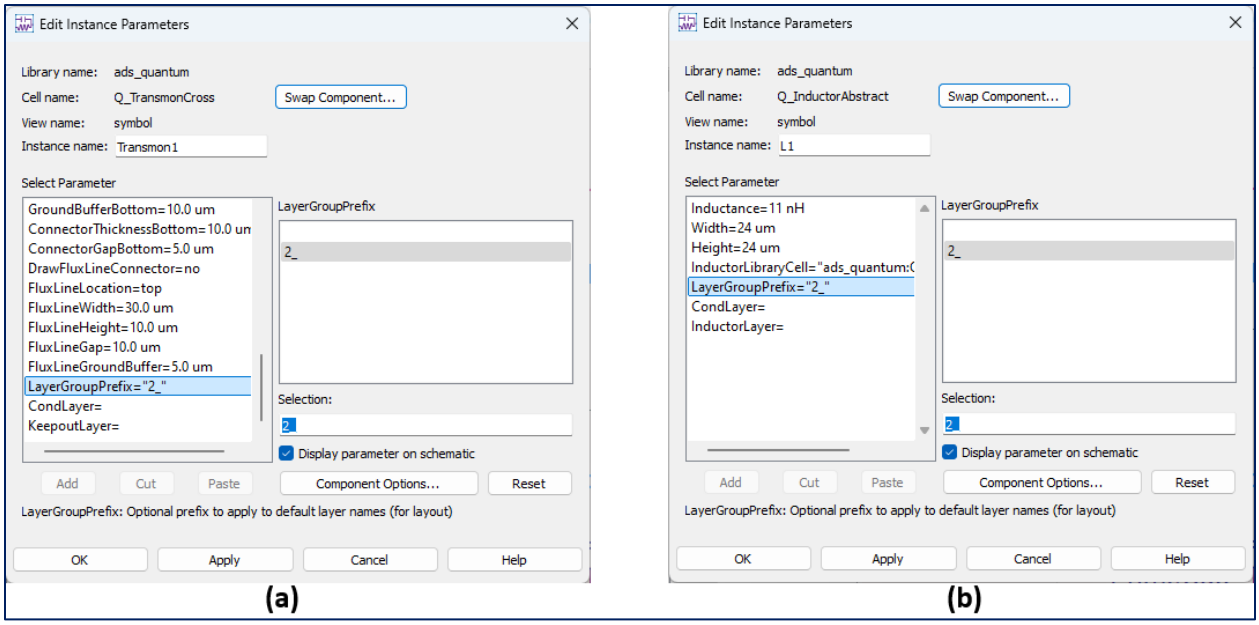


Figure 15. Changing the **LayerGroupPrefix** to "2_" for the components which belong to the second chip in the schematic editor. This is how the layout editor finds out that these components (transmon and inductor) belong to the second chip.

Then save the schematics and press **Layout > generate/update layout** from the top menu, and this opens the layout editor. The layout should look like what you see in Figure 16. As you see there is no connection or coupling between the qubit and resonator yet. The boundary layers of both chips are not drawn yet. There is no bump connecting the ground planes of both chips yet.

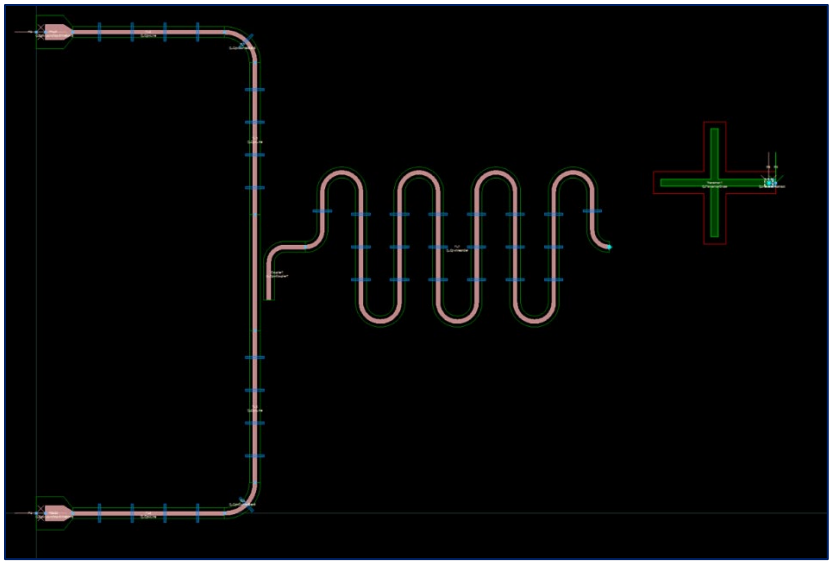


Figure 16. The layout of a feedline, resonator and a transmon qubit for the flip-chip example. The qubit-resonator coupling part, the boundary layers (ground planes), and bumps are not drawn yet.

Now select the transmon, inductor and the pins by mouse and drag them closer to the resonator open end (see Figure 17.a). Select the **cond** layer in the left panel (orange box in Figure 17.a) which lists the **Layers,** and then draw a CPW center line starting from the resonator end (blue dot in Figure 17). Usually, the mouse pointer snaps to this point when you start drawing. For this you click on the **InsertPath** icon on the top horizontal menu (red box in Figure 17.a). From the resonator end move towards the center of the cross-shaped transmon and click there again to stop drawing. You can click again on the line you just drew and see its properties in the menu which appears on the right side of the layout editor. Change the line width to be 12 µm. Repeat the above steps: Select **keepout** layer, click on **InsertPath** and draw a line along the same path as **cond** and increase its with to be 36 µm. This completes the extension of CPW line from the resonator open end towards the center of the transmon (See Figure 17.b).

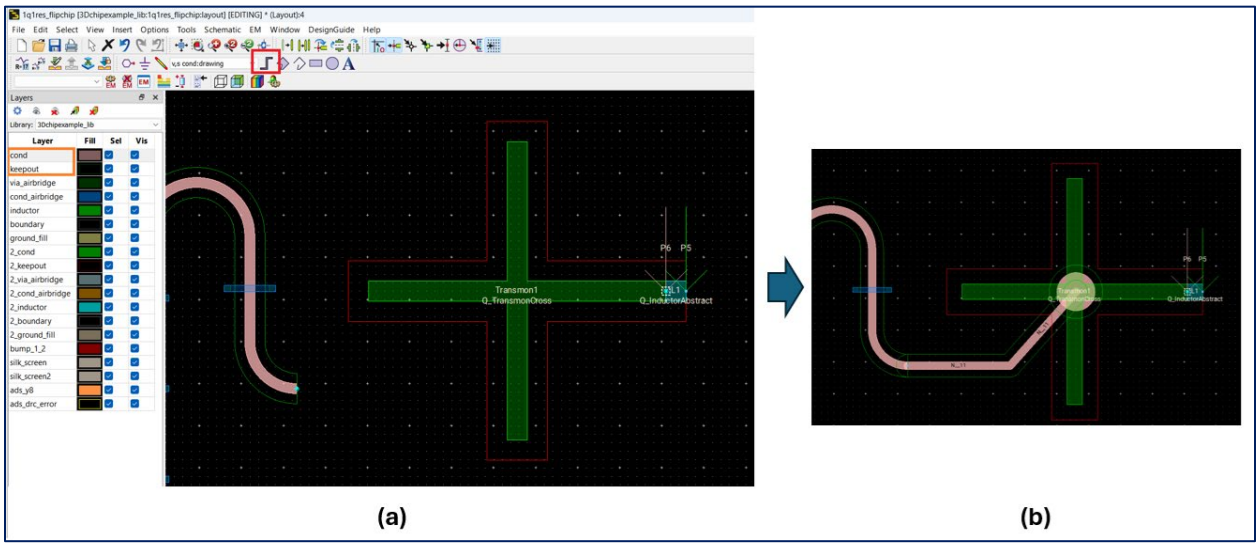


Figure 17. (a) Resonator and qubit coupling area which must be completed by drawing a **cond** line (purple) and its **keepout** (green thin line). (b) The completed resonator-qubit coupling section.

At the end of the newly drawn CPW (which is concentric with the transmon), draw a circle of 30 μm radius using **cond** layer, then draw another concentric circle with 42 μm radius using **keepout**. This is the part which defines the coupling capacitance between the transmon (on the top chip) and the resonator (on the bottom chip). See Figure 17.b. The coupling capacitance is approximately proportional to the overlapping area of this circular patch and the transmon cross (Figure 17.b). You can select the transmon and its attached inductor (with pins) and use **Ctrl+R** to rotate the transmon layout if need be (in case you want JJ to be on the north or south side of the layout). In multiqubit chips it is suggested that all JJ's have the same direction as lithographical process of JJ fabrication demands so.

Now select the **boundary** in the left Layer menu and draw a rectangle around the whole layout. This is the ground plane of your first chip (bottom chip). Then select **2_bounday** layer and draw a smaller rectangle around the transmon qubit. The size of the second chip (boundary) depends on your design.

In this example we let the ground plane of the second chip cover the bottom chip expect the bonding pads on the left (see Figure 18). In flip-chip technology, the ground planes of both chips are galvanically connected to make a uniform ground. Select **Bump_1_2** layer (red colored) and draw a few arrays of circles with 30 μm radius. Make sure that they don't overlap with any other component. They are meant to stitch two ground planes of both chips. The finished layout is shown in Figure 18.

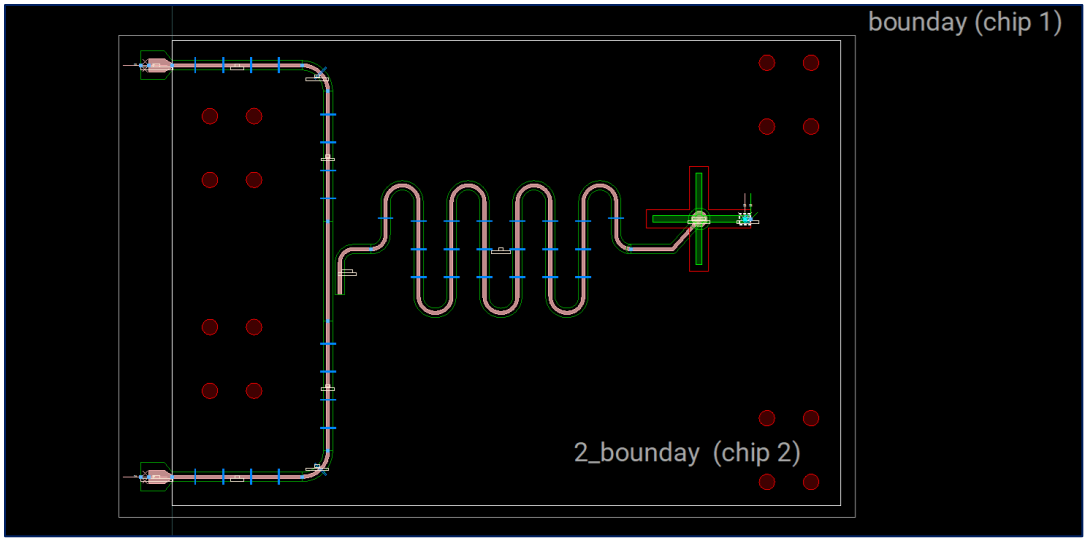


Figure 18. Top view of the device layout after drawing the qubit-resonator coupling part, bumps, and boundary (ground) layers of both chips.

For EM simulation, go to **Tools>QuantumPro** and open a new **QuantumPro** simulation setup. To better see the structure of bumps and the layout of the bottom chip you can scale the Z axis using the scroll button on the top (see the green box in Figure 19). Make sure after changing it to the scale you want, always press **ViewAll** button (see the red box in Figure 19) to bring back the layout in the viewing window. Figure 19 shows the birds eye view of the flip chip design with red bumps connecting grounds. For this example, we chose the **Air Thicknesses** in the substrate material setting be 1 μm, 6 μm, 1 μm. Meaning that air bridges are 1 μm tall for each chip (although the 2nd chip or top chip does not use any air bridges here). The chip-to-chip distance is then 8 μm in total and the parameters of CPW line e.g.,

inductance/capacitance per unit length and effective dielectric constant can be calculated using CILD for these settings.

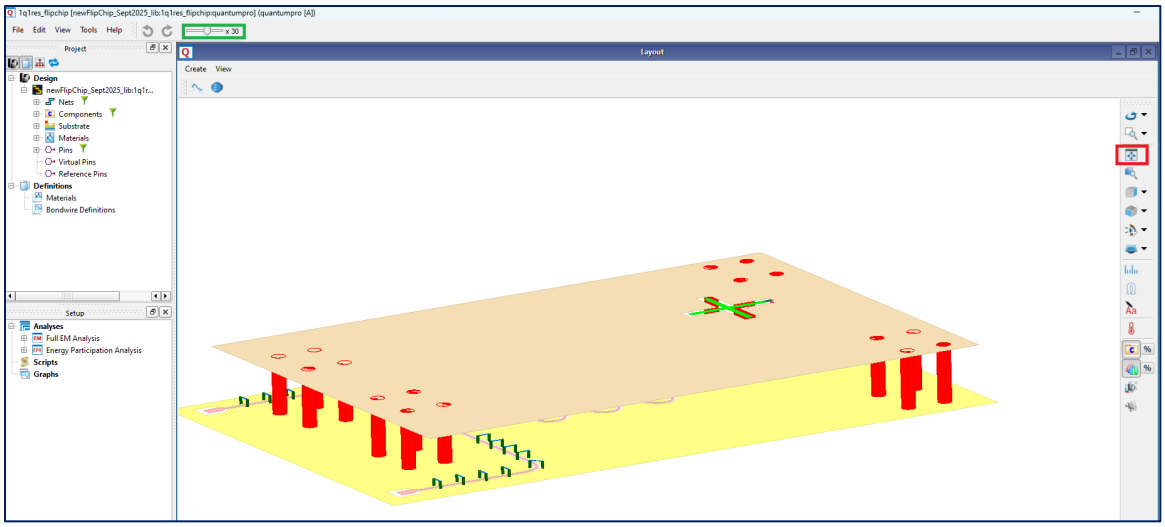


Figure 19. Exaggerated (Z-scaled) view of the transmon and readout devices in flip-chip technology. The chip-to-chip spacing (or bump height) is 8 μm and the air bridges are 1 μm tall.

EM Simulation and Parameter Extraction

For setting up the EM simulation and running the Full EM analysis or Energy Participation Analysis, the process is the same as the single chip designs which are already covered in Quantum Pro demo videos and documents. For example, see How to Design Superconducting Qubits Using QuantumPro | Keysight

Figure 20 shows the result of Full EM analysis. For this analysis we chose **Momentum Microwave** with 200 cells per wavelength (200 cpw). For **2_cond**, **cond** and **bump_1_2** layers the **Mesh density** was increased to 2000 cpw for better results. The **Edge mesh** was set to be **Automatic**. The parameters are extracted from the S-parameter shown in the figure. There are two resonances; one in 4.55 GHz and 7.1 GHz which are qubit and resonator frequencies, respectively. To assist the parameter extractor in finding the resonances, it is suggested to add another sweep (see the green box in Figure 20) after the default adaptive sweep e.g., you can add more finely spaced frequency points around 7 GHz or 4 GHz (or wherever you expect the resonances might be). Note that if the qubit-resonator coupling capacitor is very small, the qubit resonance has very high quality-factor due to under-coupling. In these cases, you need higher number of frequency points as finding the sharp resonances by the curve fitting method in Quantum Pro becomes difficult. The qubit anharmonicity, cross-Kerr, and resonator anharmonicity are given in green, yellow, and blue boxes, respectively. Better precision is achieved if Energy Participation Analysis with Finite Element Method (FEM) is used.

Figure 21 shows the table of extracted parameters using Energy Participation Analysis. Two eigen frequencies were found by the simulator which correspond to the qubit and resonator frequencies (4.37 GHz and 7.36 GHz, respectively). However, there are some differences between the MoM and FEM results (compare Figure 20 and 21). With a better meshing in Full EM analysis this difference can be minimized. For Energy Participation Analysis simulation, the mesh starts from 6 μm for both **cond** and **2_cond** layers. The bump layer is initially meshed at 10 μm. Final mesh is shown in Figure 21. The qubit anharmonicity, cross-Kerr, and resonator anharmonicity are given in green, yellow, and blue boxes, respectively.

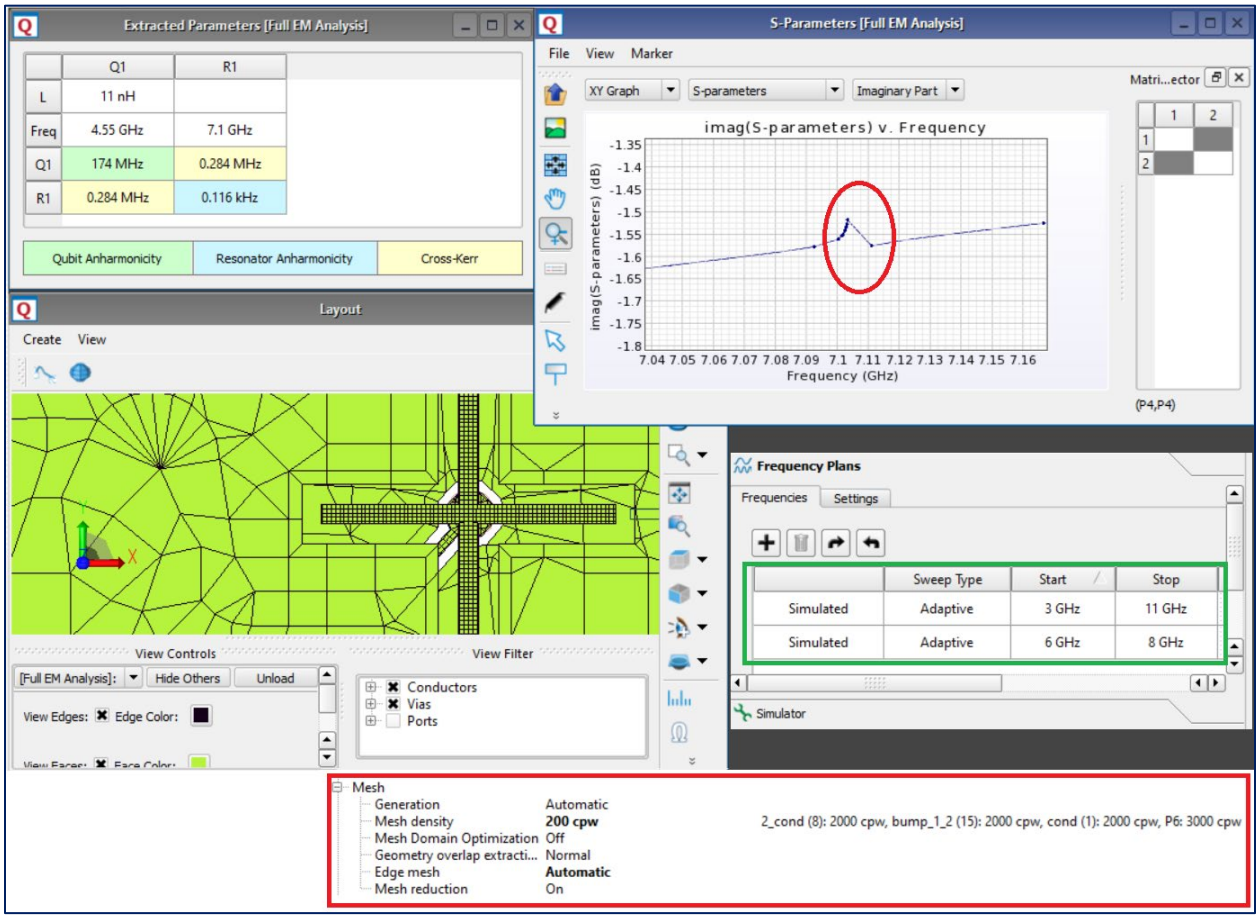


Figure 20. The Full EM analysis results based on S-parameter. The momentum microwave (MoM) method was chosen for this simulation. The dots in red area are extra sweep from 6 GHz to 8 GHz in addition to the adaptive sweep (see the green box). The red rectangle shows extra settings for Mesh density. P6 is the pin attached to the shunt capacitor of the transmon. See the refined meshing on the transmon as a result.

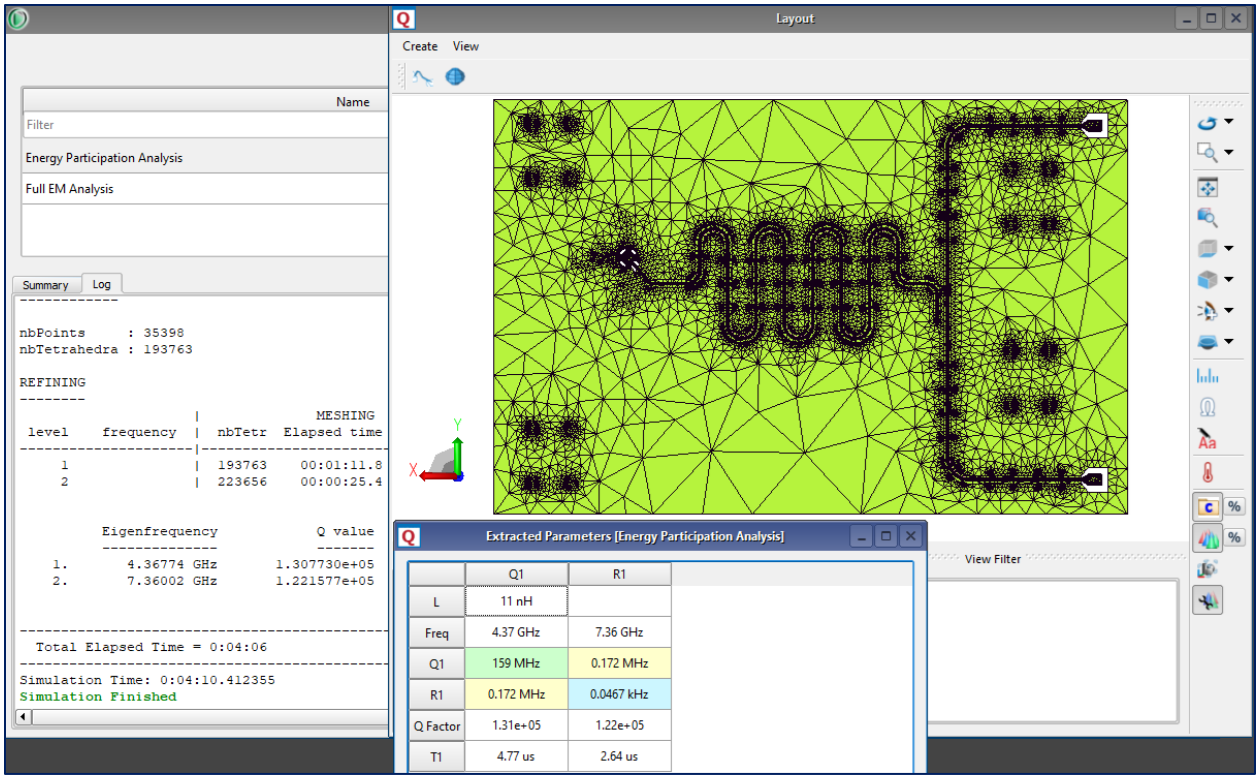


Figure 21. The Energy Participation Analysis results using FEM method and extracted qubit and resonator parameters. Bottom view of the flip-chip device with the overlaid mesh generated by FEM method.

From the anharmonicity ($E_C = 159\ MHz$) (see Figure 21, bottom table), we can extract the value of qubit total shunt capacitance. From equation (3) we obtain:

$$C_{qubit} = \frac{e^2}{2E_C} = 121.7\ fF \tag{4}$$

The qubit-resonator coupling capacitance is found from g (resonator-qubit) couiling strength. The factor g depends on the cross-Kerr factor ($\chi = 0.172\ MHz$) through the following equation:

$$\chi = \frac{g^2 E_C}{\Delta(\Delta - E_C)} \tag{5}$$

Where Δ is the detuning between qubit and resonator frequency i.e., $\Delta = f_{res} - f_{qubit} = 7.36 - 4.37 = 2.99\ GHz$. Therefore, from equation (5) we have $g = 95.6\ MHz$.

Using equation (6) we can use g to find the qubit-resonator coupling capacitance (C_g). In the following equation, C_g is the qubit capacitance (which we found before), C_{res} is the effective resonator capacitance which is half of the total resonator capacitance as explained in this application note (Calculation of CPW Resonator Properties Using the Quantum Technology File | Keysight) and reference [3].

$$g\ (Hz) = \frac{C_g}{2\sqrt{C_{res}C_{qubit}}}\sqrt{f_{res}f_{qubit}} \tag{6}$$

For equations (3), (4), and (5) you can consult with Daniel Sank's PhD Thesis [4].

Knowing the capacitance per unit length of CPW resonator (from CILD calculations) we can write:

$$C_{res} = \frac{C_{res_total}}{2} = \frac{C\ (per\ unit\ length\ of\ CPW) \times length\ of\ resonator}{2} = \frac{151.23\ ^{pF}/_{m} \times 5859\ \mu m}{2} = 443\ fF \quad (7)$$

Using the above number and the rest of data in equation (6), the qubit-resonator coupling capacitance is $C_g = 7.8\ fF$.

The electric and magnetic fields and the surface current density can be plotted at each eigen frequency (qubit or resonator). Figure 22 shows the electric field at resonance of the qubit (4.37 GHz).

The surface-current density on the top-chip ground layer is shown in Figure 23. This is plotted for the second eigen frequency which is the resonator frequency (7.36 GHz). As can be seen the current vector path resembles the shape of the meandering resonator on the bottom chip. This is the image or return current which flows on the top chip in response to the current passing through the central line of the CPW on the bottom chip. The inductance per unit length of the resonator on the bottom chip is reduced due to this return current (as the main current and the return current have opposite directions). This leads to sensitivity of the resonance frequency to the chip-to-chip distance variation in flip-chip technologies.

To make the resonator insensitive to chip-to-chip distance variation, the metal on top of the resonator can be removed or interrupted to stop the flow of the return current as discussed in [2].

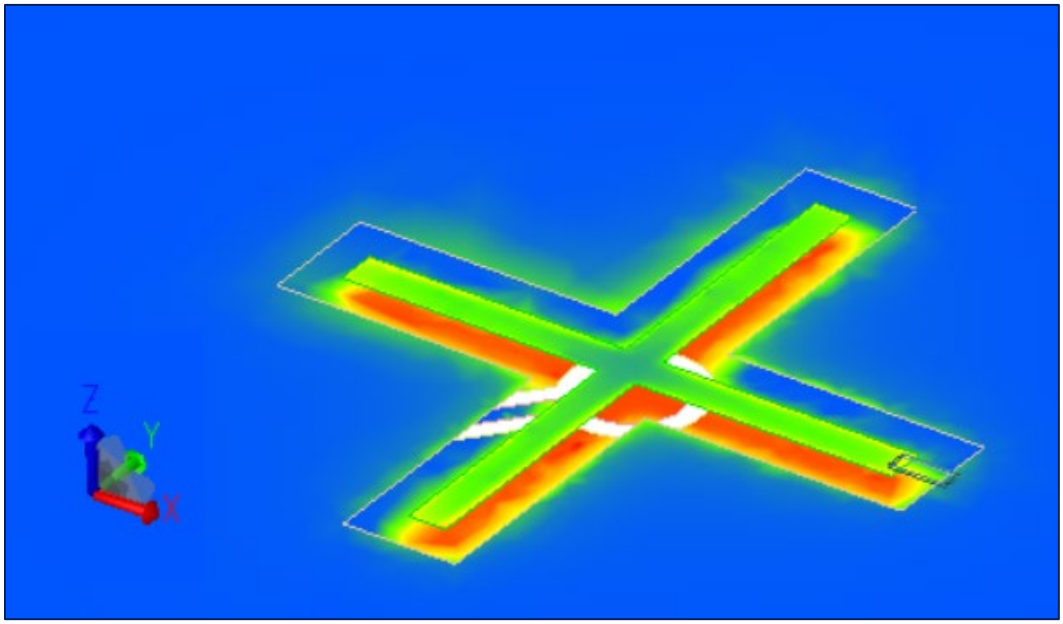


Figure 22. Electric field at qubit frequency (4.37 GHz). The qubit is on the top chip and the resonator is on the bottom chip coupling to the qubit by its circular patch.

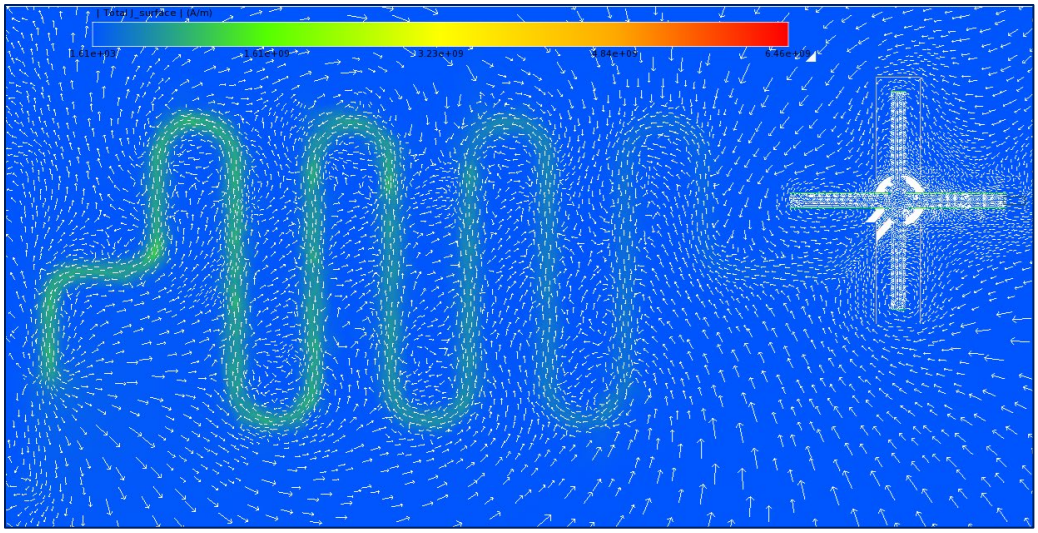


Figure 23. Top view of the surface current density on the top chip ground plane (at 7.36 GHz i.e., the resonator frequency). Notice the return current path which resembles the shape of the resonator beneath this layer.

Regarding Q_Bump and Bump_1_2

Note that in the above example **bump_1_2** layer (red colored) was used in the layout editor to connect the ground planes of both chips. There is another component in **Quantum Artwork** library which is called **Q_Bump**. This bump is meant to connect the CPW lines of a chip to the same lines of the other chip. This has by default **keepout** layers on both chips which makes the transition of CPW's possible. To connect the ground planes of two chips you cannot use this element because of the **keepout**. Figure 24 shows a simple schematic in which a CPW is split into two sections using **Q_Bump** and the right half is on the top chip. Note that everything on the right-hand side of the **Q_Bump** must be edited such that the layer prefix becomes "**2_**", a process which was explained in Figure 15.

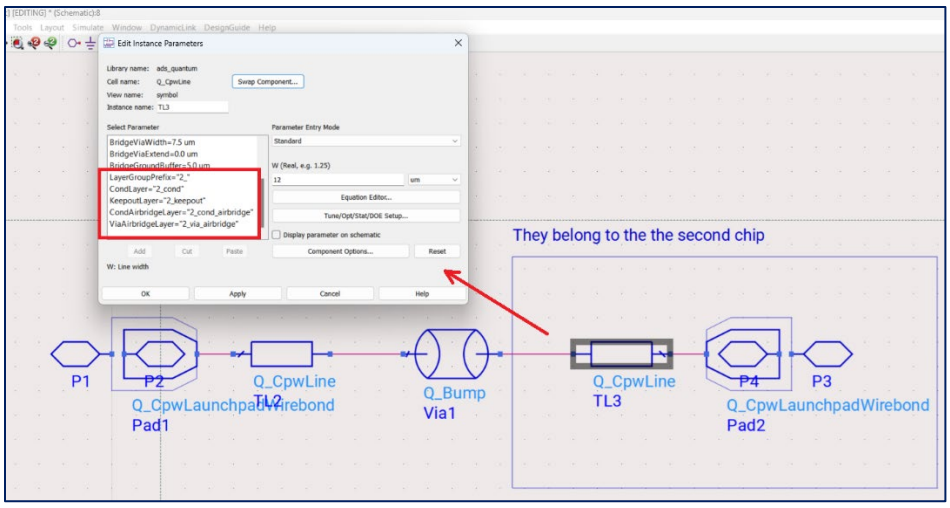


Figure 24. The schematic of an interrupted CPW by **Q_Bump**. The CPW is split into two halves; one (left) on the bottom chip and the other (right) on the top chip.

The layout is shown in Figure 25. Note that the boundary layers must be added before starting the Quantum Pro EM simulation. The exaggerated (25X scaled up Z coordinates) layout in Quantum Pro is shown in Figure 26. See how each CPW on each chip has its own airbridges and how the bump connects two CPWs but not the ground planes. To connect ground planes for EM simulation, you must use **bump_1_2** layer in the layout editor as it was explained in Figure 18.

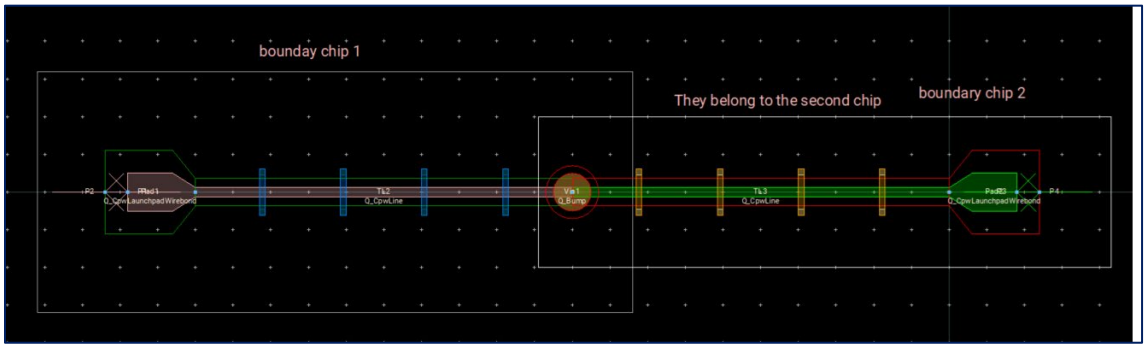


Figure 25. The layout of an interrupted CPW by **Q_Bump**. The CPW is split into two halves; one (left) on the bottom chip and the other (right) on the top chip.

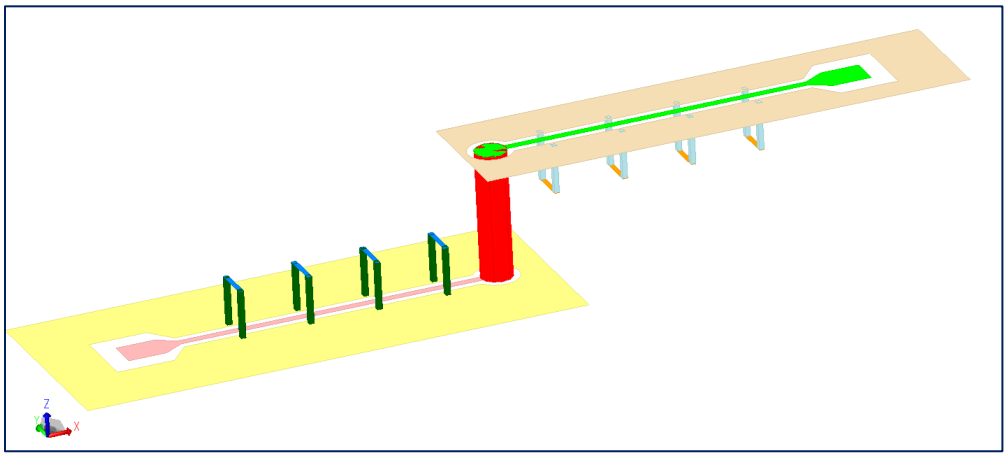


Figure 26. The layout view in Quantum Pro. The z axis is scaled up 25 times. The **Q_Bump** (red color) connects both halves of the interrupted CPW line in the flip-chip technology.

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[1] Keneth L. Kaiser, Electromagnetic Compatibility Handbook, CRC Press, Boca Raton (2005).

[2] H. -X. Li et al., "Experimentally Verified, Fast Analytic, and Numerical Design of Superconducting Resonators in Flip-Chip Architectures," in IEEE Transactions on Quantum Engineering, vol. 4, pp. 1-12, (2023).

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[4] Daniel Sank, PhD thesis at University of California, Santa Barbara (2014), downloadable from Fast, Accurate State Measurement in Superconducting Qubits

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