

Optimizing Photodetector Model to a Silicon Photonics Foundry Process

Achieving unprecedented accuracy in photonic integrated circuit (PIC) simulations

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Introduction

The rapid advancement in photonic integrated circuits (PICs) calls for sophisticated tools that streamline the design and validation process. Keysight Photonic Designer represents a leading-edge photonic design automation (PDA) solution, purpose-built to address the demands of next-generation photonic integrated circuit (PIC) design. This tool supports the creation of both purely optical circuits and hybrid electro-optical (EO) or opto-electrical (OE) systems. By incorporating sophisticated, physics-based models, Keysight Photonic Designer ensures each design step—from initial concept to final validation—is seamless and precise. With an intuitive interface and robust design verification capabilities, Photonic Designer facilitates efficient generation and validation of layouts, ensuring they meet stringent design criteria and are optimized for reliable fabrication and performance.

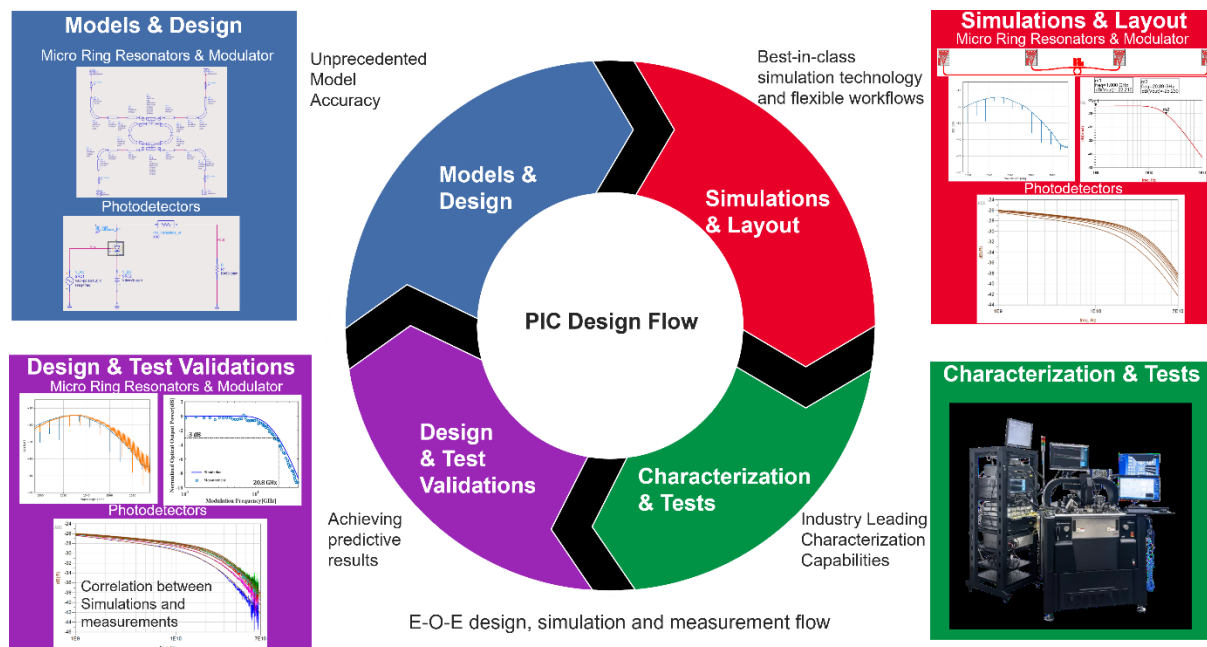


Figure 1. The complete photonic design ecosystem offered by Keysight Photonic Designer from conceptualization to validation.

To streamline the customization process, **Keysight Photonic Designer** offers a **template silicon photonics process design kit (PDK)** as part of the initial release. This template includes versatile, physics-based models that simulate both passive optical and active electro-optical components. It's designed to be flexible, allowing users to modify design variables to reflect a target foundry's specific manufacturing parameters. The template PDK ensures that users can adjust parameters to capture subtle yet impactful variations across different fabrication processes, which is essential for developing PICs that consistently meet stringent performance standards.

In this application note, we delve into an example involving a **PIN photodetector** model. By demonstrating how to fine-tune this model to a specific foundry process, we illustrate the potential of Photonic Designer to customize designs for manufacturing conditions. This process of tuning involves both the semiconductor properties of the PIN photodetector and the parasitic elements in its layout, allowing designers to achieve a high degree of accuracy by aligning simulation results with real-world measurement data. We'll cover steps from initial setup to validation against measurement data from a previously fabricated chip, providing a step-by-step approach to PDK customization.

Understanding the PIN Photodetector Model

The PIN photodetector model within the Keysight Photonic Designer is carefully crafted to simulate the nuances of this component. It includes both semiconductor properties and the parasitic elements that arise in a practical layout, such as vias, metal pads, and other resistive or capacitive elements. By capturing these parasitics, the model produces simulation results that align closely with empirical data, which is essential for designs that demand high bandwidth and signal fidelity.

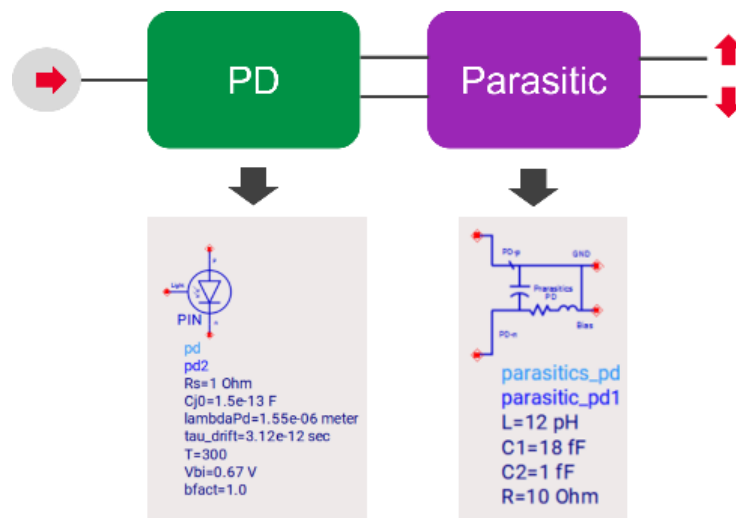


Figure 2. The photodetector includes both semiconductor properties (captured by **PIN** symbol on the left) and the parasitic elements (captured by **parasitics_pd** symbol on the right) that arise in a practical layout, such as vias, metal pads, and other resistive or capacitive elements model.

This model offers 37 design variables, of which 21 relate directly to the underlying physics of the photodetector, defining properties such as carrier mobility, junction capacitance, and depletion region parameters. The remaining 16 variables are accessible for user-driven layout customization, allowing control over physical dimensions, electrode placements, and material properties. Details about these design variables can be accessed via [ADS online documentation about Photodetector](#).

The available design variables can be used to extract different performance parameters of the PIN photodetector, such as:

Diode current using the Shockley diode equation

$$I_d = I_0(e^{\frac{V_D}{\eta V_T}} - 1)$$

Diffusion and Drift related parameters

- Diffusion current fraction: $A_{diff} = -p_{1diff}V_D + p_{2diff}$
- Drift current fraction: $A_{drift} = 1 - A_{diff}$

Noise

$$SI_{thermal} = \frac{4kT}{R}$$

Accessing and modifying these variables is straightforward: users can double-click the photodetector symbol in the schematic view, opening the **Edit Instance Parameters** window where they can adjust each parameter as needed.

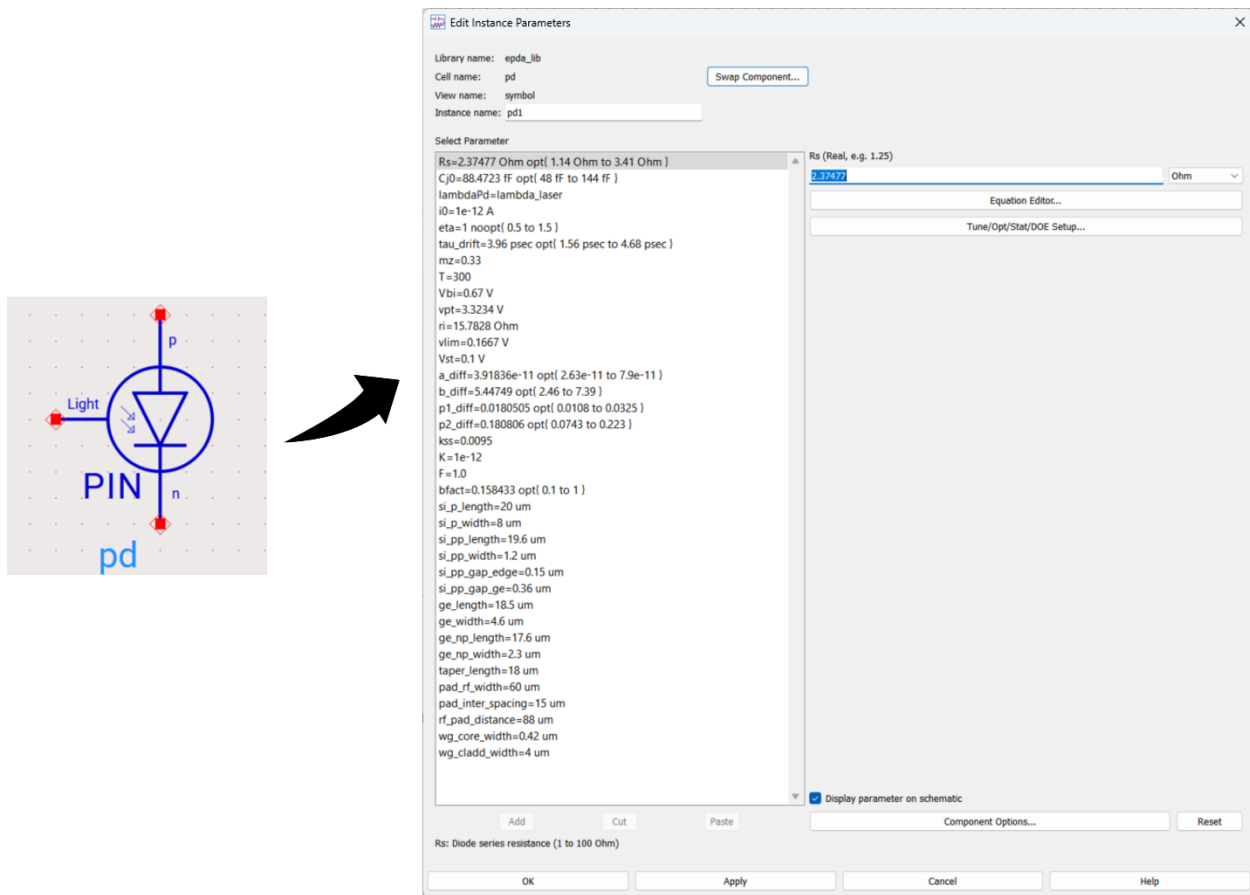


Figure 3. Variables associated with the model can easily be accessed by double clicking on the symbol in the schematic. Detailed documentation about PIN photodetector can be accessed by clicking the **Help** button at the bottom of the **Edit Instance Parameter** window.

Supported simulators

PIN photodetector model can be used with the below listed simulators:

- AC
- DC
- S-parameter
- Transient
- Envelope
- Harmonic Balance

It is important to note that the S-parameters simulator in ADS is defined as an electrical stimulation. PD is an opto-electronic device and therefore while an S-parameter simulation can be performed, the absolute value of the calculated opto-electronics S-parameters is not always representative of the real-world scenario. It is suggested to use AC simulation instead of S-parameter simulations.

Setting Up the PIN Photodetector Simulation

To begin the tuning process, we'll conduct an **AC small-signal simulation** of the PIN photodetector to determine its **3-dB bandwidth**—a critical performance metric in high-speed applications. In this simulation setup, the photodetector is configured with parasitic components, bias voltage, load resistance, and an optical input source. By covering frequencies from **10 MHz to 67 GHz**, we simulate a range typical of photodetectors in data communication systems, ensuring the model behaves realistically under operational conditions.

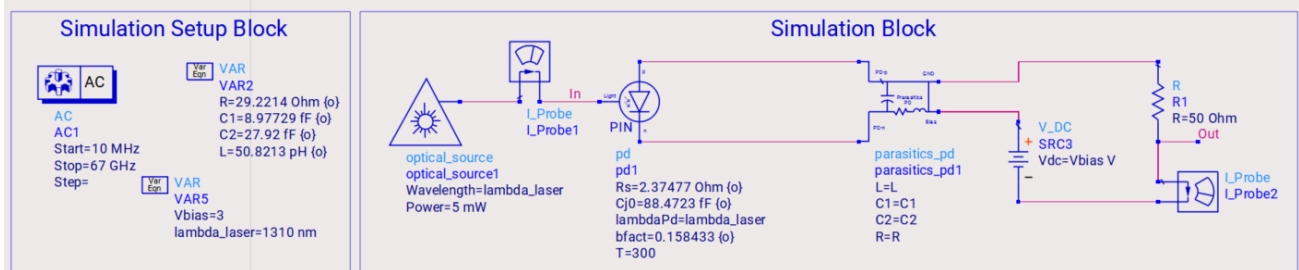


Figure 4. Snippet of the schematic used to perform AC small signal analysis of a PIN photodetector from 10 MHz to 67 GHz. The kind of the simulator and different variables are being set up in the simulation setup block. The circuit is being set up in the simulation block. You can notice that this simulation was performed for a reverse bias of 3 V.

1. Model and Measurement Alignment

To validate our model against actual fabricated results, we import **measurement data** from a previously fabricated chip. This data serves as a benchmark for our simulation, allowing us to assess the model's accuracy and identify areas for parameter tuning. Using the **S_nP block from ADS**, we set the start and stop frequencies to match those in the simulation setup, ensuring alignment across the sampled frequency range. Now running the simulation will result in importing of the measurement data being assigned to **S_nP** block.

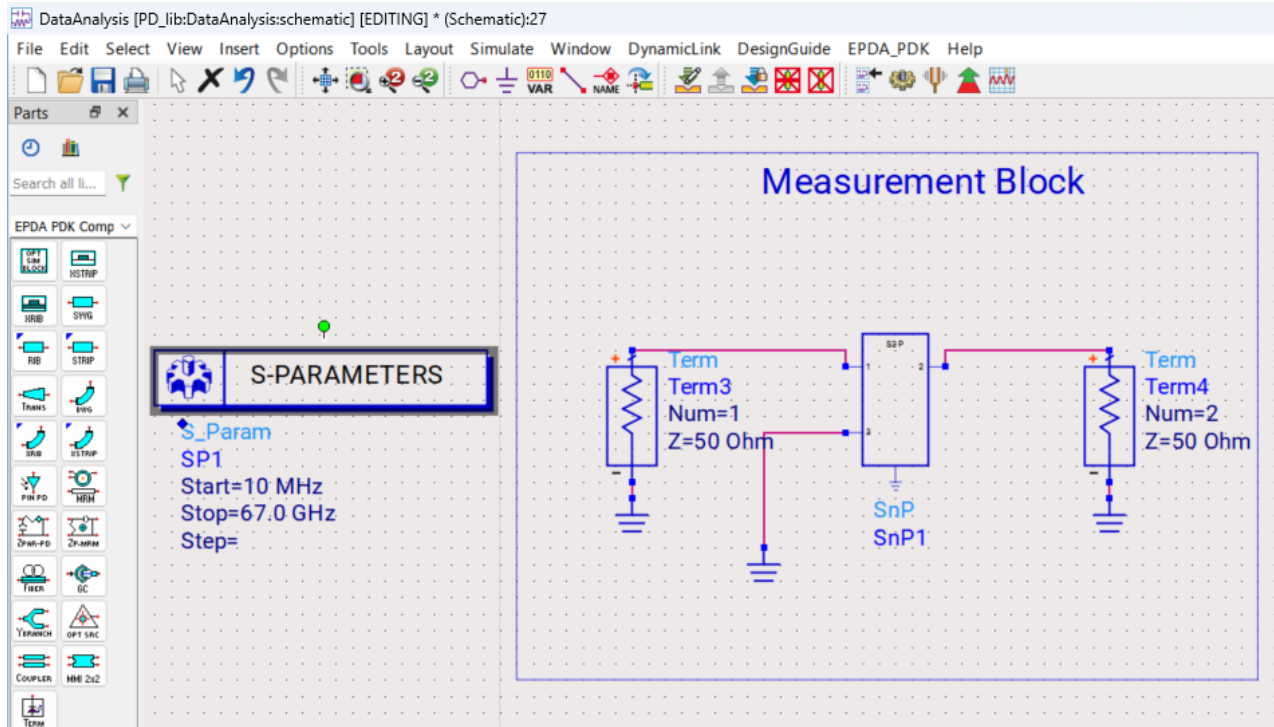
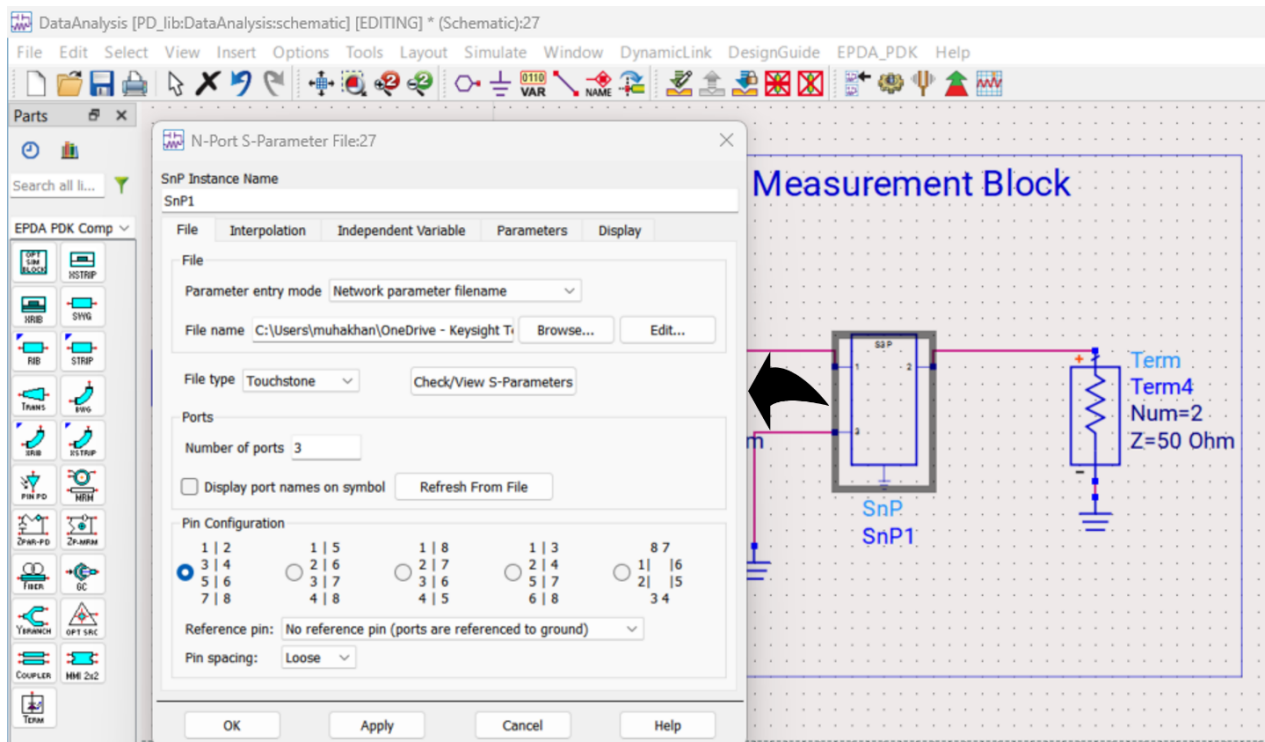


Figure 5. Demonstrating the method of importing empirical data using SnP block. It is recommended to keep the start and the stop frequencies same as used for simulation to keep the sampling frequencies similar.

2. Visualizing measured and simulated Data

Now that the measurement data has been imported, it is time to simulate the PIN photodetector circuit shown in Figure 4. Running the simulation opens a **data analysis window** that can be used to display a comparison between simulation and empirical results. This visualization is crucial as it highlights discrepancies that we can address through tuning, ensuring that the model accurately reflects the behavior of the real device.

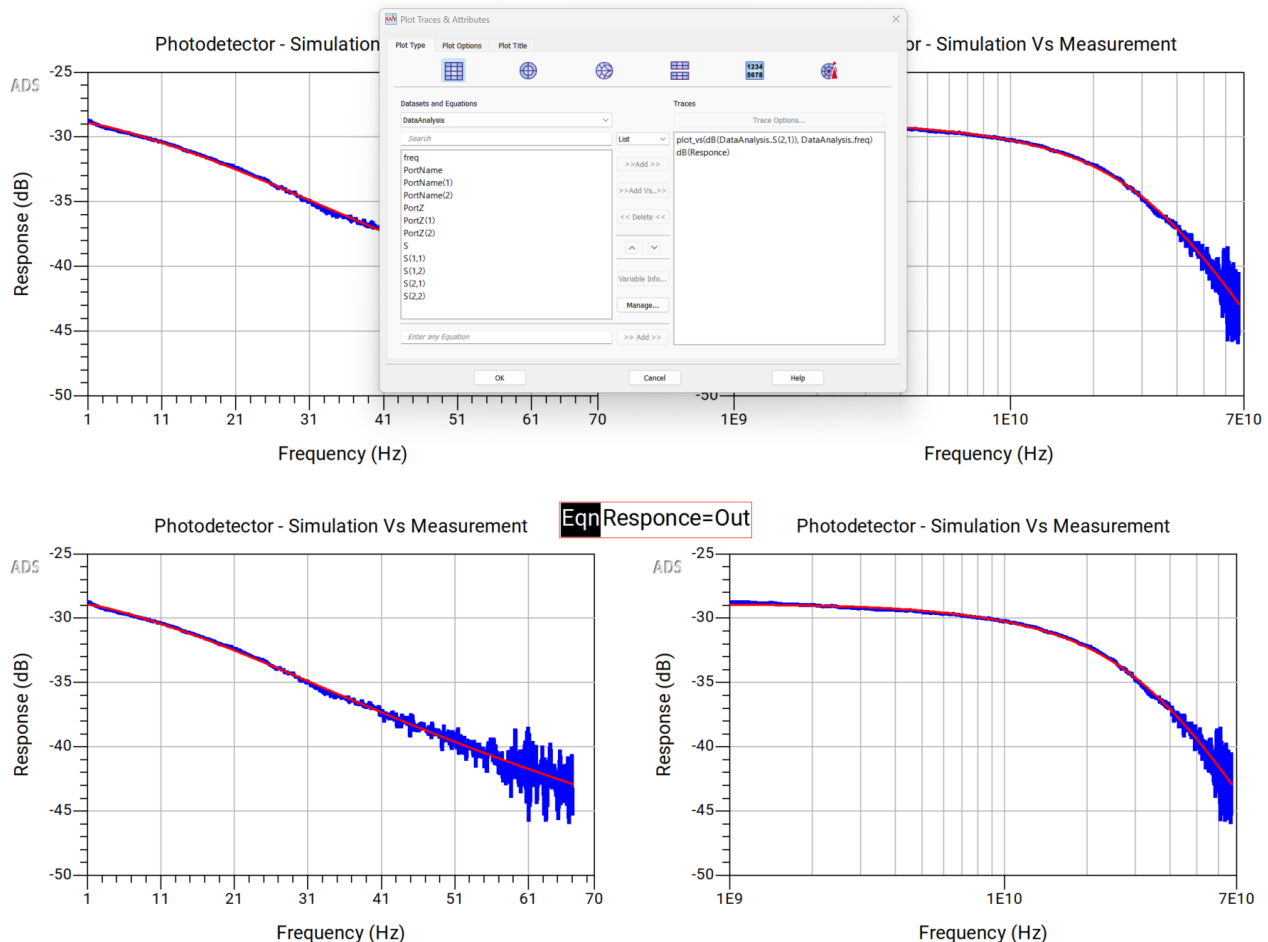


Figure 6. Demonstrating how to plot the simulated and imported empirical data. It can be noticed in the graphs that the simulation outcome is precisely matching with the imported data.

It can be noticed that the simulation results are matching precisely with the measurement data for a broad frequency range from 10 MHz to 67 GHz. This is so because the default values for the design variables have already been tuned to the foundry process that was used to fabricate these chips. Next sections covers how to tune photodetector model to a measurement data.

Model Tuning to a Specific Foundry Process

When adapting the template PDK to a specific silicon photonics foundry, the designer's primary task is to refine the available **design variables** to reflect foundry-specific variations. These adjustments are necessary because each foundry's process can influence factors like doping levels, material properties, and layer thicknesses, which impact device characteristics.

The tuning process involves adjusting the variables associated with the PIN photodetector and its parasitic components. Our goal is to modify these variables such that simulation outputs closely match measurement data. For the sake of understanding, we consider that the measurements data for a chip fabricated through the target foundry is not matching with the simulation, Figure 7.

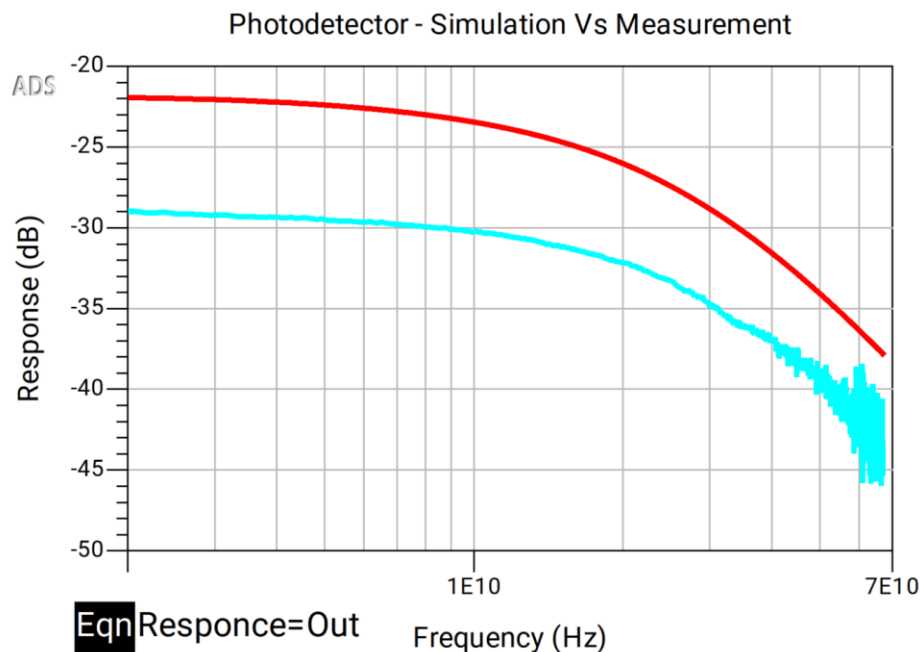


Figure 7. A graph showing a hypothetical situation when the simulation outcome does not match with the imported empirical data as the model has not yet been tuned to the fabrication process.

Using **ADS optimization tools**, we set up an iterative routine that systematically adjusts these variables until the model aligns with the imported empirical data.

Optimization routine setup

To initiate the optimization:

1. **Select Simulation Variables**
2. Navigate to **Simulate** → **Simulation Variables Setup** to identify the parameters for optimization. When fitting measurement data to a photodetector model, variables related to **parasitics**, **series resistance**, **junction capacitance**, as well as **drift** and **diffusion** mechanisms are selected for optimization.

Among these, parasitic-related variables—such as capacitances, inductances, and resistances—are particularly sensitive to changes in the foundry process. These parameters vary based on factors like pad distances, via lengths, and doping concentrations. Thus, optimizing parasitic-related variables is critical when adapting the model to a specific foundry process.

Beyond parasitics, the **series resistance** and **junction capacitance** also significantly influence the photodetector's performance, particularly its bandwidth and response time. Optimizing these parameters ensures the photodetector's RC characteristics are well-tuned for the desired application.

Finally, drift and diffusion-related variables are equally important for accurately modeling the photodetector's behavior. By including these in the optimization process, the model can be precisely tailored to match the characteristics of a given foundry process.

It is essential to define realistic ranges for each variable, as this ensures the optimizer explores plausible values, increasing the likelihood of an accurate fit.

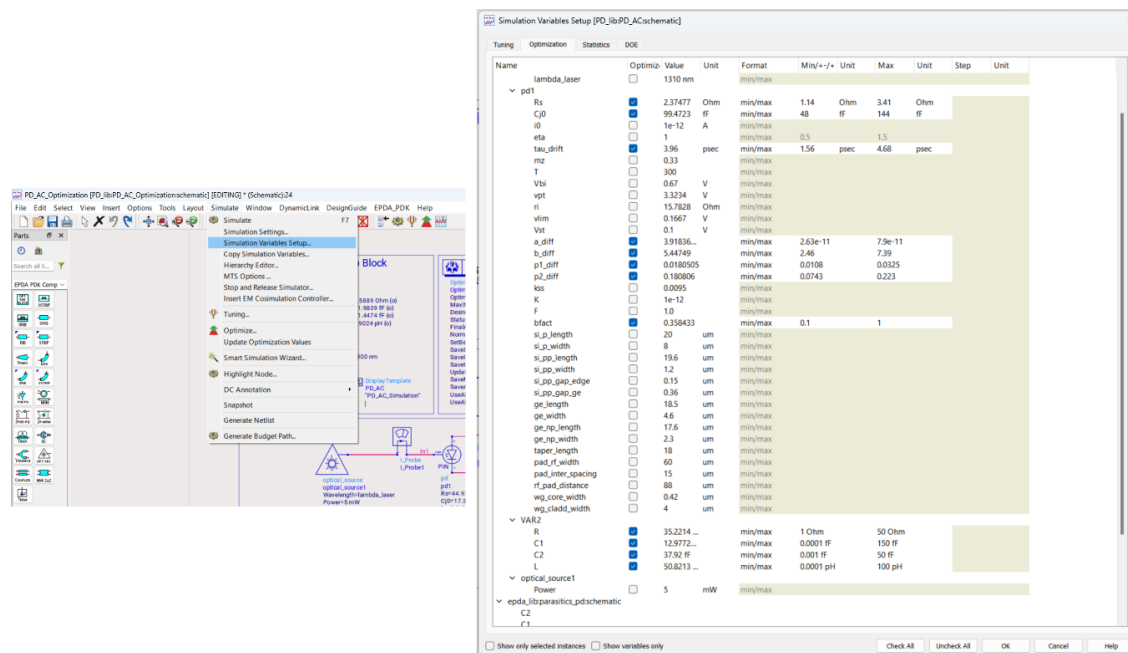


Figure 8. Demonstrating how to select the simulation variables from the optimization tab of the simulation variables setup. A realistic range for these variables should be provided to ensure accurate fit.

3. Define Optimization Goals

We set an optimization goal to align the simulation results with the measurement data. By defining this goal, the optimizer adjusts variables to minimize the difference between the simulated and real data across the chosen frequency range. ADS online documentation covers the details about [defining optimization goals and optimization cockpit](#).

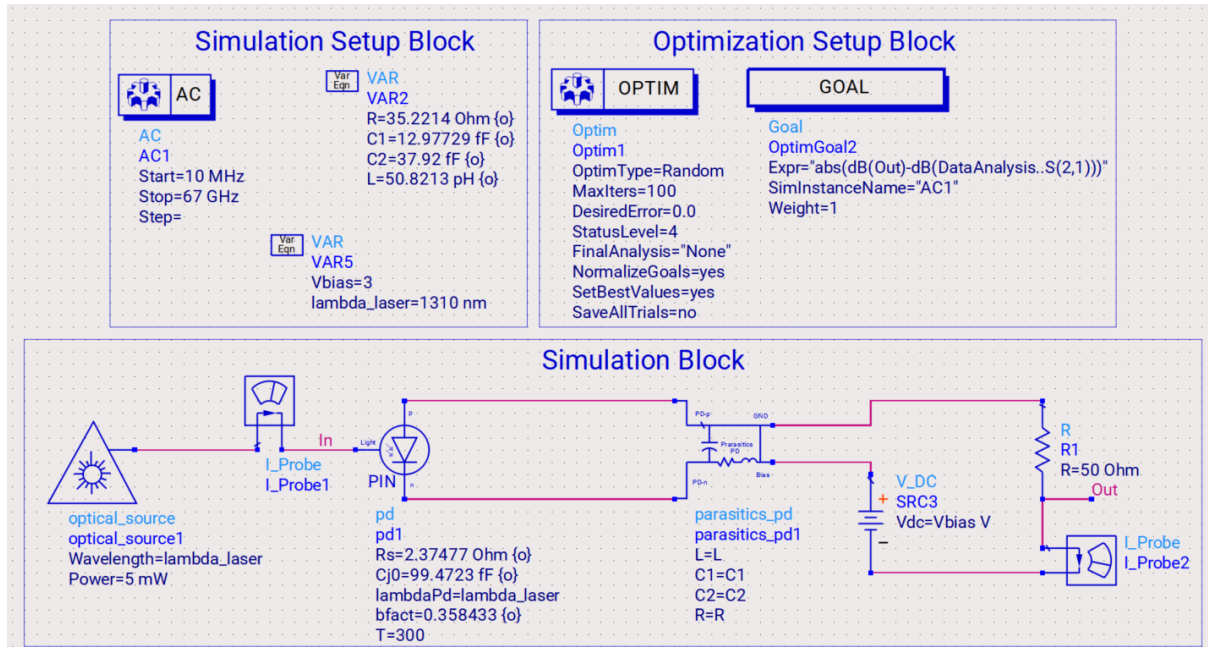


Figure 9. Snippet of the schematic used to optimize the PIN photodetector model to a foundry fabrication process. The Optimization Setup Block is being used to setup the optimization goal and other related parameters e.g. number of iterations and type of optimization routine.

4. Run the Optimization

When the optimization routine is launched, the **optimization cockpit** displays the process, showing each iteration as the algorithm works to converge on an ideal solution. This cockpit provides a live view of how closely the model aligns with measurement data, allowing the designer to observe convergence progress.

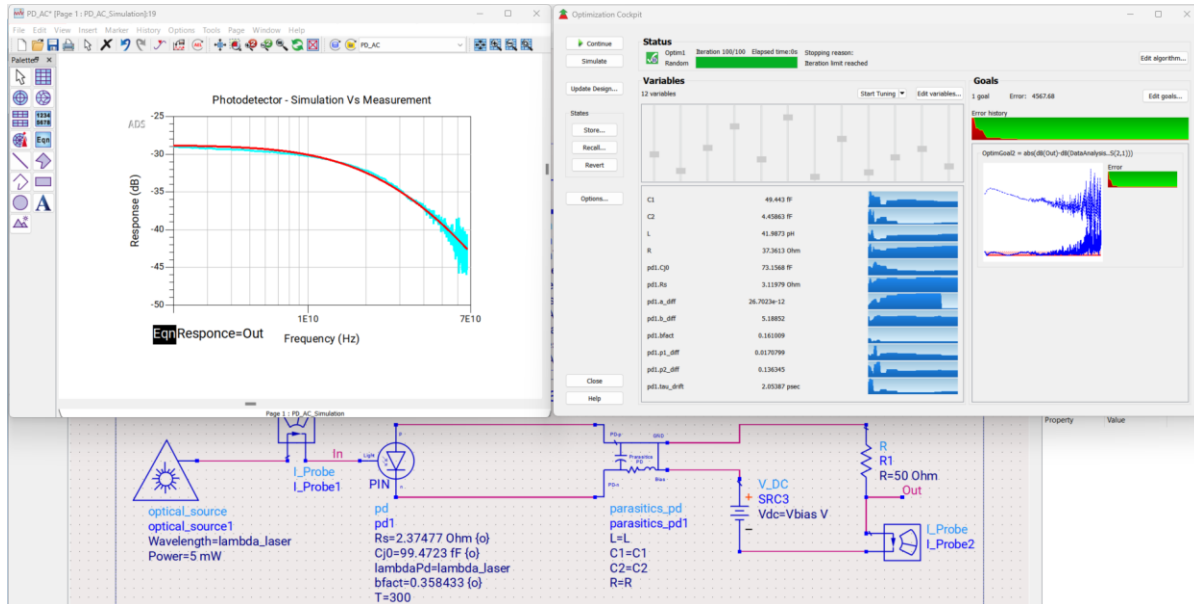


Figure 10. Snippet showing the optimization cockpit and the graph showing a precise match between the simulation and the empirical data in result of the run optimization routine.

Multi-Scenario Verification of Optimized Values

To ensure that the optimized values accurately reflect the characteristics of the foundry, it is beneficial to optimize the model across multiple operating conditions. For instance, by repeating the optimization routine under **three distinct bias voltages**, we can assess whether the variables respond consistently, which is indicative of a stable process.

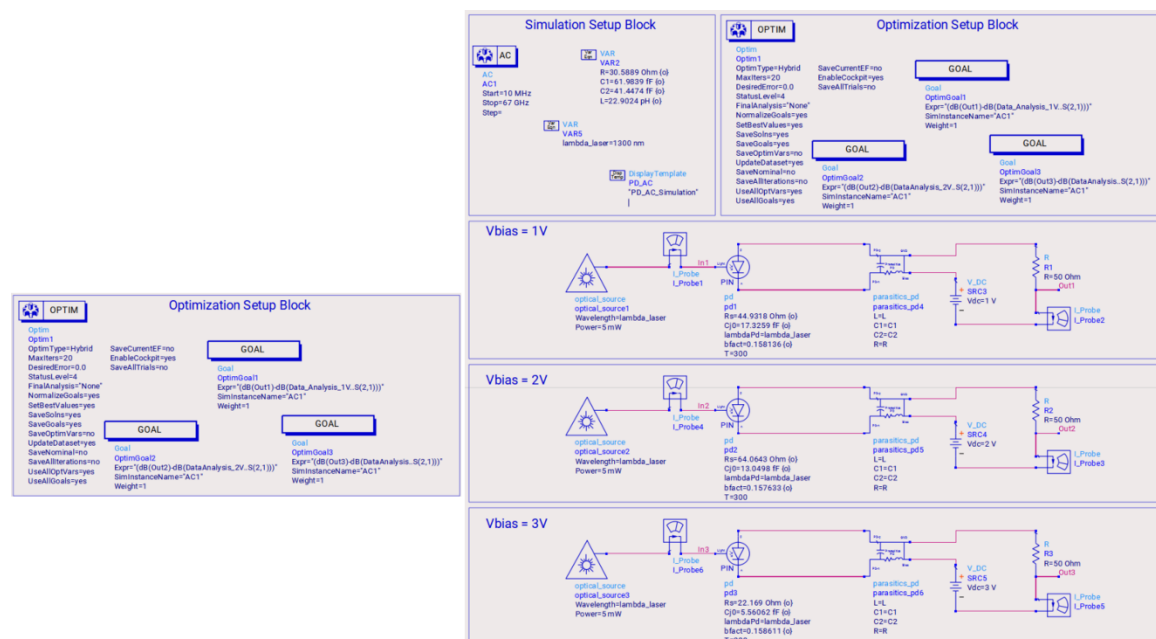
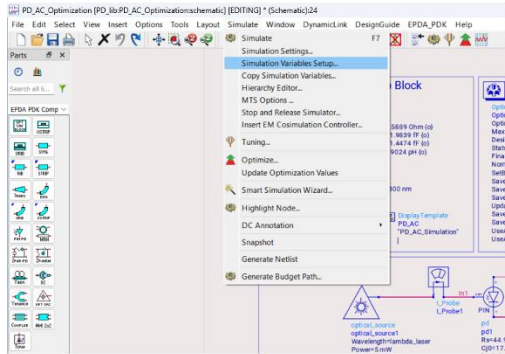


Figure 11. Snippet of the circuits and optimization goals set up for multi-scenario verification using three different bias voltages: 1 V, 2 V, and 3 V.

Conducting multi-scenario verification of the optimized values obtained from a single optimization is crucial. This process confirms that the optimized design variables accurately represent the behavior of the photodetector not just in a single scenario, but across multiple scenarios, such as varying bias voltages. It is understood that parasitic elements are not expected to change significantly with variations in bias voltage. However, the drift and diffusion of carriers within the photodetector are expected to change significantly with different bias voltages.

Therefore, only the core variables directly associated with the photodetector are allowed to vary with the bias, while the parasitic variables remain fixed, Figure 12. This approach ensures that the model accurately reflects the device's behavior while preventing extraneous changes that could compromise the integrity of the tuning process. By applying this multi-scenario verification, we gain confidence in the model's ability to perform reliably under different conditions typical of real-world applications.



Name	Optimize	Value	Unit	Format	Min/+/-	Unit	Max	Unit	Step	Unit
pd3										
Rs	☒	22.169	Ohm	min/max	0.1	Ohm	100	Ohm		
Cj0	☒	3.56062	F	min/max	0.0001	F	1000	F		
theta	☒	1e-12	A	min/max						
eta	☒	1.0		min/max						
tau_drift	☒	3.10644	psec	min/max	1.56	psec	4.68	psec		
mz	☒	0.33		min/max						
T	☒	300		min/max						
Vbi	☒	0.67	V	min/max						
vpt	☒	3.3234	V	min/max						
ri	☒	15.7828	Ohm	min/max						
vlim	☒	0.1667	V	min/max						
Vst	☒	0.1	V	min/max						
a_diff	☒	7.16893...		min/max	2.63e-11		7.9e-11			
b_diff	☒	7.29		min/max	2.46		10			
p1_diff	☒	0.0229092		min/max	0.0108		0.0325			
p2_diff	☒	0.135019		min/max	0.0743		0.223			
kss	☒	0.0095		min/max						
K	☒	1e-12		min/max						
f	☒	1.0		min/max						
bfact	☒	0.158611		min/max	0.0001		1			
si_p_length	☒	20	um	min/max						
si_p_width	☒	8	um	min/max						
si_pp_length	☒	19.6	um	min/max						
si_pp_width	☒	1.2	um	min/max						
si_pp_gap_edge	☒	0.15	um	min/max						
si_pp_gap_ge	☒	0.36	um	min/max						
ge_length	☒	18.5	um	min/max						
ge_width	☒	4.6	um	min/max						
ge_rp_length	☒	17.6	um	min/max						
ge_rp_width	☒	2.3	um	min/max						
taper_length	☒	18	um	min/max						
pad_r1_width	☒	60	um	min/max						
pad_r1_spacing	☒	15	um	min/max						
rf_pad_distance	☒	88	um	min/max						
wg_core_width	☒	0.42	um	min/max						
wg_sladd_width	☒	4	um	min/max						
VAR2	☒	30.5889 ...		min/max	1 Ohm		50 Ohm			
R	☒	61.9839 F		min/max	0.0001 F		150 F			
C1	☒	41.4424 F		min/max	0.001 F		50 F			
C2	☒	22.9024 ...		min/max	0.0001 pH		100 pH			
L	☒									
epda_lib/optical_sourceschematic										
SRCS										
Vdc	☒	0.0	V	min/max						
V_Noise	☒	0	uV	min/max						
VAR1	☒									
polTM	☒	0		min/max						
epda_lib/parasitics_pdschematic										
C2	☒									
C1	☒									

Figure 12. Demonstrating how to select the simulation variables for the multi-scenario verification. It is important to mention here that variables associated to the parasitic block are being kept constant for different bias voltages but photodetectors experiencing different reverse bias voltages are supposed to have different values for the drift and diffusion related variables. So, variables for all three photodetectors are being optimized even though it is not visible clearly from the snippet.

The outcome of the multi-scenario optimization routine can again be visualized using the data analysis window, Figure 13.

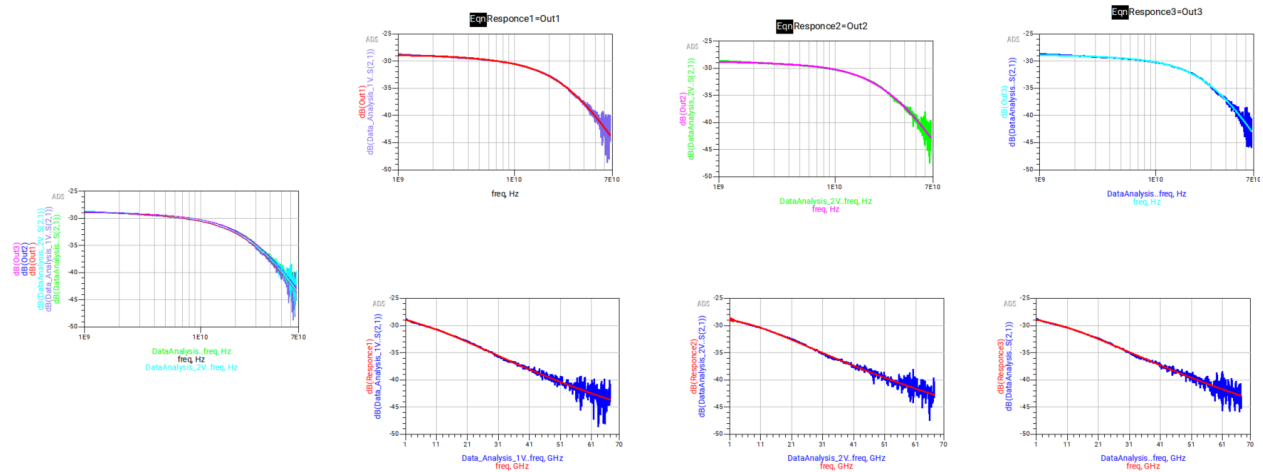


Figure 13. Outcome of the multi-scenario optimization showing very good correlation between the simulated and the imported empirical data even when bias voltage is changing. The correlation is being plotted separately for three values of bias voltages and together (Graph on extreme left) to make sure that everything is being optimized correctly.

Conclusion

In summary, this application note outlines a robust approach to **optimizing a PIN photodetector model** within the Keysight Photonic Designer template silicon photonics PDK for a specific foundry's process. By leveraging the powerful simulation and optimization capabilities of Keysight Photonic Designer, engineers can ensure high accuracy in model outputs, aligning them with empirical data to reflect the true performance of fabricated devices. This fine-tuning process enables designers to confidently customize PICs for varied foundry processes, ensuring that simulation results are not only accurate but also reliable in guiding fabrication decisions.

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