

Practical Modeling of 3D Interconnects with Hatched Ground Planes in Silicon Interposer Bridges, and Flex PCBs

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Introduction

The rapid adoption of generative AI and AI-enabled applications across multiple industries has significantly increased the need for advanced packaging solutions capable of handling demanding AI workloads. As a result, silicon interposers and silicon bridges are being used more extensively in chiplet-based designs, 3D heterogeneous integration (3DHI), and 3DIC technologies ¹.

Manufacturing silicon interposers and bridges, however, introduces several process-related challenges. These include handling very thin substrates and managing gas evacuation during layer build-up. If a continuous solid ground plane is used, trapped gases can lead to defects or delamination. To address this issue, ground planes are commonly patterned using hatch, mesh, or waffle-type geometries, which allow gases to escape while still providing acceptable electrical performance. Comparable constraints are also encountered in flexible PCB technologies, which are widely deployed in mobile and consumer electronics.

While these patterned ground structures solve manufacturing concerns, they complicate electrical analysis. Their complex geometries make accurate signal- and power-integrity modeling more difficult than with solid reference planes. Hatched ground designs can alter transmission-line impedance, increase insertion loss, introduce resonant effects, and modify coupling and crosstalk between adjacent signals. These effects must be properly captured during design to ensure robust electrical performance and avoid unnecessary cost or redesign cycles.

Hatched and Waffled Ground Planes

Representative examples of hatched and waffled ground-plane geometries are illustrated in Figure 1 and Figure 2.

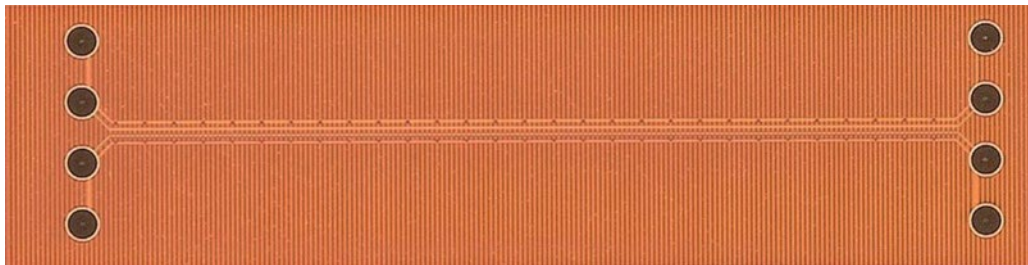


Figure 1. A picture taken from a real wafer of a differential pair on top of a hatched return plane

¹ W. T. Beyene, "Chiplet Technology and Heterogeneous Integration," April 2022. [Online]. Available: https://eps.ieee.org/images/files/enews/EDMS_TC_-_Chiplet_Technology_and_Heterogenous_Integration.pdf. [Accessed 25 November 2025].

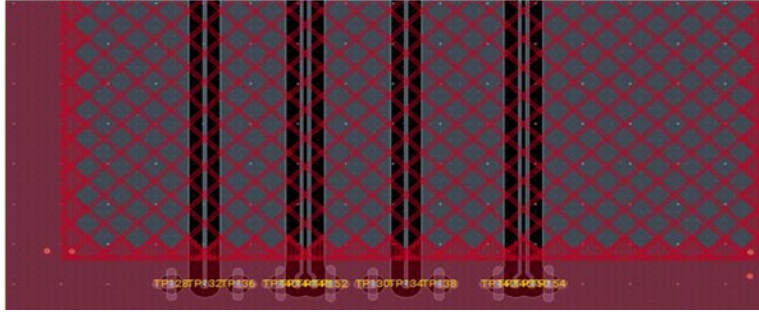


Figure 2. A close-up view of the signal traces and the hatched returned plane geometry.

Mixed-Domain Modeling Approach

Modeling hatched return ground planes requires significantly more computational effort than solid reference planes, and conventional impedance solvers are often inadequate — especially for silicon interposers, silicon bridges, and flex PCBs. While full-wave 3D FEM solvers provide high accuracy, their practical use becomes challenging for designs with lossy silicon, complex multilayer stack-ups, large patterned grounds, or 3D interconnects such as bumps and via transitions, which dramatically increase model size and runtime and often make full-channel simulation impractical.

As a result, mixed-domain (divide-and-conquer) modeling is commonly used, although clear guidelines for its application remain limited.

This application note presents a practical mixed-domain methodology for transmission lines over hatched ground planes in silicon interposers, silicon bridges, and flex PCBs. The approach combines a purpose-built quasi-static 2D field solver for transmission lines with full-wave FEM for critical transitions, delivering high accuracy with greatly improved efficiency. Best practices are provided to help streamline 3D package design without compromising electrical fidelity. The methodology is validated using two test vehicles — a UCle 2.0 silicon bridge and a mobile flex PCB—with simulation results correlated to measurements.

EM Modeling Solutions and Challenges

For high-speed digital designs, full-wave electromagnetic solvers, such as FEM or Method of Moments (MoM) techniques, are widely regarded as the most reliable way to ensure accurate modeling of passive structures and signal channels. Most signal integrity engineers are well acquainted with these tools and use them routinely. Because high-speed digital links involve fast edge rates and wide bandwidths, both transient behavior and frequency-domain transmission characteristics must be captured accurately to achieve first-pass success.

A typical high-speed channel consists of a combination of vias and transmission lines. Vias support BGA connections, layer transitions, and connector interfaces, while transmission lines —

often extending over multiple wavelengths — carry signals between chips or from chips to connectors.

Accurate full-wave modeling requires meshing both the signal conductors and surrounding ground structures, resulting in very large problem sizes and long simulation times ². This computational burden increases further when signals traverse hatched or waffled ground planes, as the detailed ground patterns must also be discretized.

To address these challenges, mixed-domain modeling has become a practical alternative. In this approach, the channel is partitioned into via-transition regions and transmission-line sections. Via transitions, which typically dominate signal integrity degradation, are modeled using full-wave FEM to preserve accuracy. The longer transmission-line regions are handled using computationally efficient quasi-static 2D field solvers.

Different modeling techniques are then applied to each section based on their electrical sensitivity:

- **Via transition regions** are analyzed using full-wave FEM solvers to capture complex 3D electromagnetic effects with high accuracy.
- **Transmission-line regions**, which are typically longer and more uniform, are modeled using computationally efficient methods such as specialized quasi-static 2D field solvers.

Unlike the approach where multiple EM techniques are combined within a single solving algorithm ³, this methodology constructs the complete channel model by cascading the S-parameters generated for each individual section. While this strategy significantly reduces simulation cost, some designers question whether it may compromise overall accuracy.

The following examples demonstrate that, when applied correctly, this mixed-domain approach provides an effective and accurate solution for high-speed digital channel modeling.

Single-Ended Transmission Lines with Via Transitions

The example shown in Figure 3 consists of a single-ended transmission line with an overall length of approximately 3 inches and includes two different via transition types: one associated with a BGA (Ball Grid Array) interface and the other connected to a DRAM (Dynamic Random-Access Memory) device.

The structure was analyzed using the mixed-domain modeling methodology described earlier. To reduce modeling complexity, the transmission-line portion was represented using only two quasi-static 2D field solver models. Nonessential geometric details such as routing bends, corners, and meander patterns were intentionally omitted. In contrast, each via transition was modeled in full three-dimensional detail using a FEM-based electromagnetic solver to accurately capture the localized discontinuities.

² H. L. H. Stephen H. Hall, *Advanced Signal Integrity for High Speed Digital Designs*, John Wiley & Sons, Inc, 2009.

³ Z. L. L. R. W. a. S. H. Z. Chen, "A mixed-domain modeling method for RF systems," in *IEEE Custom Integrated Circuits Conference*, San Jose, 2015.

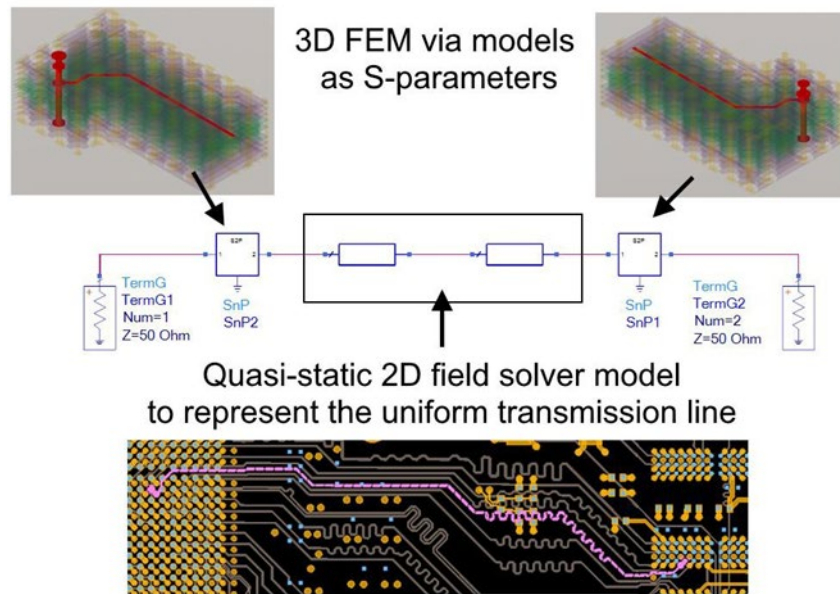


Figure 3. An S-parameter simulation schematic setup of a mixed-domain simulation approach.

A comparison between simulated and measured results is shown in Figure 4. The analysis yields a Mean Similarity Metric of -14.2 dB for S_{11} and -11.9 dB for S_{21} . These metrics are based on the IEEE P370 Error Vector Method and Similarity Metric definition ⁴, which provides a quantitative measure of agreement between two sets of S-parameters over frequency. Reference ranges and their practical interpretation are summarized in Table 1, with a more detailed discussion of the Mean Similarity Metric included in the appendix.

As indicated in Table 1, both Mean Similarity Metric values are well below -5 dB, corresponding to a strong correlation between the mixed-domain simulation results and the measured data. This level of agreement is particularly noteworthy given the simplified treatment of the transmission-line geometry, as well as the presence of normal fabrication variability and measurement uncertainty.

⁴ IEEE Standard for Electrical Characterization of Printed Circuit Board and Related Interconnects at Frequencies up to 50 GHz, IEEE Std 370-2020.

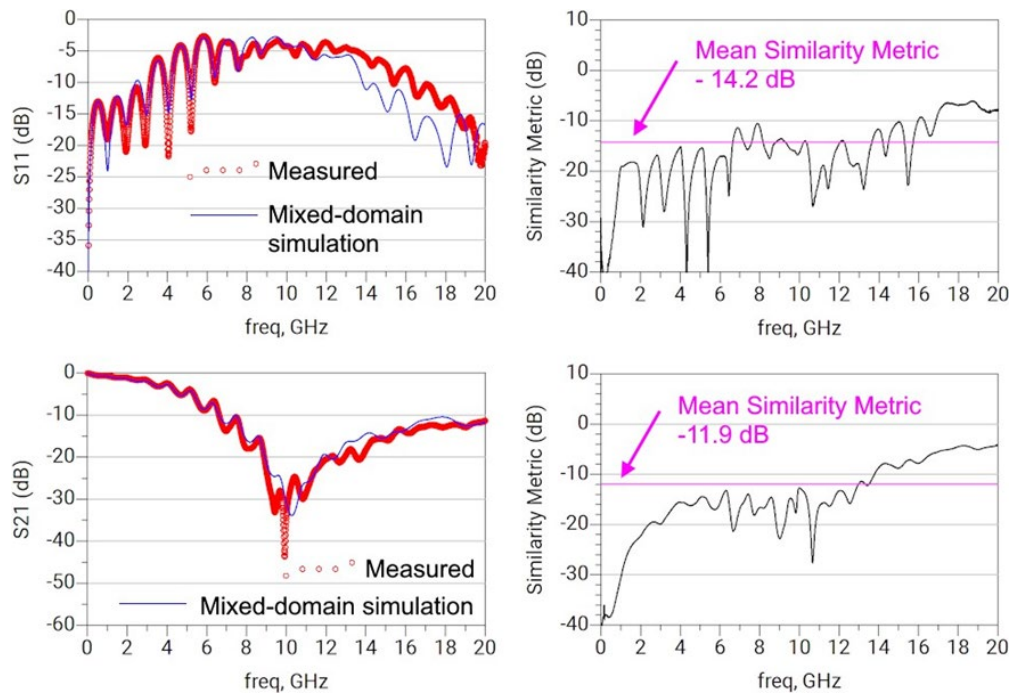


Figure 4. A comparison between mixed-domain simulation and measurement data indicates a good qualitative correlation between the measured and simulated results.

Mean Similarity Metric (dB)	Qualitative Interpretation	Description
Less than -300 Db	Perfect	Equivalent to comparing two identical simulated transmission-line S-parameters
Less than -50 dB	Excellent	Similar to repeated measurements of the same 20 dB attenuator using the same setup
Less than -20 dB	Very Good	Comparable to measuring a Beatty standard with different connector families
Less than -5 dB	Good	Similar with comparing two simulated Beatty standards, where one has a width and length 1.5% larger than the other
Less than 0 dB	Fair	Similar to comparing two simulated Beatty standards, where one has a width and length 3% larger than the other
Greater than 0 dB	Poor	Worse agreement than the 3% variation case

Table 1. A list of reference values for the Mean Similarity Metric, its interpretation, and descriptions.

Figure 5 compares the eye diagrams generated from measured channel data with those from the mixed-domain channel model for a memory application.

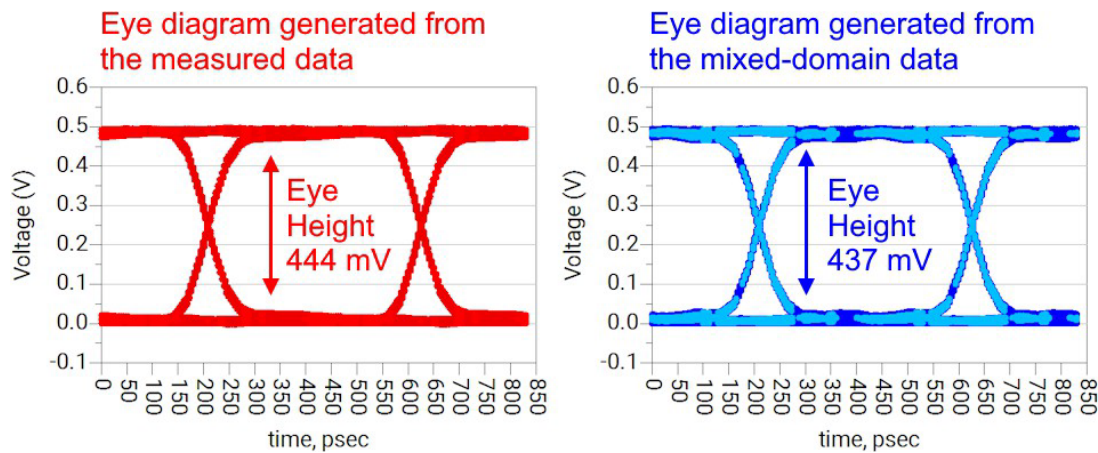


Figure 5. An eye diagram comparison between the mixed-domain approach and measured eye diagram data. The eye height difference is 7 mV. The mixed-domain eye height (437 mV) is within 2.1% of the eye height generated from the measured data (444 mV).

Differential Transmission Lines with Via Transitions

Figure 6 presents results for a differential transmission channel, showing trends similar to the single-ended case. Despite the transmission line being long and including multiple meanders, it was represented using a simplified quasi-static cross-sectional differential transmission model. The via transition was modeled in full 3D using a FEM-based solver to accurately capture localized discontinuities.

Figure 7 provides an example comparison of the differential insertion loss along with the corresponding Similarity Metric. Table 2 summarizes the key parameters that were evaluated. Overall, the mixed-domain simulated S-parameters show strong agreement with the measured data, confirming the effectiveness of the modeling approach even for complex differential channels.

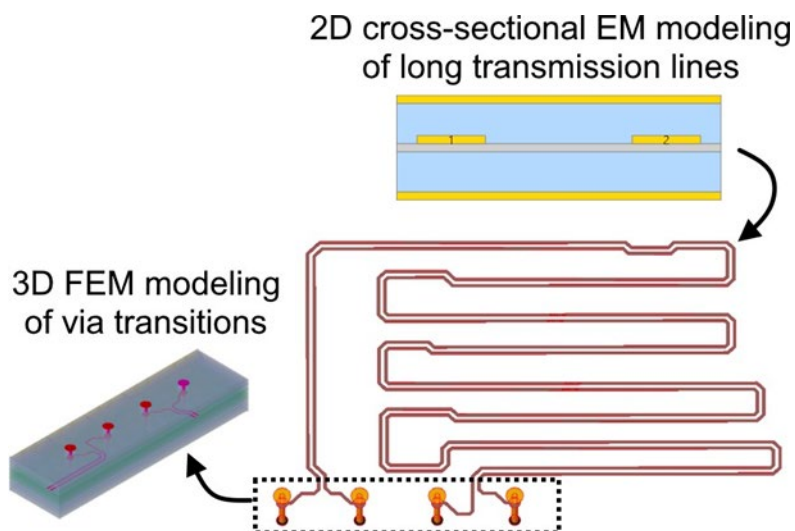


Figure 6. A differential pair example setup of the mixed-domain approach

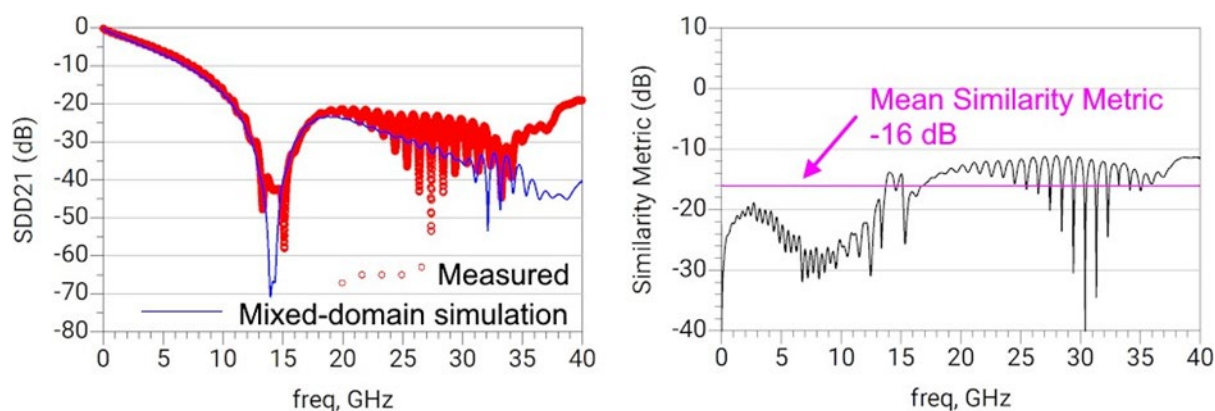


Figure 7. The measured eye diagram and the mixed-domain simulated eye diagram show differences within 2.1% of eye height.

Parameters to Compare	Result of Comparison
SDD11	Mean Similarity Metric: -10.2 dB (Good match)
SDD21	Mean Similarity Metric: -16.0 dB (Good match)
SCC11	Mean Similarity Metric: -10.1 dB (Good match)
SCC21	Mean Similarity Metric: -16.6 dB (Good match)
Eye Height	Perfect difference: 2.1%

Table 2. Comparison Results between Measured Data and Mixed-domain Simulation

Practical Benefits of the Mixed-Domain Modeling Approach

In high-speed digital applications, maintaining clean signal integrity is critical, and eye-diagram openings are often used as a key performance metric. The mixed-domain modeling methodology proves highly practical in this context, delivering the accuracy needed for design verification while significantly reducing computational effort and simulation time.

Table 3 provides several representative examples. Here, Full FEM refers to conventional full-wave finite element simulations, Quasi-static indicates the use of simplified transmission-line or bus models, and FEM Transition represents the sections of the design where signal transitions are modeled using full 3D FEM within the mixed-domain framework.

As the table demonstrates, the mixed-domain approach achieves substantial reductions in both simulation runtime and required computational resources. Equally important, it allows engineers to efficiently analyze complex, high-bandwidth bus structures without being constrained by solver capacity or encountering simulation failures.

Structure	FEM Simulation Resources Required	Mixed-Domain Simulation Resources Required	
		Quasi-Static	FEM Transition
Simplified 2000um single stripline with hatched ground planes (rectangular hatch) in a 4 RDL layer silicon bridge	Memory usage: 100GB		
	Simulation time: 2hr 14m	<1 min	
	On a server	On a laptop	NA
Simplified 1000um single microstrip with hatched ground planes (rectangular hatch) in 4 RDL layer silicon bridge	Memory usage: 340GB		Memory usage: 40GB
	Simulation time with HPC: 7hr 30min	<1 min	Simulation time with HPC 30 min
	On a server		On a server
Differential 2000um stripline with hatched ground planes in 4 RDL layer silicon bridge	Failed due to memory limit	<2 min	Memory usage: 55GB
			Simulation time: 4hr
			On a laptop

Best Practices for the Mixed-Domain Modeling Approach

After demonstrating the effectiveness of the mixed-domain modeling methodology, a key practical consideration is determining where to partition the model — specifically, which regions should be analyzed using a full-wave FEM solver and which can be handled by a quasi-static 2D field solver. While no universal rule applies to all designs, several general guidelines can help ensure accurate and reliable results.

First, the regions where signal transitions or mode conversions occur should be included as much as possible within the full-wave FEM domain. These areas are typically the most sensitive, as they contain discontinuities and parasitic effects that must be captured with high fidelity to avoid missing unintended signal behavior.

Second, domain boundaries should not be placed in regions where the electromagnetic fields have not yet reached a stable propagation mode. Introducing a boundary before the signal has fully settled into a transmission-line mode can reduce accuracy and may produce inconsistent or non-physical simulation results.

Third, careful attention must be paid to the ground return path at the interface between domains. Because S-parameters represent voltage differences between signal and reference conductors, the reference (negative) nodes in each domain must share the same electrical potential when cascading S-parameter blocks. Failing to maintain this consistency can introduce errors when the models are combined.

Silicon Interposers and Bridges with Hatched Ground Planes

The continued growth of High-Performance Computing (HPC) systems places increasing demands on data bandwidth and latency between processors and High-Bandwidth Memory (HBM). Traditional two-dimensional packaging approaches are limited by I/O density and interconnect length, making it difficult to meet these requirements. As a result, 2.5D heterogeneous integration has gained traction as an effective packaging strategy, enabling multiple dies to be integrated side by side. Despite its advantages, challenges related to cost optimization and long-term reliability remain key areas of focus.

Silicon Interposers and Silicon Bridges

A silicon interposer acts as an intermediate substrate that supports multiple dies on a common platform and provides signal and power routing through fine-pitch redistribution layers (RDLs), as shown in Figure 8. While silicon is the most common material, organic and glass interposers are also used in certain applications. Electrical connectivity between wiring layers is achieved using Through-Silicon Vias (TSVs), and additional components such as Deep-Trench Capacitors (DTCs) can be integrated when required.

Silicon bridges enable fine-pitch die-to-die interconnects by embedding a small silicon die only in the localized region between adjacent chips, as illustrated in Figure 9. Unlike full interposers, bridges typically do not require TSVs and confine dense routing to limited areas, providing advantages in both cost and manufacturing yield. However, mechanical stress caused by Coefficient of Thermal Expansion (CTE) mismatch between silicon and organic substrates must be carefully managed. Common mitigation techniques include underfill materials, structural reinforcement, or, in some cases, the use of organic bridge alternatives.

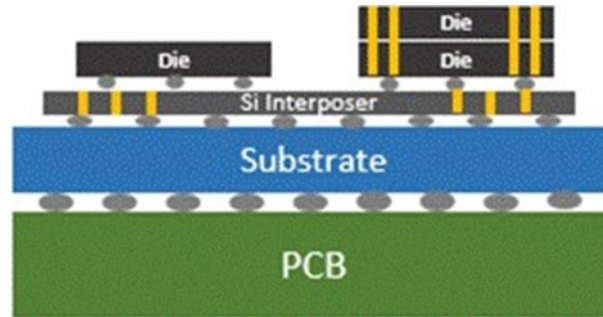


Figure 8. Conceptual cross-section of Silicon Interposer (2.5D).

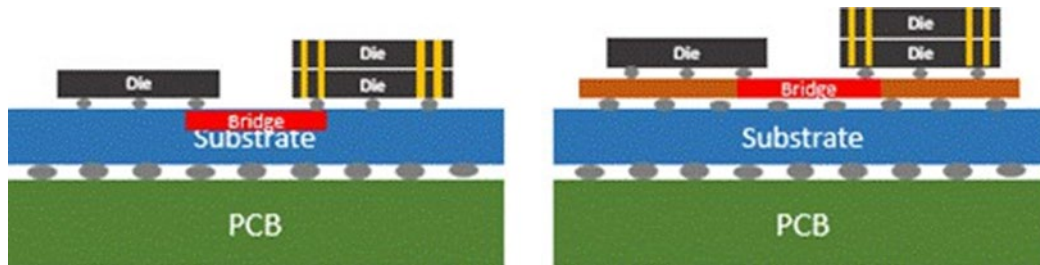


Figure 9. Conceptual cross-section of Embedded Silicon Bridge (2.1D & 2.3D).

A **hatched ground (Hatch GND)** replaces a continuous ground plane with a patterned lattice, reducing copper coverage to relieve mechanical stress and package warpage caused by CTE mismatch. The reduced metal area also lowers parasitic capacitance to signal traces, improving impedance control and minimizing crosstalk, while enhancing thermal dissipation and underfill flow during assembly.

These benefits come with trade-offs: the patterned return path increases inductance, so trace width and hatch pitch should be optimized for the operating frequency. Critical regions may be reinforced with via stitching or localized solid ground areas. In silicon interposer and bridge designs, Hatch GND is applied selectively, typically under fine-pitch routing or directly beneath the bridge, depending on thermal, mechanical, and signal integrity requirements.

Interposer and bridge technologies are commonly used to connect AI and HPC accelerators — such as GPUs, TPUs, NPUs, and FPGAs — to High-Bandwidth Memory (HBM), enabling ultra-high data rates and low latency. They are also employed in chiplet-based CPUs and SoCs, where EMIB or organic bridge structures provide fine-pitch die-to-die connections while balancing

performance, yield, and cost. Additionally, these technologies support high-bandwidth memory interfaces in networking systems, such as links between switch or router ASICs and HBM, improving overall system throughput (Figure 10).

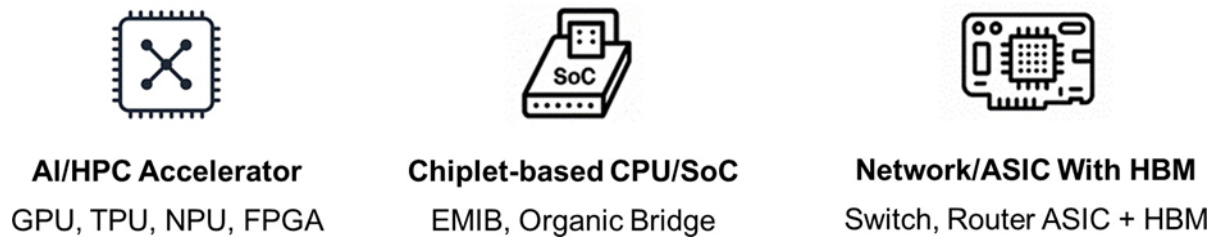


Figure 10. A summary of the bridge and interposer technologies and their applications.

Flex PCBs with Hatched Ground Planes

A flexible Printed Circuit Board (FPCB) consists of conductive copper layers laminated onto a flexible dielectric substrate, most commonly polyimide. FPCBs are valued for their thin form factor, low mass, and ability to support three-dimensional routing through bending and folding, making them well suited for mobile and wearable electronics. Their multilayer construction also allows many standard PCB design and fabrication practices to be applied with minimal adaptation.

Ongoing industry pressure to reduce overall FPCB thickness has driven the use of thinner dielectric layers, which complicates the use of a continuous solid ground plane as a signal reference. As the separation between signal traces and the reference plane decreases, the characteristic impedance can drop substantially, creating impedance discontinuities when the FPCB is considered as part of the full system channel. To compensate for this effect, hatched ground planes are increasingly adopted as the reference layer for high-speed signals in FPCB designs.

Use Cases and Modeling Challenges

Hatched ground planes are widely used in FPCBs, particularly in hinge regions of foldable and flip phones, where high-speed signaling and reliable power delivery must be maintained under severe mechanical and environmental stress. These designs must withstand tens of thousands of folding cycles, as well as potential exposure to dust and moisture, making signal integrity under mechanical deformation a key consideration.

In conventional smartphones and tablets, FPCBs connect peripherals such as cameras, displays, and USB Type-C interfaces to the mainboard. While these applications are mechanically less demanding, they introduce significant electromagnetic challenges. The coexistence of multiple antennas for 4G/5G, Wi-Fi, and GPS creates complex RF environments, and hatched ground planes can distort return-current paths and radiation patterns. This may lead to EMI/RFI issues such as antenna desense or signal degradation caused by antenna transmit coupling.

FPCBs are also essential in wearable devices, where flexibility is required to conform to the human body. In these applications, patterned ground structures often necessitate full 3D EM analysis to capture electromagnetic behavior accurately. However, such simulations are computationally expensive and slow design iteration, driving the need for a 2.5D mixed-domain modeling approach that balances accuracy with efficiency.

From a modeling standpoint, flex PCB cross sections introduce additional uncertainty. Although simulations assume ideal geometries, actual dielectric thickness and material deformation can vary significantly, as illustrated in Figure 11, further complicating accurate electrical characterization.

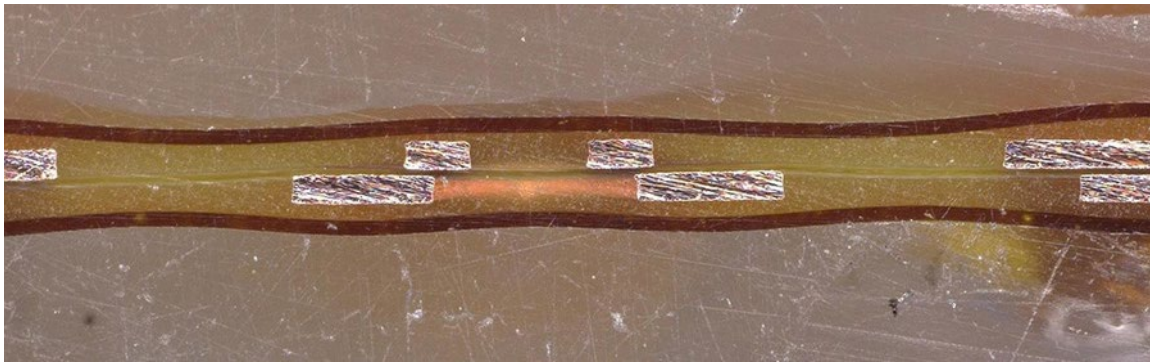


Figure 11. A cross-sectional view of a flex PCB.

Fabrication of a Silicon-Bridge Interconnect Using BEOL Cu Damascene

The silicon-bridge (Si-bridge) interconnects used in this paper were fabricated using a standard Back-End-of-Line (BEOL) copper damascene process. The device comprises four metal layers (including ground). The top pads are connected to Metal-4 through vias.

Process Flow

1. ILD1 deposition (TEOS SiO_2 , CVD)
2. M1 lithography (i-line stepper) → M1 trench etch (dual-damascene etch)
3. Barrier/liner deposition (Ti/TiN, sputter)
4. Cu electroplating (fill) → Cu CMP
5. ILD2 deposition → Via1 + M2 pattern/etch (dual-damascene)
6. Barrier/liner deposition (Ti/TiN) → M2 Cu electroplating → Cu CMP
7. Repeat dual-damascene stack-up for M3 and M4
8. Top dielectric deposition → Top-via/opening etch → Pad formation

Unit Processes Used

- Dielectrics: TEOS SiO₂ by CVD
- Barrier/Liner: Ti/TiN by sputtering
- Lithography: i-line stepper
- Etch: Dual-damascene dry etch for vias/trenches in SiO₂
- Metallization: Cu electroplating and CMP

Inline Metrology

Critical Dimension (CD) and metal thickness were monitored on 1 μm line-width patterns (TEG designs may employ different target widths). Table 4 and Table 5 summarize representative in-line data.

	Target	Mean	3 σ
Line Thickness	1 μm	1.13 μm	0.249

Table 4. Metal Line Thickness Data

Layer	Target	In-Line Measurement	
		Mean	3 σ
Metal1	1 μm	1.19 μm	0.058
Metal2	1 μm	1.21 μm	0.138
Metal3	1 μm	1.19 μm	0.072
Metal4	1 μm	1.15 μm	0.062

Table 5. Metal Line Critical Dimension (CD) Data

Cross-Sectional Characterization

Figure 12 shows a representative cross-sectional SEM photo of the fabricated Si-bridge (vertical cut). Comparison of the SEM with the in-line data indicates minor deviations from initial design intent, attributable to cumulative process tolerances (lithography bias, dielectric etch profile, ECD fill/CMP dishing/erosion). These variations are within typical BEOL process windows and will be accounted for in subsequent electrical correlation.

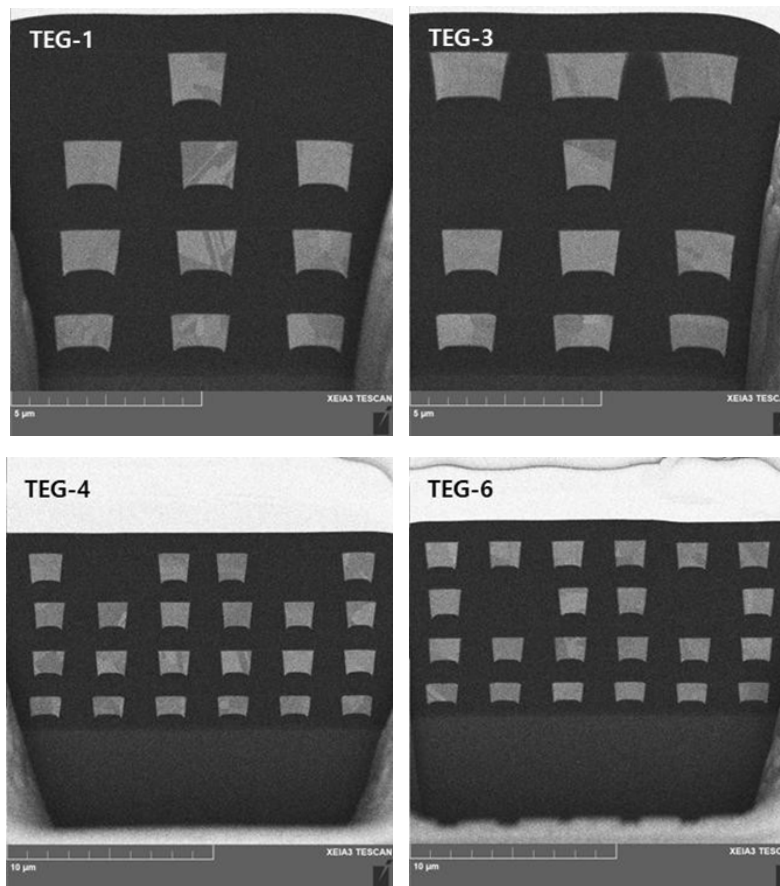


Figure 12. A collection of cross-sectional SEM photos of the Si-bridge. Photos from four different Test Element Group (TEG) were taken.

Silicon Bridge TEG (Test Element Group) Designs

To validate the mixed-domain modeling approach, both hatched-ground transmission lines and via structures were characterized. The hatched geometries were implemented based on transmission-line widths and aligned with manufacturing design rules. Via layouts were optimized to study impedance discontinuities and coupling, while probe pad size and probe-tip pitch were carefully selected to ensure accurate correlation between simulation and measurement.

As shown in Figure 13, the TEG structures were organized into four groups:

- **2000 µm Transmission Line Group:** Single-ended and differential microstrip and stripline structures, with additional 2× and 5× differential spacings to evaluate coupling.
- **1000 µm Transmission Line Group:** Identical configurations to the first group, but with shorter line lengths.
- **Via Transition Group:** Structures with varying via spacings and transition geometries to assess via-related signal integrity effects.
- **UCle Design Group:** Layouts based on the UCle standard package bump map to represent realistic high-speed interconnect scenarios.

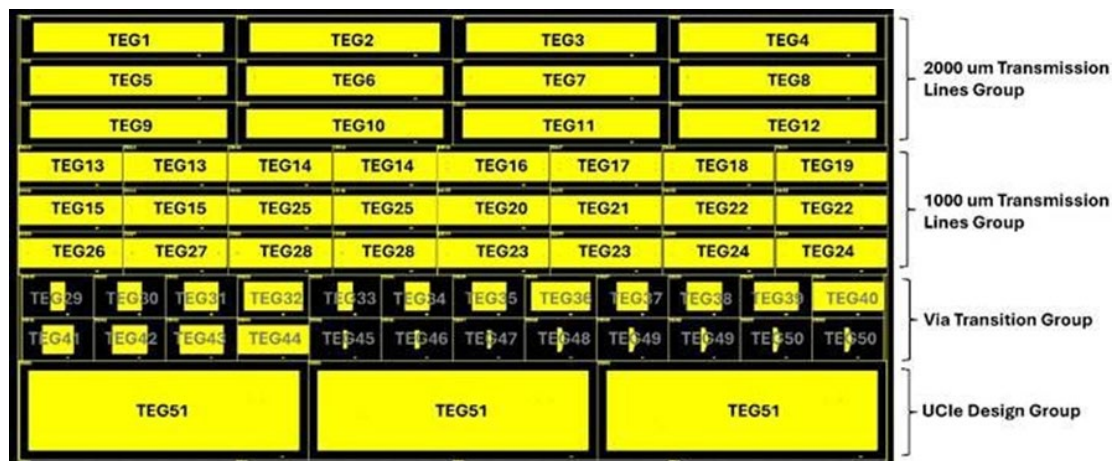
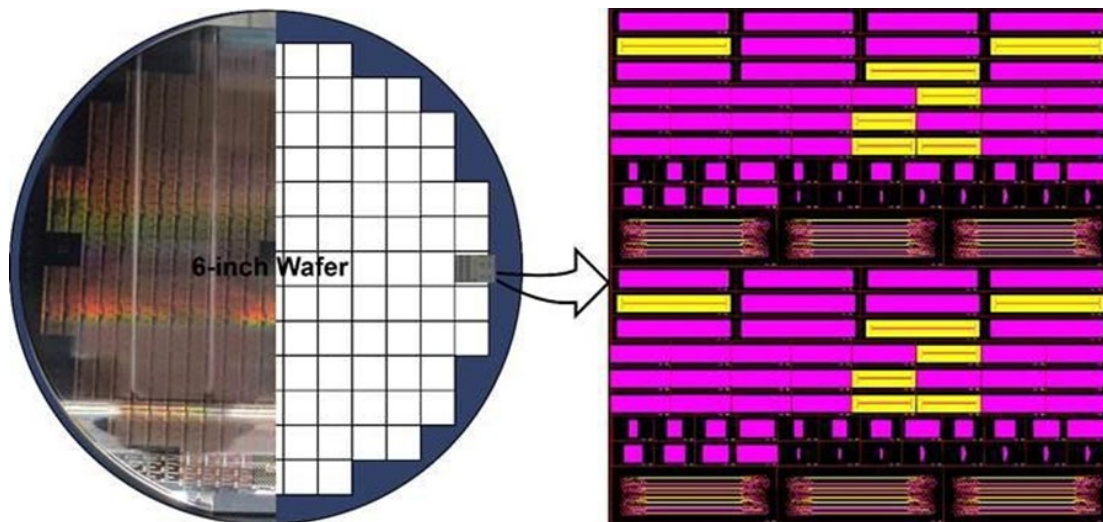


Figure 13. The four TEG design groups and their locations on a 6-inch wafer.

Silicon Bridge TEG Measurements

Probe-based measurements on the Silicon Bridges are challenging because of several issues:

1. 50-100 μm pitch and 25-75 μm pad sizes make it difficult to land the probes and get sufficient tip scrub,
2. The insulating layers are often thin and brittle, so they tend to break under typical probe pressure (~1 ounce), and
3. The pads are often metalized with aluminum, which often causes problems for copper-based probe tips.

It pays to be proactive in tackling these issues to avoid measurement problems. Therefore, our design was set at 75 μm pitch for more room for probing, and the probing pads were gold-plated to aid probe contact. Before starting the measurements, we tested the Silicon Bridge dielectrics by

landing a probe directly on the surface, applying standard probe force, and checking for fracturing under a microscope – no fracturing was observed.

Figure 14 shows an example measurement setup. The measurement setup for the Silicon Bridge measurements was:

- GTL-4040 probing platform with two positioners and a six-inch wafer chuck
- N5227A Precision Network Analyzer
- 40A-GS-80-DP & 40A-GS-55-D-55-N probes (qty=2 each)
- GTL-1001 & CS-3-50 calibration substrates
- Short-Open-Load-Reciprocal (SOLR) calibration to the probe tips

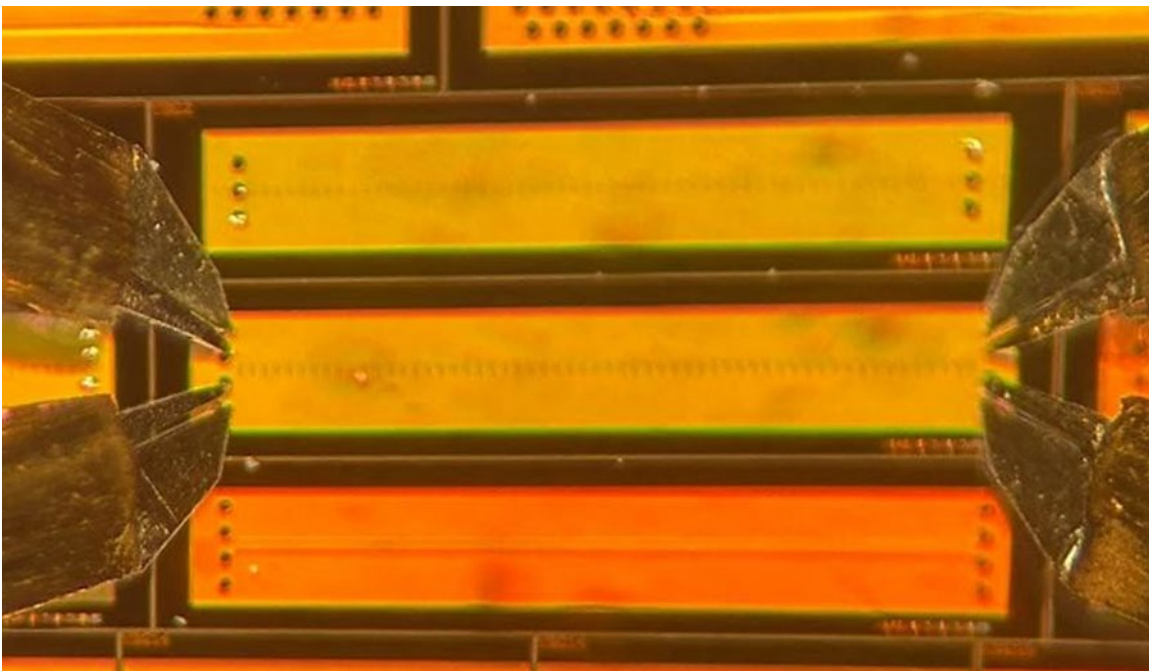


Figure 14. A photo of the measurement setup.

The SOLR calibration method was used because it calculates the loss of the THRU standard in real time, unlike SOLT (Short-Open-Load-Thru), which assumes a lossless THRU. This approach helps prevent passivity errors and was validated by measuring both the calibration THRU and a known coplanar waveguide. Some measurements showed contact resistance, which was minimized by probing at the inner edges of the pads for a cleaner scrub.

Silicon Bridge Validation

This was performed by comparing mixed-domain simulation results with measured data from several TEG structures. The pad-via-feed regions were modeled using full-wave FEM for high accuracy, while the transmission lines were modeled with Keysight EDA Chiplet 3D Interconnect

Designer. Due to symmetry, the FEM portion was simulated once and reused across identical sections.

2000 μm Length Stripline with Hatched Ground

A representative case, **TEG2**, features a 2000 μm stripline with hatched ground: "Probe Pad – Stacked Via – Stripline on 2nd Layer with Hatched Ground – Stacked Via – Probe Pad" (Figure 15). The mixed-domain modeling was applied as follows:

- **Via transitions** were analyzed using full-wave FEM to capture critical discontinuities.
- **Stripline with hatched ground** was modeled using the quasi-static 3D interconnect solver.

Figure 16 compares the S-parameters and the Mean Similarity Metric between simulation and measurement, yielding -18.9 dB (S11) and -17.1 dB (S21). These results demonstrate that the mixed-domain approach accurately predicts the behavior of silicon bridges with complex hatched ground planes.

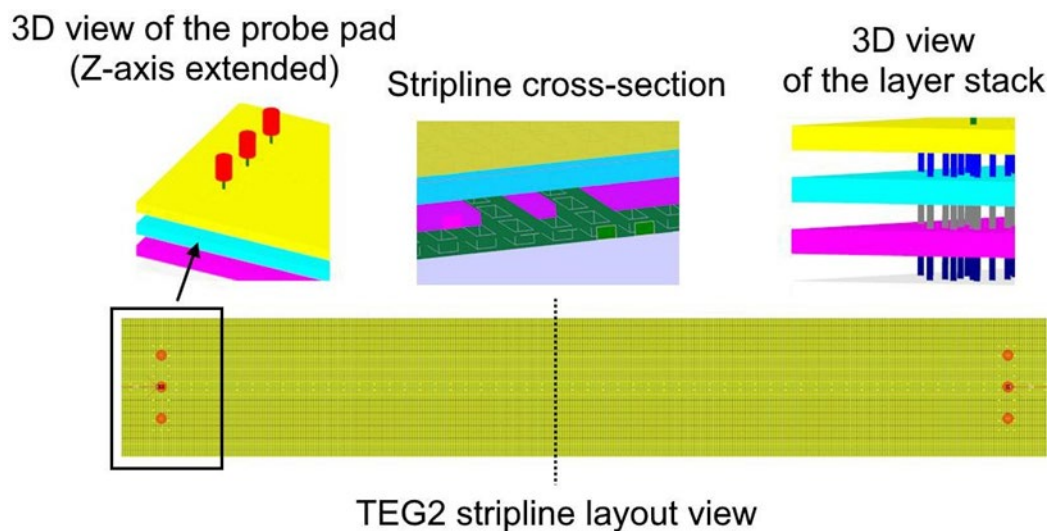


Figure 15. A TEG2 stripline layout representing the test case: probe pad – stacked via – stripline on the 2nd layer with hatched ground – stacked via – probe pad

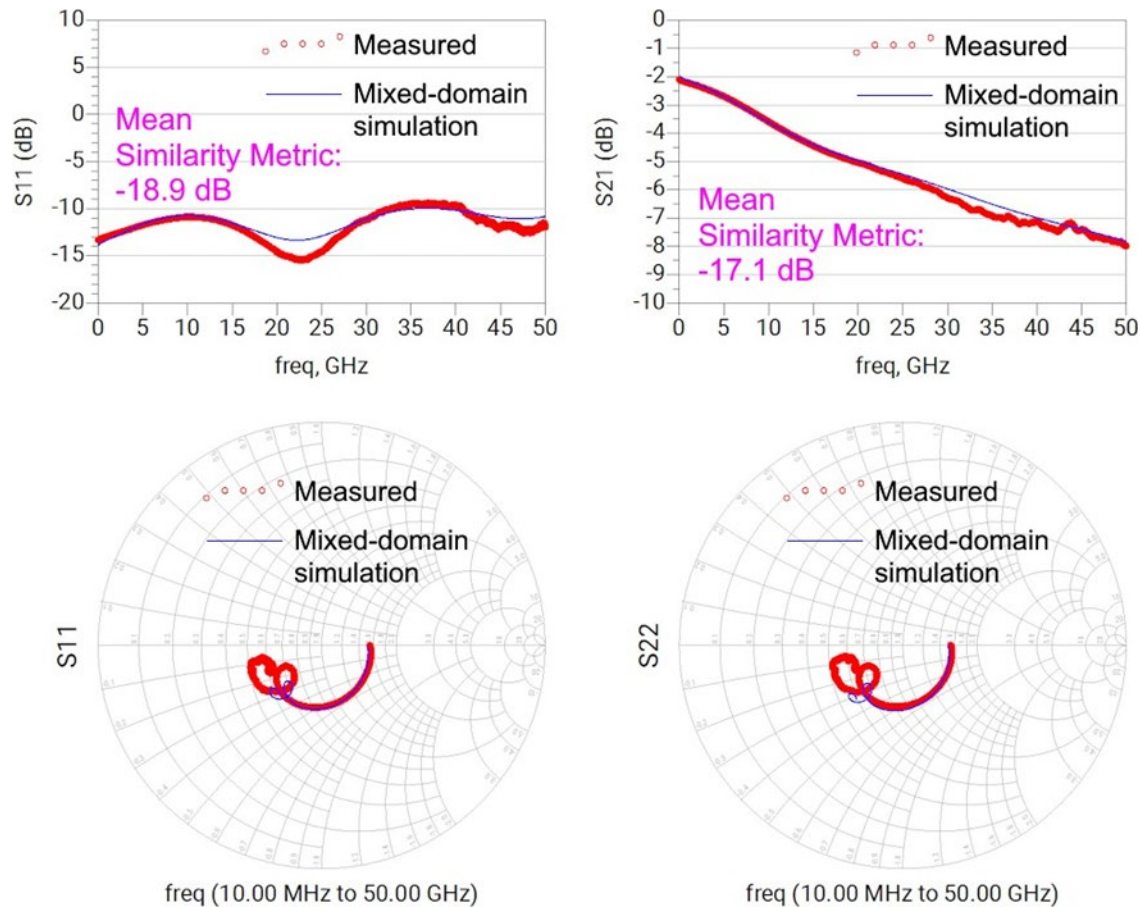


Figure 16. S-parameter results from TEG2 measurement and mixed-domain simulation comparison. The mean similarity metrics for S11 and S21 are -18.9 dB and -17.1 dB, respectively, indicating a good match for both S-parameters.

2000 um Length Microstrip Line with Hatched Ground

TEG1 represents a specific test case featuring the configuration: "Probe Pad – Stacked Via Microstrip on top layer with hatched ground – Stacked Via – Probe Pad," as illustrated in Figure 17. The total line length is 2000 μm from pad to pad. The mixed-domain modeling approach was applied in the same way for the TEG2 case.

As shown in Figure 17, the resulting agreement between the model and measured data is similar to TEG2 case. The S-parameters and the resulting mean Similarity Metric between the model and measured data, which are -16.2 dB and -15.9 dB, indicating a **good** match for both the scalar magnitude and the vector data. There are a few more mismatches in the return loss around 20 GHz and 50 GHz. This may be due to the probe grounding effects.

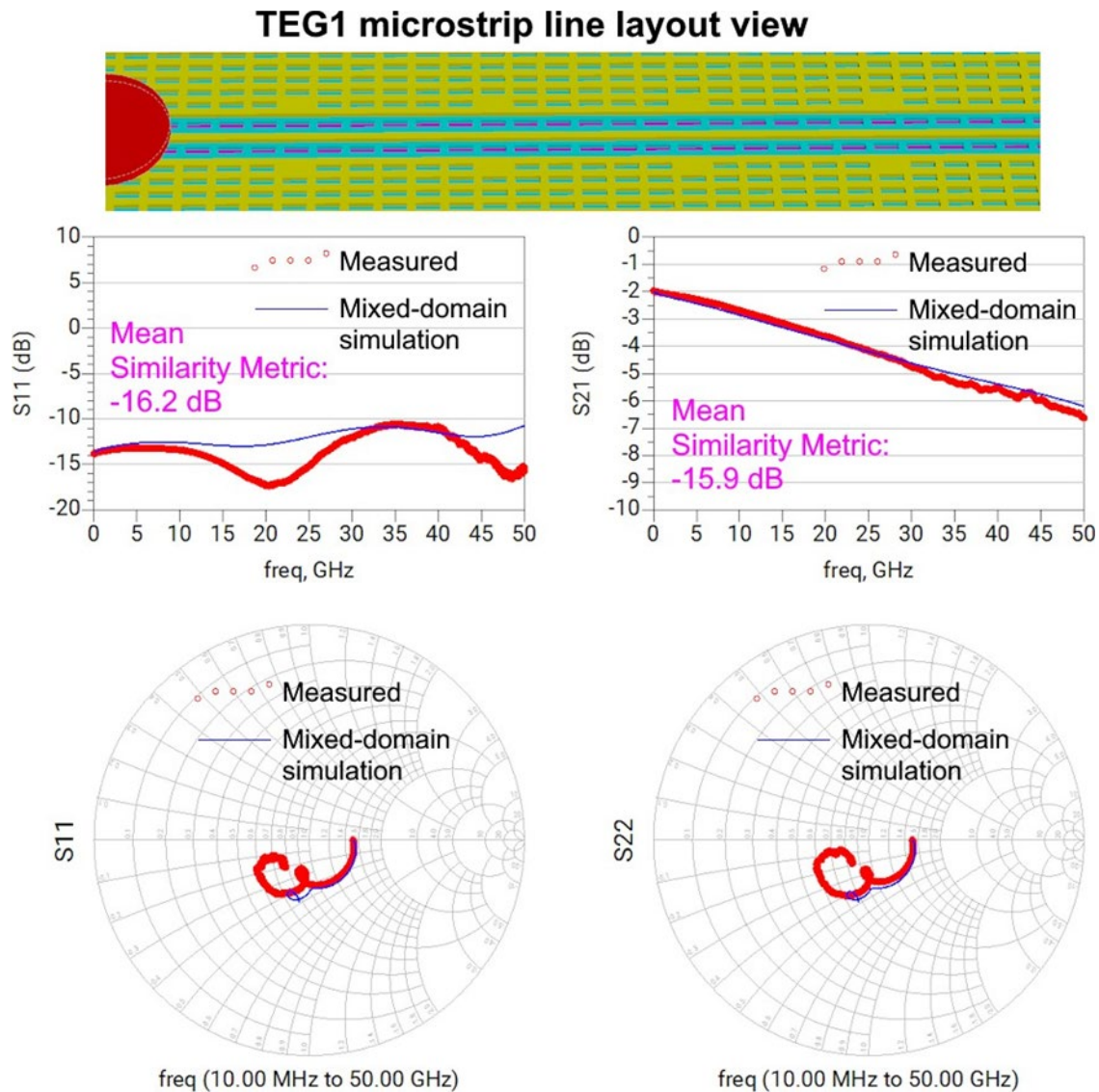


Figure 17. S-parameter results from TEG1 measurement and mixed-domain simulation comparison. The mean similarity metrics for S11 and S21 are -16.2 dB and -15.9 dB, respectively, indicating a good match for both S-parameters.

2000 μm Length Differential Stripline with Hatched Ground

In the previous test cases, only single-ended structures were evaluated. The TEG5 test case represents a configuration using differential signaling, consisting of Probe Pad – Stacked Via – Stripline on the 2nd Layer with Hatched Ground – Stacked Via – Probe Pad, as illustrated in Figure 18. The total stripline length is 2143 μm from pad to pad, including the fan-in structure. The central differential-pair segment is approximately 2002 μm long. A mixed-domain modeling approach was applied in a manner consistent with the other test cases.

The resulting correlation between the modeled and measured data indicates a good match for the SDD11 similarity and a very good match for SDD21. The SDD parameters exhibit close agreement, although a deviation of approximately 1.2 dB is observed in the insertion loss near 40 GHz. The differential return-loss responses (SDD11) closely follow the measured trends, yielding strong overall agreement.

Although additional refinements could further improve the match between the two, the validation results demonstrate excellent agreement, especially when considering measurement challenges, repeatability limitations, and fabrication tolerances.

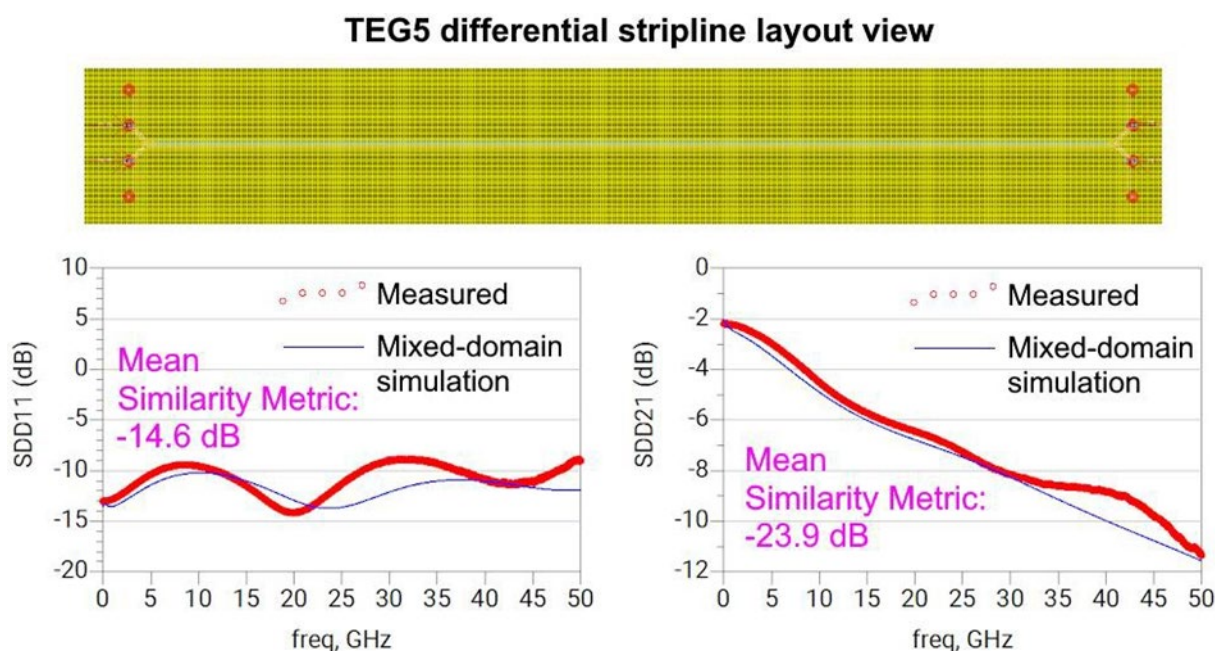


Figure 18. S-parameter results from TEG5 differential stripline measurement and mixed-domain simulation comparison. The mean similarity metrics for SDD11 and SDD21 are -14.6 dB and -23.9 dB, respectively, indicating a good match for SDD11 and a very good match for SDD21.

FlexPCB Measurements and Validation

Measuring FPCBs presents unique challenges due to their flexible, non-rigid nature. In this work, the flex circuits were mounted onto a piece of acrylic with an elongated hole in the middle, allowing most of the flex would be suspended in air. The measurement setup and calibration followed the same procedures used for the silicon bridge, with GTL40-400-GSSG-DP probes and a GTL-1022 calibration substrate.



Figure 19. An example measurement setup of the Flex PCB Measurement.

FlexPCB Validation

Validation results, shown in Figure 20, indicate strong agreement between the mixed-domain model and measured data. The Mean Similarity Metrics were -14.2 dB for S_{11} and -8.7 dB for S_{21} , demonstrating good match for both magnitude and phase. The simulations closely matched measured S-parameters, accounting for variations in the flex PCB stack-up introduced by manufacturing tolerances. Additional investigations may further reduce minor discrepancies in return and insertion loss.

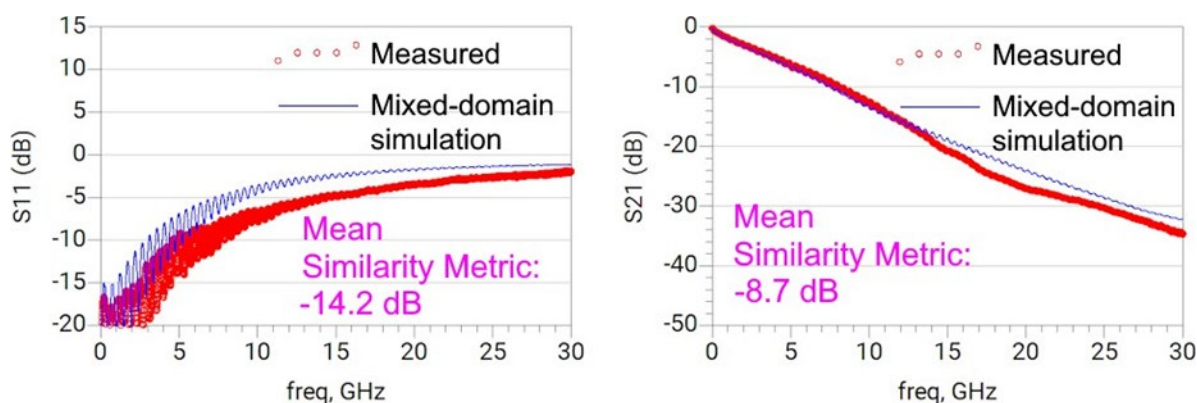


Figure 20. S-parameter results from the Flex PCB measurement and mixed-domain simulation comparison. The mean similarity metrics for S_{11} and S_{21} are -14.2 dB and -8.7 dB, respectively, indicating a good match for both S_{11} and S_{21} .

Conclusion

This work demonstrates a practical and efficient methodology for modeling 3D interconnects that incorporate hatched return planes in silicon interposers, silicon bridges, and flex PCBs. Patterned return structures, while critical for manufacturability and mechanical reliability, introduce significant electromagnetic complexity that traditionally required full 3D EM simulations, often with high computational cost, especially for lossy, multilayer stack-ups.

By combining a specially designed quasi-static 2D field solver with full 3D EM analysis under a mixed-domain modeling framework, essential physical effects of hatched return planes can be captured accurately while significantly improving simulation efficiency. This approach allows designers to evaluate and optimize complex interposer and flex PCB interconnects early in the design process, reducing reliance on fully meshed 3D simulations without sacrificing accuracy for high-speed digital links.

Two fabricated test vehicles — a UCIe 2.0 silicon bridge and a mobile flex PCB — were used to validate the methodology. Across both platforms, simulation and measured S-parameters showed excellent agreement, confirming that the combination of quasi-static 2D solvers for transmission lines and full-wave FEM for transition regions provides a reliable and scalable approach for evaluating advanced interconnects with patterned ground planes.

Overall, this methodology bridges the gap between manufacturable designs and simulation-driven workflows, providing system architects and signal integrity engineers with a validated, efficient path to predict performance, accelerate design iterations, and reduce development risk as chiplet-based and flex PCB systems scale toward higher data rates and greater integration complexity.

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