APPLICATION NOTE

Trapping Extraction of GaN HEMTs

KEYSIGHT

Introduction

Gallium nitride (GaN) is gaining importance due to its ability to provide significantly improved performance with reduced energy and physical space compared to conventional silicon technologies. In some applications where silicon has reached its limits, GaN becomes essential, while in others, its efficiency, switching speed, size, and high-temperature operation make it increasingly attractive.

Trapping effects modeling is a complex and interdisciplinary field that involves solid-state physics, numerical methods, materials science, and electronics. Accurate modeling of trapping effects is essential for optimizing semiconductor device performance, reliability, and functionality. The CMC standard compact models for GaN high electron mobility transistors (HEMTs), such as ASM-HEMT [1] and MVSG_CMC [2], consider the effects of trapping.

ASM-HEMT 101.3.0 has four trapping models, which can be controlled using the switch parameter TRAPMOD. The fourth model (TRAPMOD=4), recommended for its higher degree of freedom, separates the gate-lag and drain-lag by two independent sub-circuits controlled by different parameters. MVSG_CMC 3.1.0 has two trapping models controlled by the switch parameter TRAPSELECT. The second model (TRAPSELECT=2) is the newest and recommended.

The latest trapping models from ASM-HEMT and MVSG_CMC use two sub-circuits to simulate gate-lag and drain-lag. However, in ASM-HEMT, the trapping effective voltage mimics from the RC sub-circuit and trapping parameters are applied to the core parameters and influence the output drain current. In contrast, MVSG_CMC mimics the trapping effective voltage through the RC sub-circuits and emission/capture time constants and applies it to the calculation of charge to realize the effect of trapping on the output current.

The parameter extraction of ASM-HEMT and MVSG_CMC in PathWave Device Modeling (IC-CAP) includes trapping modeling. Despite the two compact models' different implementations of the trapping model, the same parameter extraction strategy is used. Trapping extraction is performed after S-parameter extraction, and gate-lag trapping extraction is performed before drain-lag. We extract gate-lag before drain-lag because it affects the initial transistor response and overall behavior during transitions. Properly characterizing gate-lag helps to better account for it when studying drain-lag effects. For the measurement setup, we use input pulse voltage and extract trapping parameters by fitting the delay in the output drain current.

Trapping Model in ASM-HEMT

A variety of trap effect models are introduced in ASM-HEMT. The model configuration switch TRAPMOD can turn these different modeling methods on or off. Each TRAPMOD setting uses a different approximation to model the trapping effect. These different approaches are discussed below to meet usage requirements and equipment selection.

TRAPMOD=0: The trapping model is off.

TRAPMOD=1: A single RC sub-circuit with a diode in series is used.

TRAPMOD=2: Two different RC sub-circuits are used for the gate-lag and drain-lag trapping model

TRAPMOD=3: A single RC sub-circuit is used. Only the drain-side resistance is affected in this trap model.

TRAPMOD=4: This is the most recommended trapping model in ASM-HEMT. Modeling drain-lag and gate-lag phenomena independently use two different RC sub-circuits. The trap effective voltage and trapping parameters act on the key model parameters VOFF, U0, VSAT, DLNS0S, and DLNS0 in pulsed simulation conditions, influencing output performance. DC and S-parameter simulations are not affected by the parameter change.

Trapping Model in MVSG_CMC

A new trapping model has been added to the MVSG_CMC 3.1.0 official release. To select these models, switch the flag TRAPSELECT. Details are discussed below:

TRAPSELECT=0: The trapping model is off.

TRAPSELECT=1: A trapping model replicates the impact of an increased RDSON (on-resistance) caused by charge trapping. The RDSON shift is determined by the bias (V_{DG}), and a simple RC subcircuit with one time constant is used for trapping and de-trapping, enabling frequency dependence.

TRAPSELECT=2: This model is the most recommended one in MVSG_CMC. The trapping model includes realistic drain-lag and gate-lag effects observed in measurements. The observed drain and gate voltage dependencies are incorporated through separate subcircuits. Both capture and emission time constants are considered. In addition, the temperature dependence is added. Figure 1. (a) and (b) show the sub-circuits for gate-lag and drain-lag. V_G and V_D are inputs to each sub-circuit. Using an RC delay network, they mimic the state of the voltage after being affected by the trapping effect $V_{G,Lag}$ and $V_{D,Lag}$ shown in the figure, act as bias-dependent trapping stress functions and model the channel-currents and charges to mimic trapping effects.

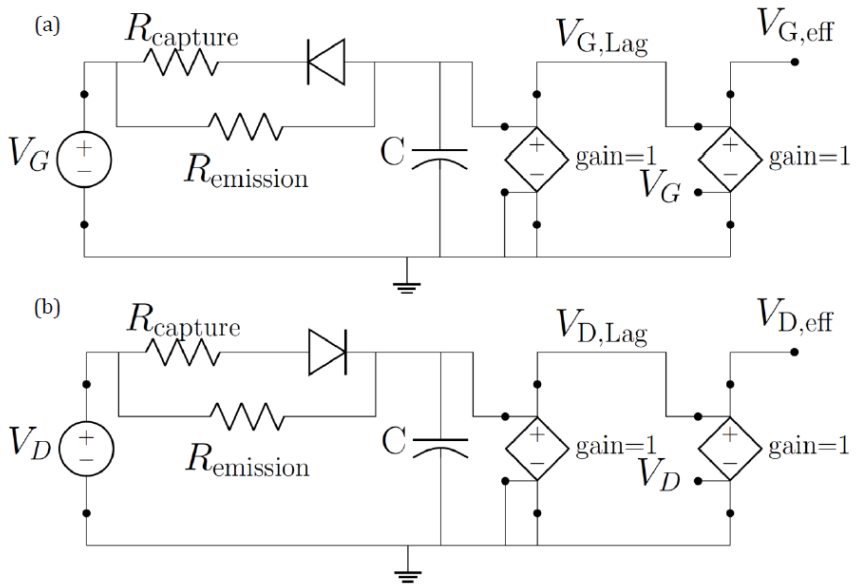

Figure 1. (a) Gate-lag and (b) Drain-lag sub-circuit schematic of the trapping model with TRAPSELECT=2 in MVSG_CMC

Trapping Extraction with ASM-HEMT and MVSG_CMC

Trapping effects can significantly impact electronic devices' performance and reliability, as trapped charge carriers can cause shifts in the device characteristics, affecting parameters like threshold voltage and capacitance. Thus, accounting for these effects in the devices' design, manufacturing, and operation is very important to ensure their functionality and longevity.

In the IC-CAP CMC GaN RF Modeling package, we provide trapping effect modeling flows for ASM-HEMT and MVSG_CMC respectively. Although the trapping model differs between these two models, the extraction strategy remains the same. Next, the trapping extraction process for both models will be introduced.

ASM-HEMT trapping extraction

As described above, TRAPMOD=4 is the most recommended trapping model in ASM-HEMT. In IC-CAP, we use this model as an example. Figure 2. shows the parameter extraction workflow of ASM-HEMT. After extracting the S-parameter, we proceed with the trapping parameter extraction and divide it into gate-lag and drain-lag.

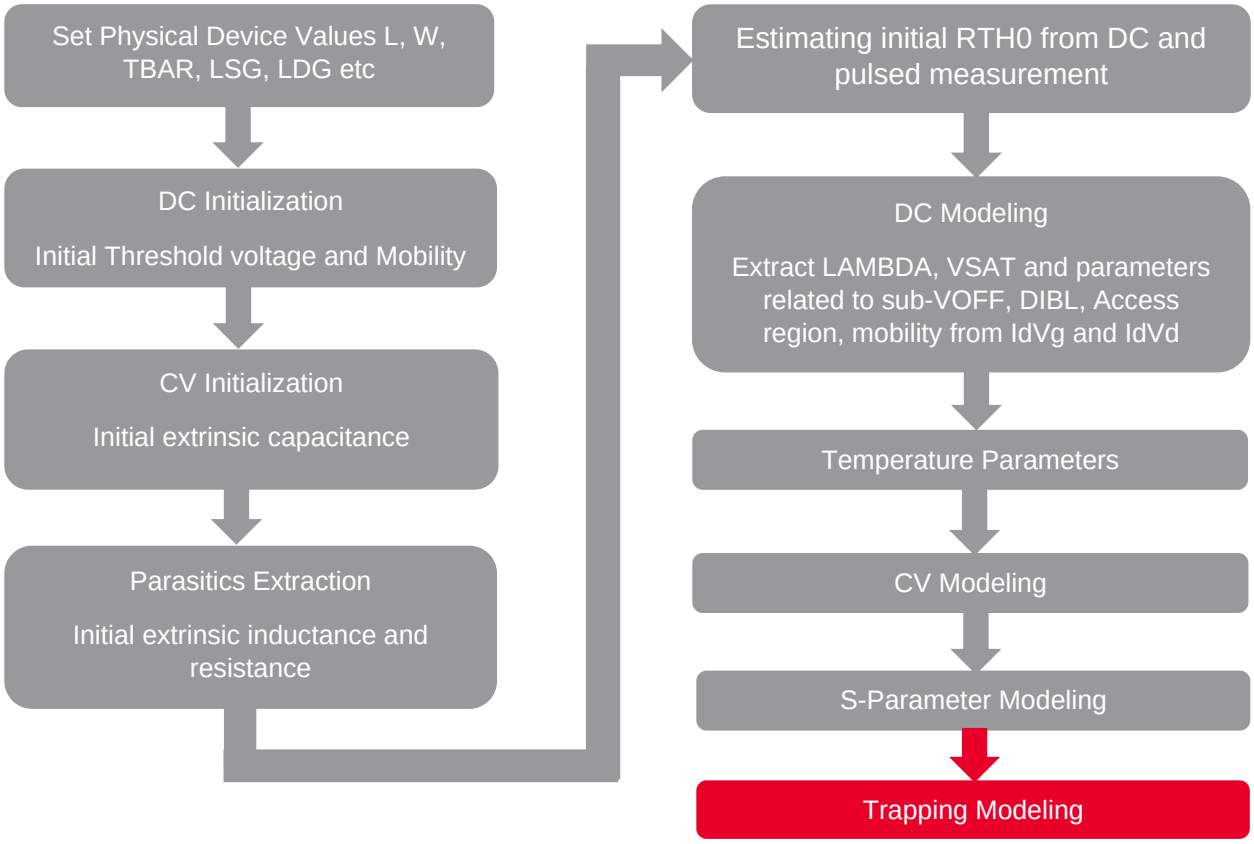

Figure 2. Overview of ASM-HEMT parameter extraction flow.

Due to the gate-lag phenomenon, the current flowing through a transistor takes time to respond to gate voltage changes. It can cause a delayed turn-on or turn-off response of the transistor. Charge trapping and de-trapping processes in the gate oxide primarily cause gate-lag and affect the effective threshold voltage of the transistor. Figure 3. (a) and (b) show input gate voltage V_g and output drain current I_d changing with time. V_g represents the input pulsed voltage, while the drain voltage V_d is constant. The purple box highlights a delay in the output current due to the trapping effect.

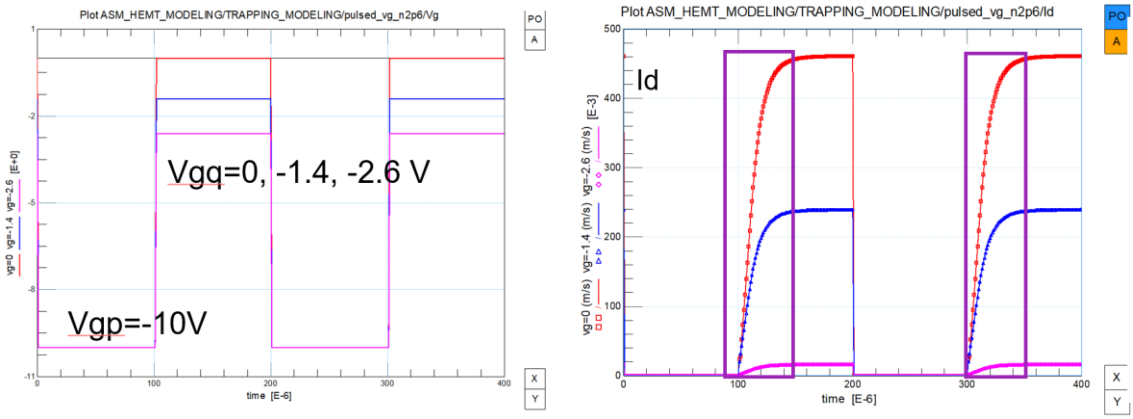

Figure 3. (a) Input pulsed Gate voltage V_g-time and (b) Output drain current I_d-time. The quiescent operating points V_{gq}=0, -1.4, -2.6 V, and pulsed voltage V_{gp}=-10V. Input drain voltage V_d=10V.

In ASM-HEMT, the effective voltage generated by the RC sub-circuit and trapping-related parameters acts simultaneously on core parameters such as cut-off voltage VOFF to represent the trapping effect in simulation. Table 1. displays the relevant parameters of gate-lag extraction. Table 1. shows the relevant parameters of the gate-lag extraction.

Table 1. Parameters of the gate-lag extraction.

Parameter	Value	Description
REMIG	50	Gate-lag trapping resistance
CGLAG	200n	Gate-lag trapping capacitance
ARCAPG	10m	Gate-lag trap potential tuning parameter
BRCAPG	50m	Gate-lag trap potential tuning parameter
VGLMAX	5	Gate-lag parameter for limiting parameter change
GLVOFF	-2.5m	Voff tuning due to gate-lag
GLU0	220m	U0 tuning due to gate-lag
GLVSAT	230m	VSAT tuning due to gate-lag

Drain-lag phenomenon in transistors, where channel current response to changes in drain voltage is delayed. The delay occurs due to the impact of drain voltage on the electric field across the device, which influences the movement of charge carriers in the channel. It takes some time for the channel current to reach a new steady-state value as the drain voltage changes, owing to charge storage effects within the device. Figure 4. (a) and (b) show input drain voltage $\boldsymbol{V_d}$ and output $\boldsymbol{I_d}$ changing with time. $\boldsymbol{V_d}$ is a pulsed voltage, and input gate voltage $\boldsymbol{V_g}$ is constant. Note the delay of $\boldsymbol{I_d}$ highlighted in the purple box. Table 2. shows the relevant parameters of the drain-lag extraction.

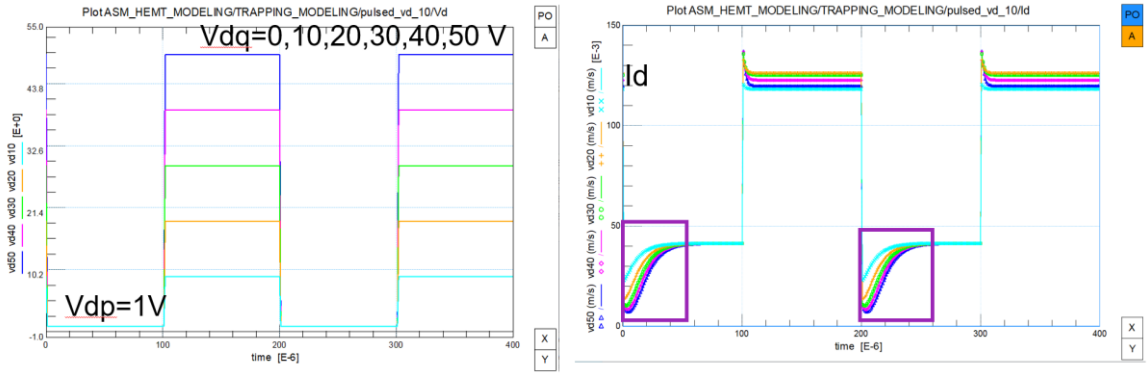

Figure 4. (a) Input pulsed drain voltage V_d-time and (b) Output drain current I_d-time. The quiescent operating points V_{dq}=0, 10, 20, 30, 40, 50 V, and pulsed voltage V_{dp}=1V. Input gate voltage V_g=-2V.

Table 2. Parameters of the drain-lag extraction.

Parameter	Value	Description
REMI	10	Drain-lag emission resistance
CDLAG	1u	Trap Network capacitance, shared parameter TRAPMOD=1 and 4
ARCAP	50m	Drain-lag trap potential tuning parameter
BRCAP	500m	Drain-lag trap potential tuning parameter
VDLMAX	20	Drain-lag parameter for limiting parameter change
DLVOFF	-10m	Voff tuning due to drain-lag
DLNS0S	0	Source-side 2-deg tune due to drain-lag
DLNS0D	0	Drain-side 2-deg tune due to gate-lag

MVSG_CMC trapping extraction

In MVSG_CMC, the recommended trapping model is TRAPSELECT=2. Unlike ASM-HEMT, MVSG_CMC generates a charge ratio based on the effective voltage impacted by trapping, influencing the charge used to compute drain current. While the two compact models have different trapping modeling, they share the same extraction strategy. The trapping parameters are extracted after the S-parameter, followed by gate-lag and drain-lag extraction.

Figure 5. (a) and (b) show the input $\boldsymbol{V_g}$ and output $\boldsymbol{I_d}$ changing with time for gate-lag extraction. $\boldsymbol{V_g}$ is a pulsed voltage and $\boldsymbol{V_d}$ is constant. After performing the transient simulation, we can see the delay in the output current due to the trapping. Table 3. shows the relevant parameters of the gate-lag extraction.

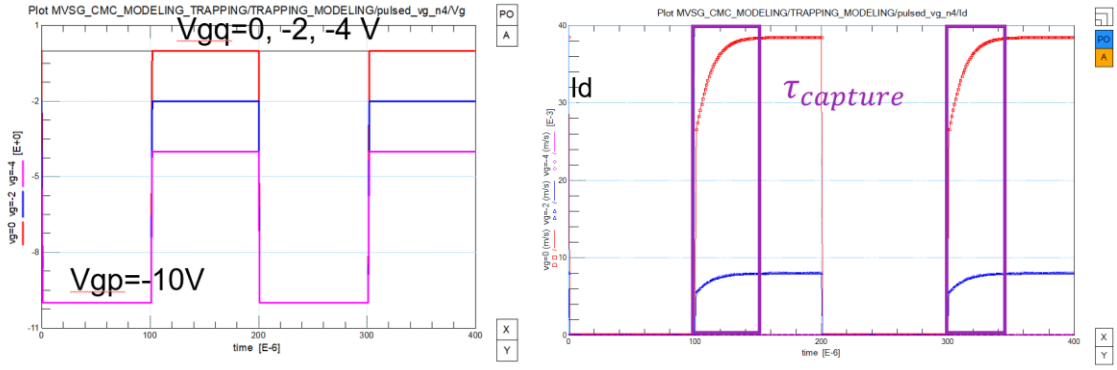

Figure 5. (a) Input pulsed gate voltage V_g-time and (b) Output drain current I_d-time. The quiescent operating points V_{gq}=0, -2, -4 V, and pulsed voltage V_{gp}=-10V. Input drain voltage V_d=10V.

Table 3. Parameters of the gate-lag extraction.

Parameter	Value	Description
VGLTRAPTH	10	Trapping gate-lag stress threshold voltage
RSLOW (RCAPTURE)	10	Trapping capture time constant
CDGLAG	1u	Trapping emission and capture time constant-C
RCT1GL	5m	Linear gate-lag temperature coefficient
RCT2GL	0	Quadratic gate-lag temperature coefficient
ISAT	1n	Trapping reverse saturation current for diode

Figure 6. (a) and (b) show input $\boldsymbol{V_d}$ and output $\boldsymbol{I_d}$ changing with time for drain-lag extraction. $\boldsymbol{V_d}$ is a pulsed voltage, and $\boldsymbol{V_g}$ is constant. After running the transient simulation, we observe a delay in the output current caused by trapping. The delay in the purple box is mainly determined by the emission time constant, while the ones in the red boxes result from the capture time constant. Table 4. shows the relevant parameters of the drain-lag extraction. Table 4. shows the relevant parameters of the drain-lag extraction.

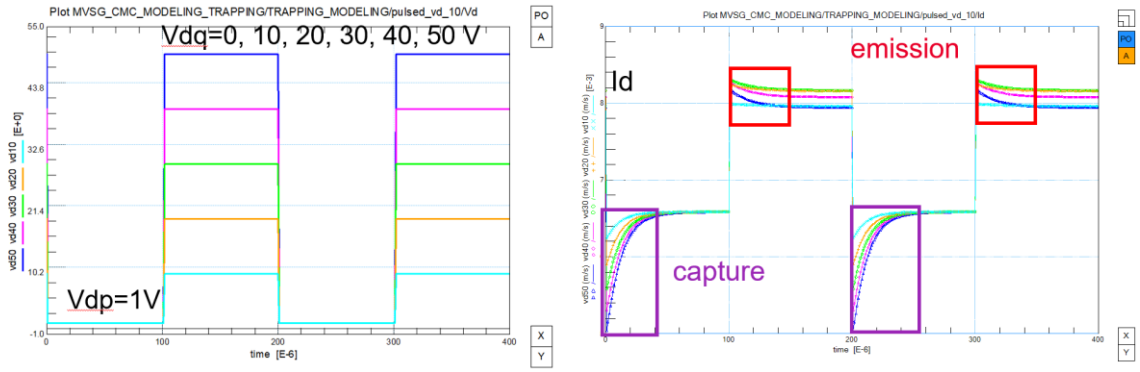

Figure 6. (a) Input pulsed drain voltage V_d-time and (b) Output drain current I_d-time. The quiescent operating points V_{dq}=0, 10, 20, 30, 40, 50 V, and pulsed voltage V_{dp}=1V. Input drain voltage V_g=-2V.

Table 4. Parameters of the drain-lag extraction.

Parameter	Value	Description
VDLTRAPTH	100	Trapping drain-lag stress threshold voltage
RSLOW (RCAPTURE)	10	Trapping capture time constant
RFAST (REMISSION)	50m	Trapping emission time constant
CDGLAG	1u	Trapping emission and capture time constant-C
RCT1DL	-5m	Linear drain-lag temperature coefficient
RCT2DL	0	Quadratic drain-lag temperature coefficient
ISAT	1n	Trapping reverse saturation current for diode

Conclusion

In conclusion, trapping plays a significant role in the device modeling of GaN HEMTs for circuit design. Accurate modeling of trapping effects is crucial in RF engineering to ensure RF components and systems' desired performance, efficiency, and reliability. By understanding and mitigating the impact of trapping, designers can create more effective RF devices that meet the demands of modern communication, sensing, and signal-processing applications.

In extracting parameters for ASM-HEMT and MVSG_CMC, we cover the trapping parameters extraction and use their latest models as examples in IC-CAP. Although the trapping models are different for the two compact models, the extraction strategy remains the same. The trapping parameters can be efficiently extracted by modeling the gate-lag and drain-lag using the corresponding pulsed voltage.

Reference

[1] Sourabh Khandelwal, Jason Hodges, and Nikhil Reddy, “ASM-HEMT 101.3.0 Advanced SPICE Model for HEMTs Technical Manual,” 2022

[2] Ujwal Radhakrishna, and Lan Wei, “MIT Virtual Source GaN HEMT: MVSG Model Manual,” 2021

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