

# Virtual Reference Design

PathWave ADS Workspace for Transphorm

tdt4000w066c

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# PathWave ADS Workspace for Transphorm tdttp4000w066c

This application note provides information to obtain and use a PathWave ADS workspace that you can use to simulate a virtual version of a physical reference design from Transphorm, Model tdttp4000w066c. This model showcases the gen IV GaN power transistors (TP65H035G4WS series) also from Transphorm. Provides the details on how they can be used to build your next-generation switched-mode power supply. In addition, the reference design – in both virtual and physical forms - can be used as starting point for your own project.

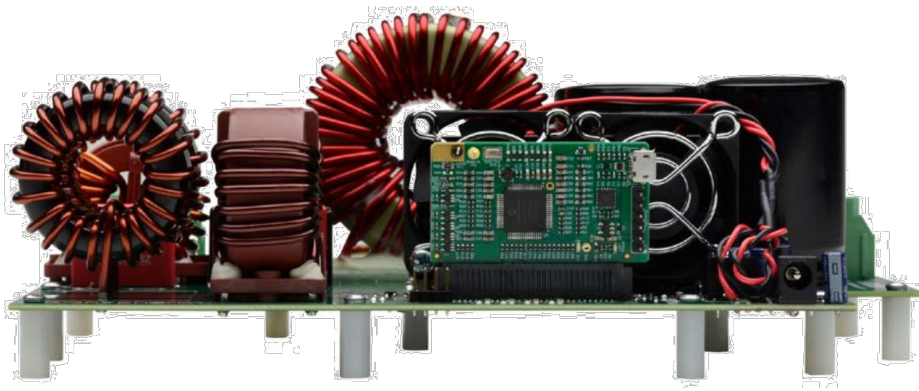


Figure 1. Transphorm's tdttp4000w066c

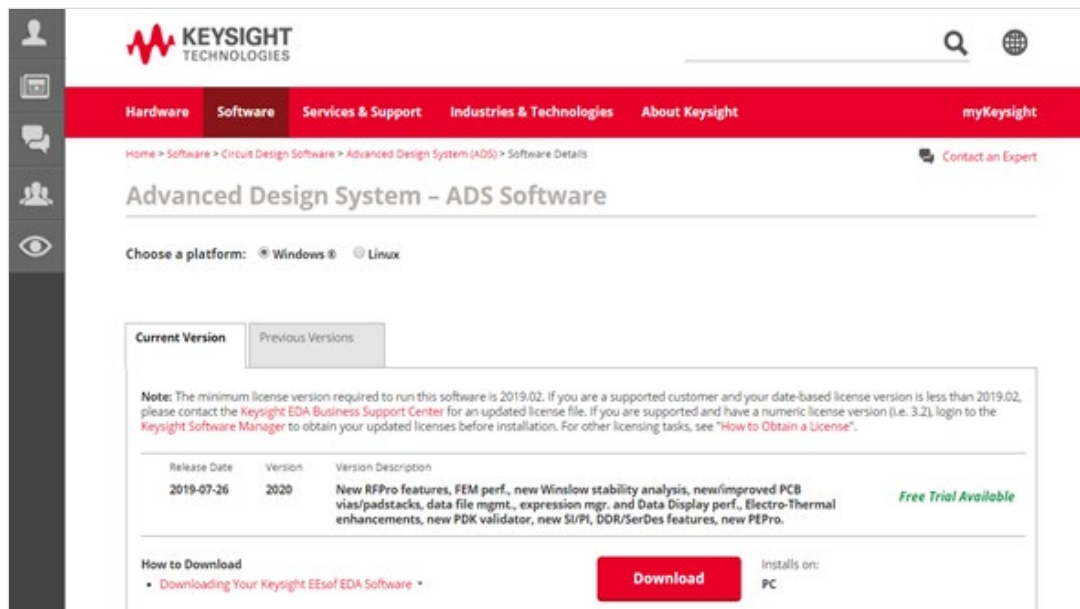
## Dependencies/Pre-requisites from Keysight and Transphorm

This section lists the dependencies/pre-requisites that you will require from Keysight and Transphorm.

### Dependencies/pre-requisites from Keysight

#### Step 1: Download and Install the PathWave ADS binaries

1. Go to <http://www.keysight.com/find/eesof-ads-latest-downloads>.
2. Download the ADS installation file(s): **64-bit**: ads\_20XX\_win\_x64.exe to any folder, for example C:\Temp.



Note: If you need any assistance, click Contact an Expert to reach out to an expert.

## Step 2: Request a no-charge 45-days evaluation license

1. Go to <http://www.keysight.com/find/eesof-ads-evaluation>.

## Installing Advanced Design System (ADS)

To install Advanced Design System on Windows, follow these steps.

1. Run the downloaded installation file from the location where you saved it. Before starting the installation, the installation file extracts all the necessary files in a temporary folder.
2. Select the language from the drop-down list of **Installation** window and click **OK** to continue.
3. On the **Introduction** screen, click **Next** to read the License Agreement. This is only a usage agreement and is not related to the licenses required to run the software.
4. On the **License Agreement** screen, accept the agreement and click **Next**.
5. On the **Choose Install Set** screen, choose any one of the two installation options:
  - **Complete**: For complete ADS installation. It requires about 4.5 GB of disk space and installs the ADS design environment, simulators, documentation, examples, and design guides. If you choose **Complete** installation, skip the next step.
  - **Custom**: For custom ADS installation where you can choose from the ADS items you want to install. While you can choose which ADS items you want to install, the ability to run them is determined by the purchased licenses.

6. For custom installation, the next screen lets you choose the items you want to install. Click any item name to see the description of the same in the window. Select the items you want to install and click **Next**.

You must choose to install *ADS programs and tools* which includes *Layout, Simulators and Schematic Capture*; else ADS will not run properly. *Manuals & Help* is selected by default to install the entire ADS documentation set. If you uncheck this item, documentation and help files will not be available regardless of which other items you choose.

7. At the Choose Install Folder screen, click:
  - **Next** to install to the default folder. The installation program creates this folder if it does not already exist. One more option **Restore Default Folder** is also provided to restore the default folder after every uninstallation.
  - **Choose** to specify a different destination folder. If you specify a folder that does not already exist, the installation program will create it for you. The default folder for ADS installation is: **64-bit:**"C:\Program Files\Keysight\ADS20XX"  
You can change the default location and select your own desired path. Ensure that you must have permissions to write to the disk drive on which you want to install ADS. The installation also adds entries to your PC's Windows Registry, so ensure that you have permissions to do so.
8. At the Set Your Home Directory screen, click:
  - **Next** to accept the default.
  - **Choose** to select a different folder. The folder you specify will be the default startup folder for ADS. It will also be used to store the configuration data in a subfolder called *hpeesof*. For every single release and sub-release of ADS (such as ADS 2012.08, ADS 2013.06, ADS 2014.01, ADS 2015.01 and ADS 2016.XX), you must choose a new *Home* folder for each version. For the best performance, choose a folder on your local, not network drive.
9. At the Choose Shortcut Folder screen:
  - You can type a name in *Start Menu Folder Name* to have the same named folder in **Start** menu, by default it is Advanced Design Systems 2016.XX.
  - If you want ADS icon on desktop, check the *Icon To Desktop* option.
10. At the Pre-Installation Summary screen, review your choices, and click:
  - **Previous** to access previous screens to verify entries and make changes. This screen appears again if you go back to make other choices.
  - **Install** to start the installation. Immediately after you click **Next**, the *Setup Status* screen appears, and the program configures the installation process. When the program determines that your system is ready for installation, it begins to install files. The status screen displays the files being installed and the progress.
  - **Cancel** to exit the Setup without completing the installation.
11. After installation, click **Done** to quit the installer. The ADS License Setup Wizard starts automatically after this and check for the license status. Before launching ADS, you must complete the ADS license setup.

# Setting up licenses on Windows

This section describes how to set up a node-locked license or a floating (network) license on Windows.

Both node-locked and floating licenses require license server to get installed and started. For a node-locked license, license server and the client machine are the same machine (that is, your local machine). For a floating license, these can be separate machines.

## Setting up floating licenses on windows

Setting up floating licenses on Windows is a two-step process where both server-side setup and client-side setup are needed.

### Step 1: License server setup

To setup a dedicated floating license server that has no Keysight EDA software installed, you will need to download and install the EEsof EDA License Server Software. This will install the license daemons and utilities needed to configure and start the license server.

Repeat the following steps for each license server you have.

### Step 2: Client setup

Once the license is configured successfully for all the license servers, configure each client computer to point to the network license server. **License Setup Wizard** offers the easiest method to get this done. Alternatively, you can perform this step manually by following step 3 of Setting up Node-locked License on Windows section. Make sure to specify the network license server in the format of `port@host.domain` or if no static TCP port is used on the license server, use the format `@host.domain`.

#### Examples

`27001@myServer.myCompany.com`  
`@myServer.myCompany.com`

In case a license server is down or is running slow, it is recommended to remove it from the server list using the **License Setup Wizard** to avoid any performance degradation caused by the dead/slow servers.

## Setting up node-locked license on Windows

On Windows, the License Setup Wizard offers the easiest way to set up your node-locked license. We strongly recommend you to use the **License Setup Wizard**, especially when you have multiple Keysight EEsof products installed on one computer. For more information, refer to Quick Install-Windows. This section describes how to set up a node-locked license manually, should you decide not to use the **License Setup Wizard**.

Do not perform manual setup steps with the **License Setup Wizard**. Choose one method or the other. **License Setup Wizard** may not be able to replace what you set up manually due to Administrator Privilege differences.

The following instructions assume that you have already installed Keysight EEsof Licensing Tools in *C:\Program Files\Keysight\EEsof\_License\_Tools* folder. In case you have not yet installed the tools, run the Keysight EEsof Licensing Tools installer on the machine to which the license is tied to.

- If you have installed an EEsof product released before 1st August, 2014 on your system prior to installing an EEsof product released after 1st August, 2014 then the default EEsof Licensing tools path will remain C:\Program Files\Agilent\EEsof\_License\_Tools. On the systems that only have EEsof products released after 1st August, 2014 installed then the default EEsof Licensing tools path will be C:\Program Files\Keysight\EEsof\_License\_Tools.
- Make sure to save the license file on the same machine where you install the Keysight software.

The following 3-step process shows how to manually set up a counted license that is tied to a CPU ID.

### Step 1: Start license server managers

Start the FlexNet license server managers ( *lmgrd* and *agileesofd* ) on the computer to which the license is tied as follows:

1. Open the MS-DOS command prompt and change directory to the following path: *C:\Program Files\Keysight\EEsof\_License\_Tools\bin*.
2. Specify the full path and location of the license file and the license log file, respectively, by typing the following command:  
*lmgrd.exe -c <license file path> -l <license log file path>*  
where,
  - <license file path> specifies one or more full pathnames to the license file(s).
  - <license log file path> is the full pathname to the debug log file.

The spaces in pathnames requires double quotes around the path-names.

#### Example

```
lmgrd.exe -c "C:\Program Files\Keysight\EEsof_License_Tools\licenses\license.lic" -l  
"C:\Users\Public\my_server_log.txt"
```

## Step 2: Create Windows Service

To automate the restart of the license server managers upon PC reboot, configure a Windows Service as follows:

You must have Administrator Privileges to configure a Windows Service. The service will run under the Local System account.

1. Run the *Imtools.exe* from *C:\Program Files\Keysight\EEsof\_License\_Tools\bin*. The **Imtools** utility window is displayed.
2. In the **Service/License File** tab, select the **Configuration using Services** option.
3. Click the **Config Services** tab and enter the following details:
  - **Service Name:** Type the service name (for example, *EEsof EDA License Server*).
  - **Path to the *lmgrd.exe* file:** Click **Browse** and specify the path to the *lmgrd.exe* file on the license server (for example, *C:\Program Files\Keysight\EEsof\_License\_Tools\bin\lmgrd.exe*).
  - **Path to the license file:** Click **Browse** and specify the path to the license file on license server (for example, *C:\Program Files\Keysight\EEsof\_License\_Tools\licenses\license.lic* ). If you have multiple license files for serving multiple Keysight EEsof products, you should include them all.
  - **Path to the debug log file:** Click **Browse** and specify the path to the debug log file on license server (for example, *C:\Users\Public\my\_server\_log.txt*).
1. Select the **Use Services** option.
2. Select the Start Server at Power Up option.
3. Click Save Service.
4. To verify that the service is created, click the **Start/Stop/Reread** tab and observe that your service shows up in the **FlexNet license services installed on this computer** list.  
To verify if the license managers are running, click again on the **Config Services** tab later and click **View Log**. A log window appears that confirms whether *lmgrd* and *agileesofd* are up and running.

## Step 3: Set product environment variable

Set the environment variable <PRODUCT>\_LICENSE\_FILE to point the machine running the license server managers (**Imgrd** and **agileesofd**).

1. Select **Start > Control Panel > System**. Click **Advanced system settings**. The **System Properties** dialog box appears and the **Advanced** tab is selected by default).
2. Click **Environment Variables**.
3. In the **Environment Variables** dialog box, add the product specific environment variable <PRODUCT>\_LICENSE\_FILE as a new system variable. For example, for SystemVue, it is **SYSTEMVUE\_LICENSE\_FILE**, for ADS, it is **ADS\_LICENSE\_FILE**, for EMPro, it is **EMPRO\_LICENSE\_FILE** and so on.
4. In the **New System Variable** dialog box, set the value to be the same as what you specified in the -c argument when you start *Imgrd* . To use the example illustrated in Step 1, second bullet, this value would be *C:\Program Files\Keysight\EEsof\_License\_Tools\licenses\license.lic*.
5. Repeat 3 and 4 for each Keysight EEsof product you have installed on your computer.

## Dependencies/pre-requisites from Transphorm

For details on the Transphorm hardware, including information on how obtain it, please visit <https://www.transphormusa.com/en/evaluation-kit/tdt4000w066c-kit/>

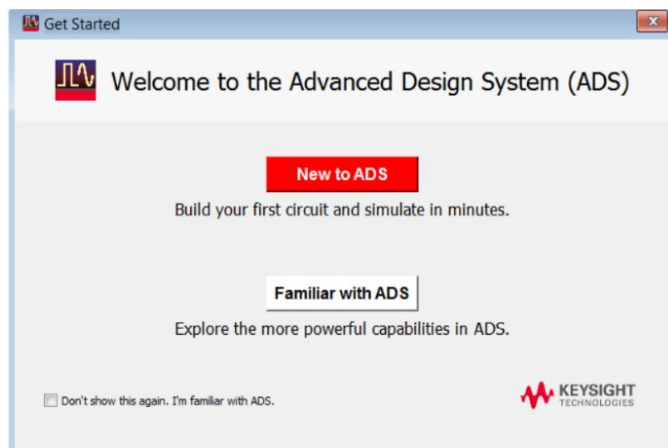
## Step 1: About Transphorm workspace

To download the archive of the Virtual Workspace of the Transphorm 4kW Totem-pole PFC GaN Evaluation Platform, visit: <https://connectp.keysight.com/Transphorm-Evaluation-Platform>

## Launching Advanced Design System (ADS)

To start Advanced Design System (ADS), click Start > Advanced Design System 201x.xx from the taskbar.

- For existing ADS users, ADS starts normally.
- For a new ADS user, The Welcome to the Advanced Design System screen is displayed with two options:
  - **New to ADS** - Starts ADS Quick Start, which enables new users to discover the basics of ADS quickly.
  - **Familiar with ADS** - Starts ADS in normal mode and enables you to explore all the powerful and advanced ADS capabilities.



## ADS Quick Start Mode highlights

- First-time User Detection: ADS Quick Start mode is enabled by default for the first time ADS users. It can be enabled or disabled in the ADS (Main) preferences.
- Simplified Experience: Skips all the startup screens and wizards of the standard mode.
- Overlay Tips: Provides quick steps for getting started effectively with circuit drawing, setting up simulation, and plotting/viewing results.
- Missing Step Detection: Displays messages when critical steps have been missed such as placing a Simulation Controller or in some case a Source.

## Tips to invoke ADS Quick Start Mode

### For new user

When ADS starts, the Welcome to the Advanced Design System screen is presented. To turn off the screen:

- Check the "Don't show this again." on the lower left corner of the screen.  
or
- From ADS Main window, click **Options > Preferences** and uncheck the "Enable Quickstart" checkbox.

### For existing user

ADS starts normally. To enable ADS Quick Start:

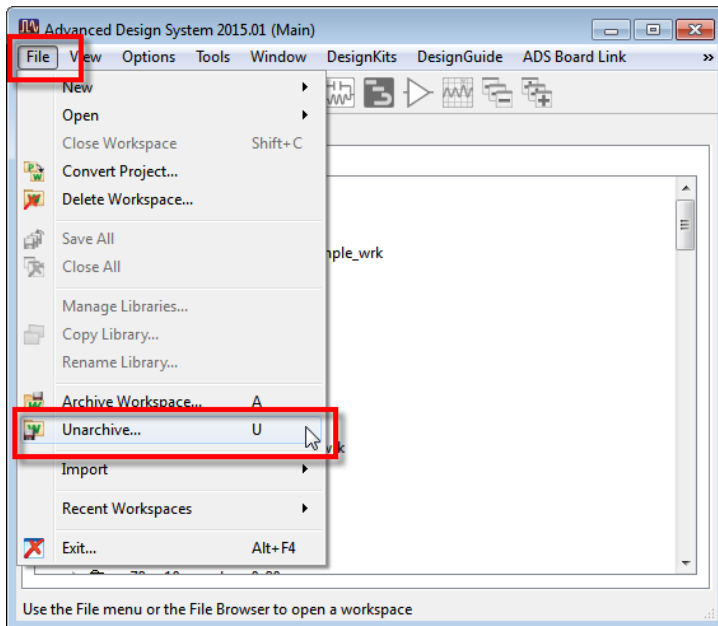
- Type `ads -quickstart` from the command prompt.  
or
- Create a new ADS shortcut that calls `ads -quickstart`.  
or
- From ADS (Main) window, click **Options > Preferences** and check the "Enable Quickstart" checkbox

# Unarchiving the Advanced Design System (ADS) Workspace

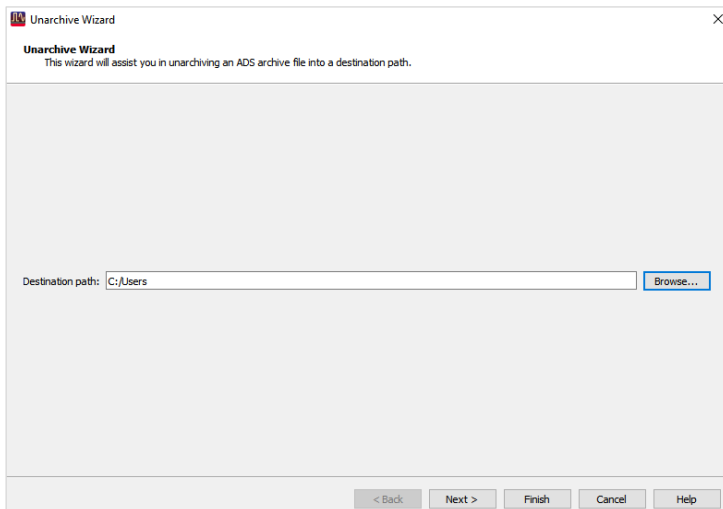
To unarchive the workspace:

1. Click **File > Unarchive**.

The Select an Archive File browse window is displayed.



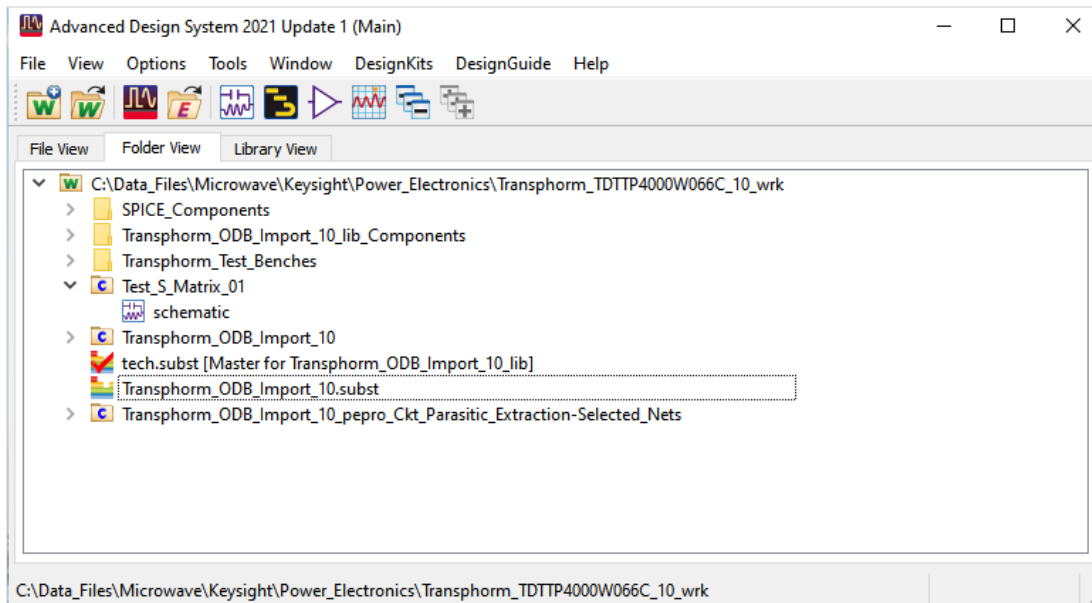
2. Browse to the folder where you downloaded the workspace.
3. Click **Open**. The Unarchive wizard is displayed.



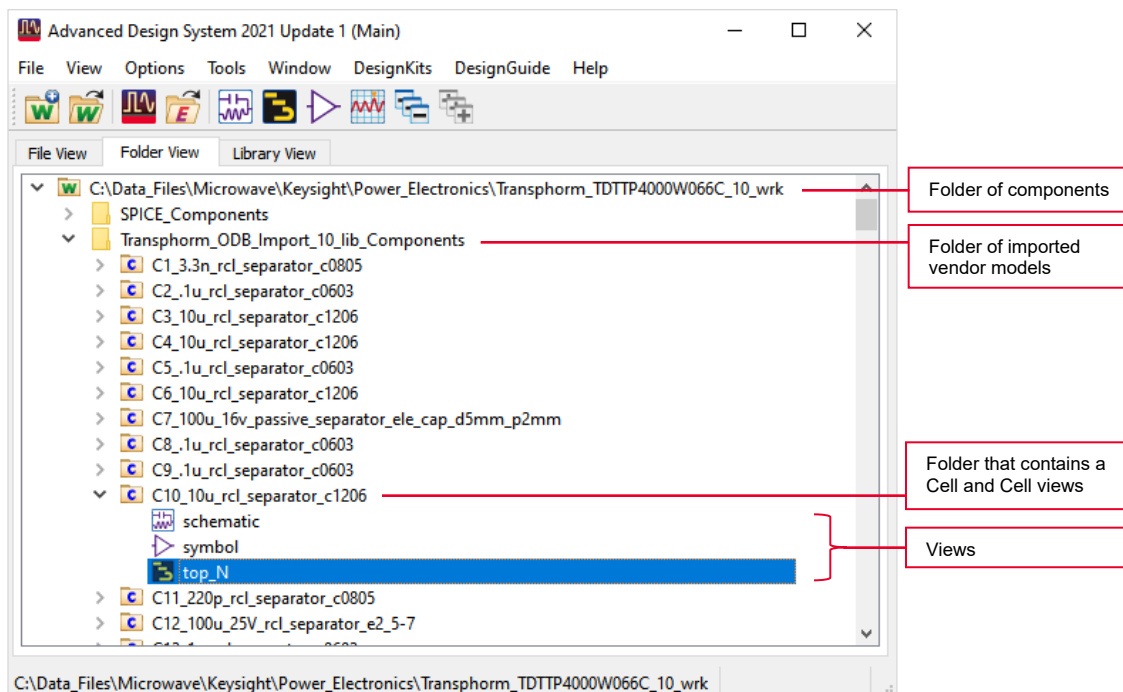
4. Browse to select the destination folder.
5. Click **Finish**.

# Understanding the ADS Workspace

## 1. ADS main window



## 2. Folder of components



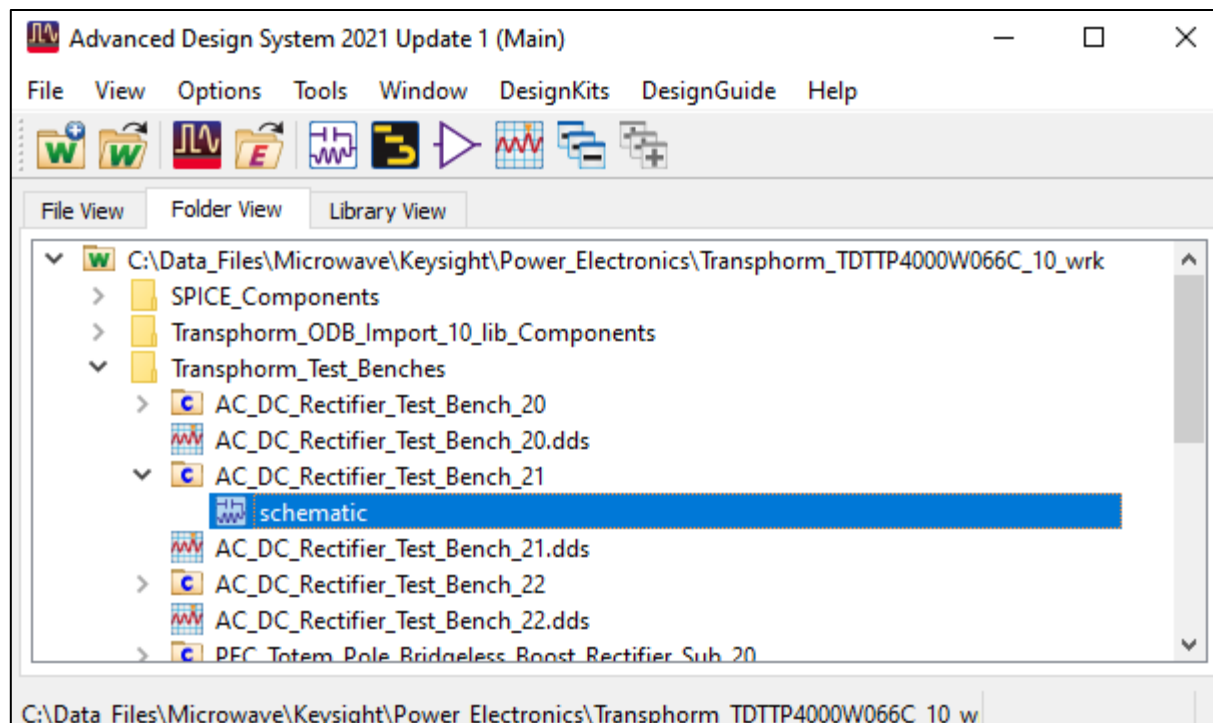
# Running the Circuit Simulations “as-is”

The workspace contains circuit simulations with without parasitics and with different fidelity transistor models. The simulation time is strongly dependent on both. The simulation time for 4 AC periods is just under a minute for most idealized model to 2 ½ hours for a full SPICE transistor and parasitic model.

| Number | Boost transistors | Commutator transistors | Extracted nets | Time (4 AC periods) | Factor | Subcircuit |
|--------|-------------------|------------------------|----------------|---------------------|--------|------------|
| 1      | Ideal             | Ideal                  | No             | 56 = 00:00:56       | 1      | _20        |
| 2      | SPICE             | Ideal                  | No             | 830 = 00:13:15      | 15     | _21        |
| 3      | Ideal             | Ideal                  | Yes            | 5916 = 01:38:36     | 105    | _20X       |
| 4      | SPICE             | Ideal                  | Yes            | 9,277 = 02:34:37    | 166    | _21X       |
| 5      | SPICE             | SPICE                  | Yes            | 11,758 = 03:15:58   | 210    | _20X       |

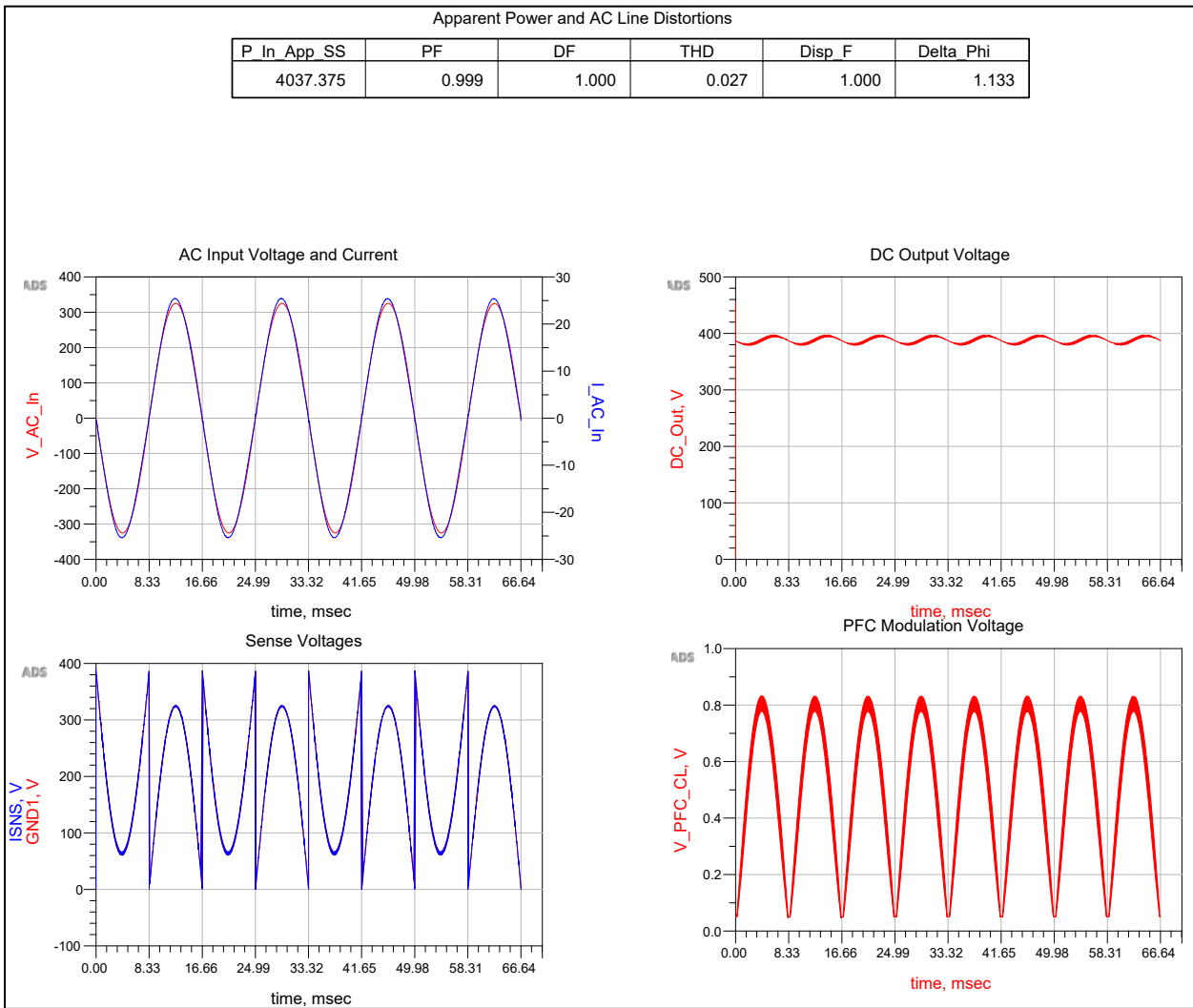
Running the test benches for the circuit models

1. Double-click schematic for AC\_DC\_Rectifier\_Test\_Bench\_21

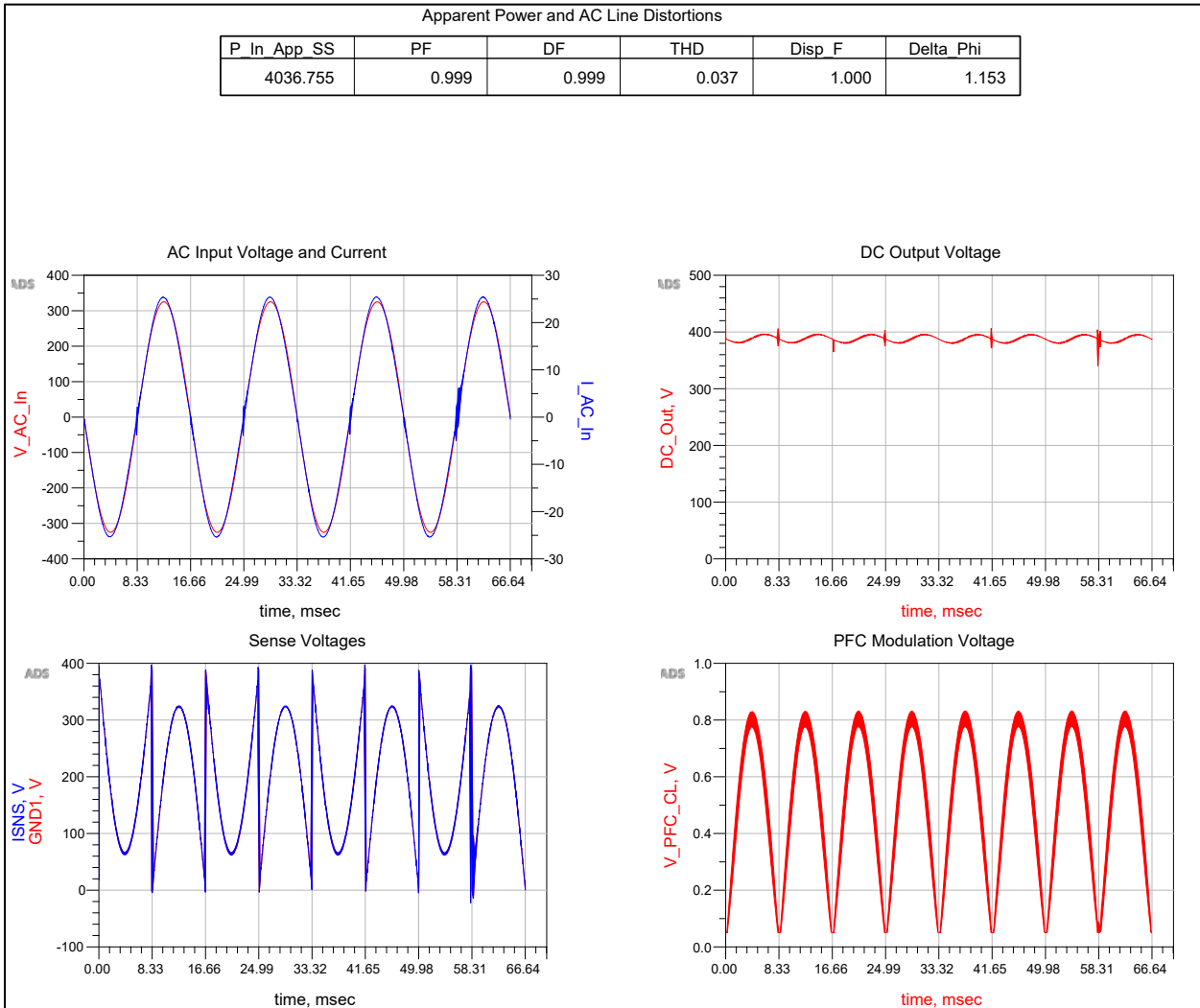




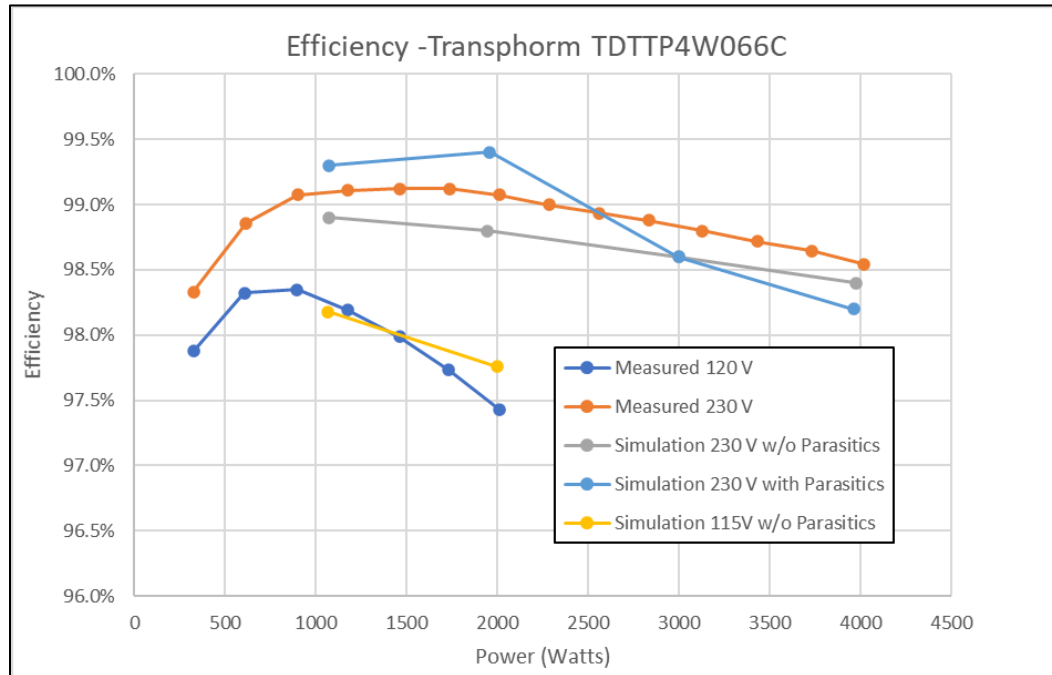
This simulation should take about 13 minutes on a 3 GHz CPU. After the simulation finished, the data display with the results will open automatically. A portion of the data display that summarizes the results is



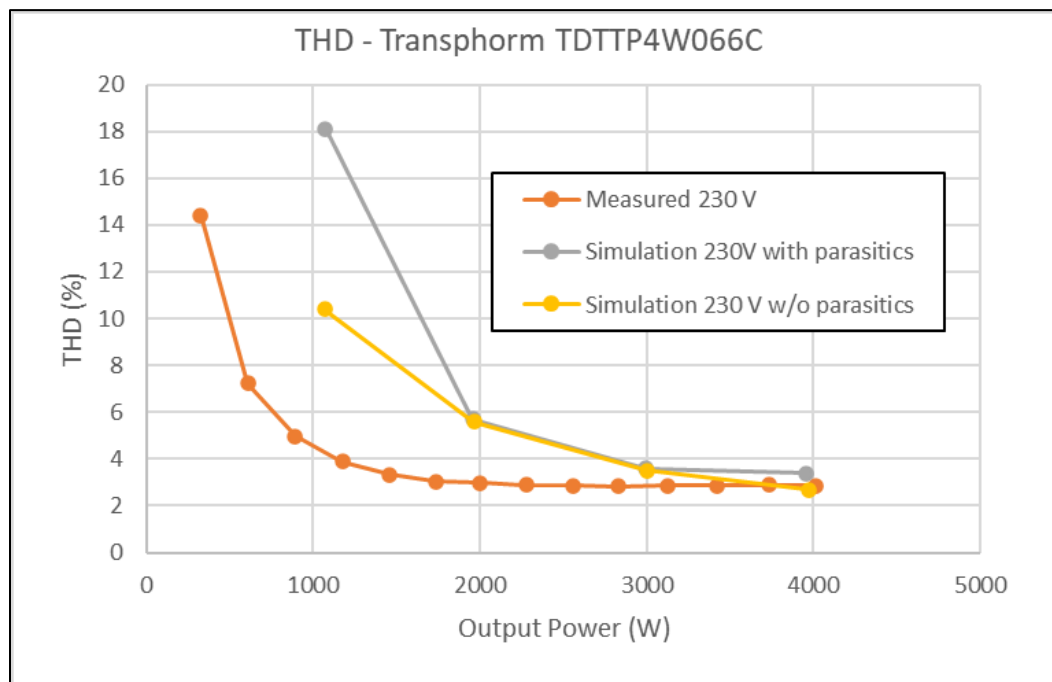
To run the simulation with the parasitics, disable the component “21” and enable “21X”. This simulation will take about 2 ½ hours on a 3 GHz CPU.



## Efficiency and Total Harmonic Distortion (THD)



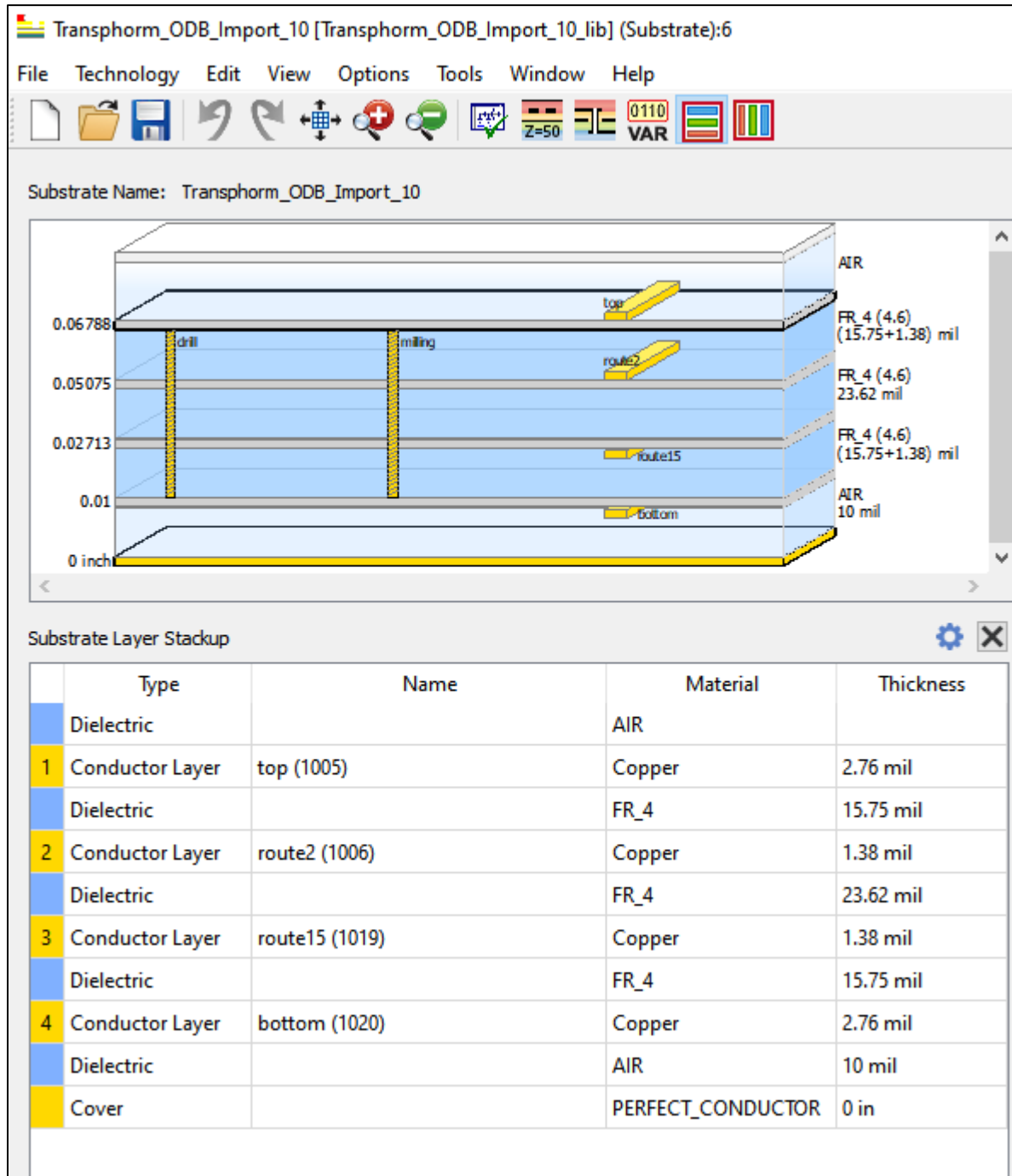
Efficiency – measured and simulated



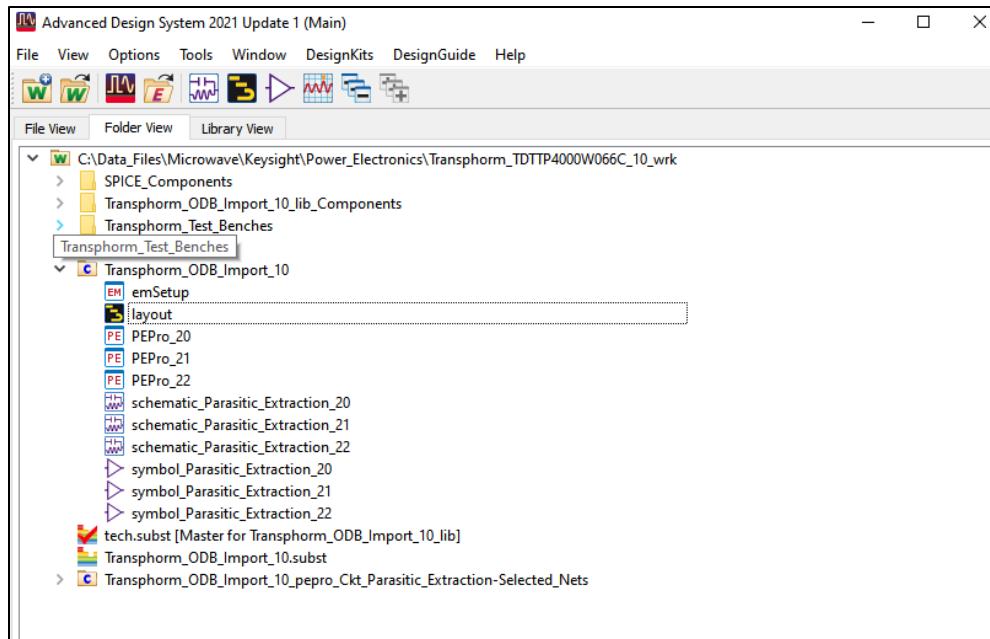
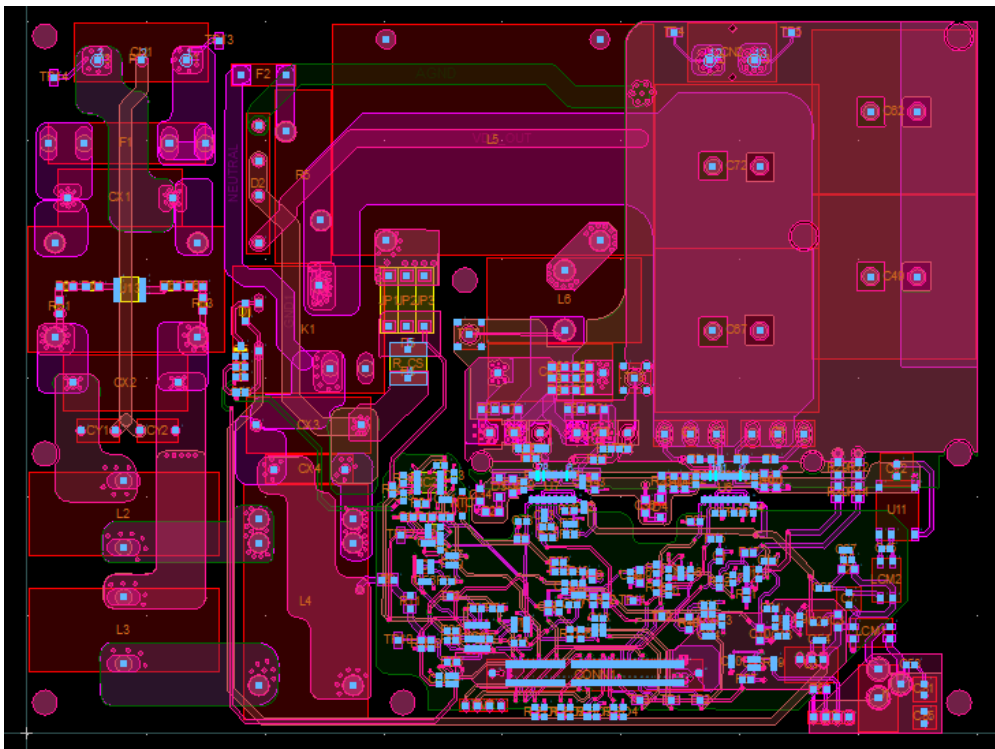
Total harmonic distortion – measured and simulated

## Viewing the details of the set-up

To see the substrate – click on “Transphorm\_ODB\_Import\_10.subst” in the main window. The bottom cover provides the ground reference for the parasitic extraction.



To see the layout – click on the layout icon in the “Transphorm\_ODB\_Import\_10” subdirectory in the main window.



The left panel can be set to view the “Navigator” or “Layers”

The Layers panel allows the setting of the visibility of the imported layers. It is set to view the four metal layers and the via (drill) layer.

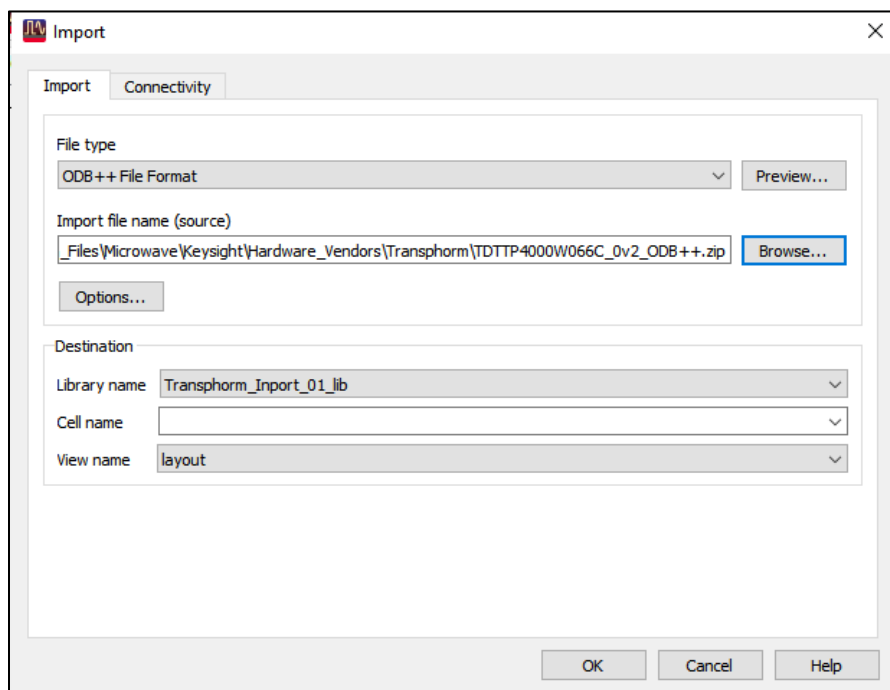
| Layer           | Fill                                                                              | Sel                                 | Vis                                 |
|-----------------|-----------------------------------------------------------------------------------|-------------------------------------|-------------------------------------|
| comp_pkg_top    |  | <input type="checkbox"/>            | <input type="checkbox"/>            |
| comp_pkg_bottom |  | <input type="checkbox"/>            | <input type="checkbox"/>            |
| comp_pkg_pad    |  | <input type="checkbox"/>            | <input type="checkbox"/>            |
| tcream          |  | <input type="checkbox"/>            | <input type="checkbox"/>            |
| tstop           |  | <input type="checkbox"/>            | <input type="checkbox"/>            |
| top             |  | <input checked="" type="checkbox"/> | <input checked="" type="checkbox"/> |
| route2          |  | <input checked="" type="checkbox"/> | <input checked="" type="checkbox"/> |
| route15         |  | <input checked="" type="checkbox"/> | <input checked="" type="checkbox"/> |
| bottom          |  | <input checked="" type="checkbox"/> | <input checked="" type="checkbox"/> |
| bstop           |  | <input type="checkbox"/>            | <input type="checkbox"/>            |
| bcream          |  | <input type="checkbox"/>            | <input type="checkbox"/>            |
| drill           |  | <input checked="" type="checkbox"/> | <input checked="" type="checkbox"/> |
| milling         |  | <input type="checkbox"/>            | <input type="checkbox"/>            |
| silk_screen     |  | <input type="checkbox"/>            | <input type="checkbox"/>            |
| silk_screen2    |  | <input type="checkbox"/>            | <input type="checkbox"/>            |
| ads_y8          |  | <input type="checkbox"/>            | <input type="checkbox"/>            |
| ads_drc_error   |  | <input type="checkbox"/>            | <input type="checkbox"/>            |

The Navigator panel allow allows for selection of the specific parts of the layout: nets, ports, components, traces, and geometry.

## Import of ODB++ file

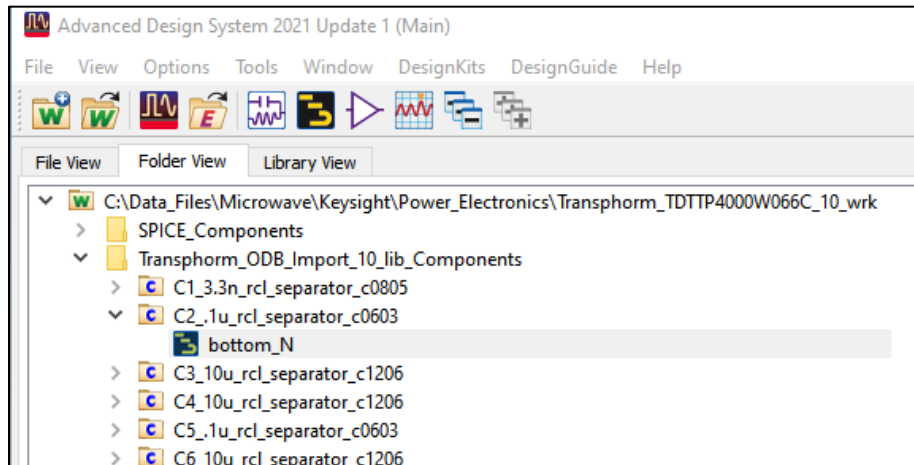
The ADS units needed to be changed to the ODB++ units before the import is performed. The requisite menu is found from the top ADS menu: Options->Technology->Technology Set Up.

Create a new ADS workspace and then import the ODB++ file using the import menu from the main menu.

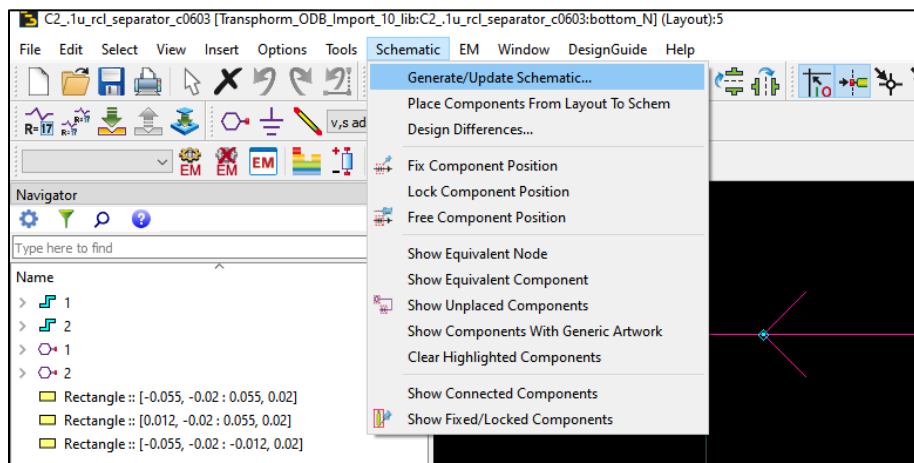


After the import is complete, check the layer configuration in the Substrate Editor to make sure it matches with the design.

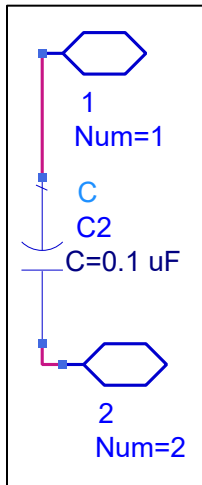
One limitation of importing a design into ADS instead of building the whole design from scratch in ADS is that circuit models for discrete components will not be imported. It is partially due to the input data format which does not contain much information about circuit model for each component. The user must create or import circuit models for each component to be used in the EM parasitic extraction. Click on the layout icon of the component model to be updated with a symbol and circuit.



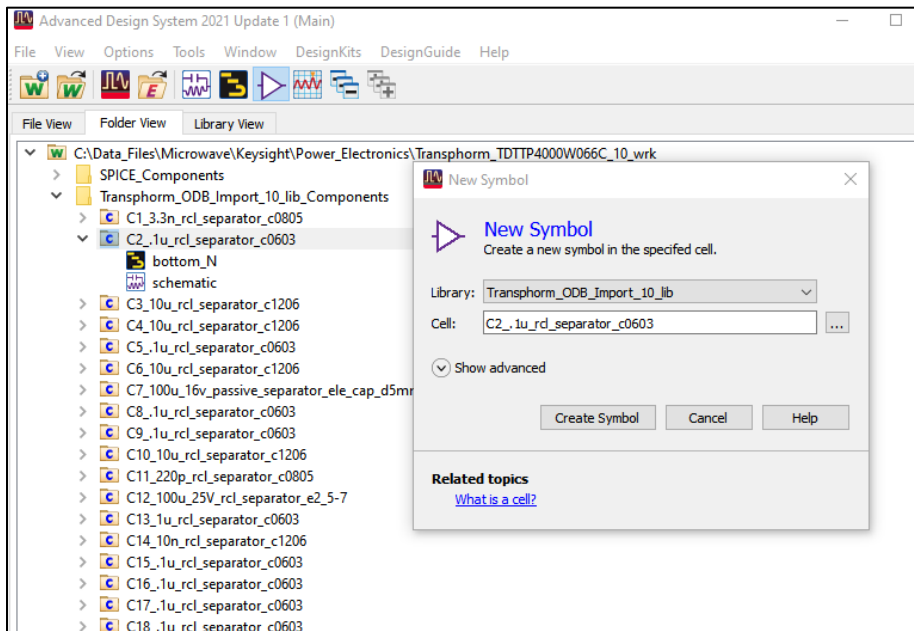
This will open the layout showing the pin positions of the component. Click on Schematic->Generate/Update Schematic.



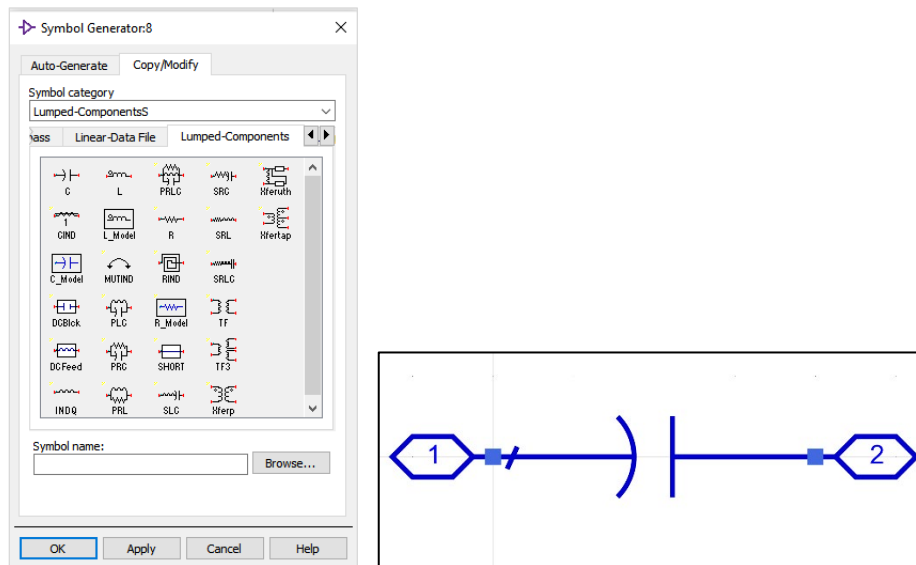
This will bring up a schematic with two ports. Add the circuit value (0.1 uF capacitor).



In the main menu select the component and add a symbol.



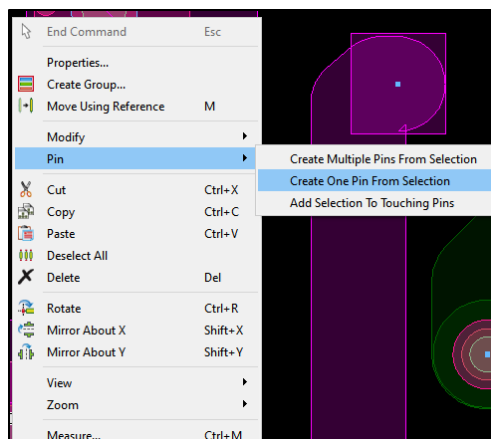
Used the copy/modify to select the correct symbol for the component.



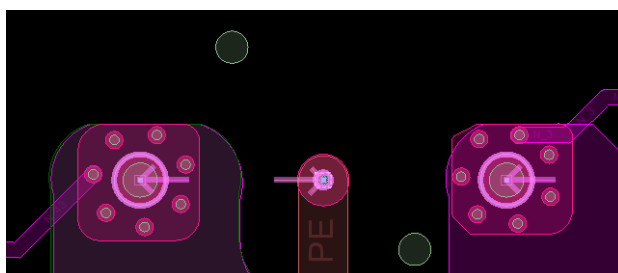
This process must be used for the components that are to be selected for the PEPro analysis. For active components, ideal switches or SPICE modes are used in the component model. For this Transphorm example, 31 or 37 components are used.

Finally, the Input/Output pins need to be inserted. This is done in layout prior to invoking PEPro.

Select the geometry about the pin location and then right click: select Pin->Create One Pin from Selection.

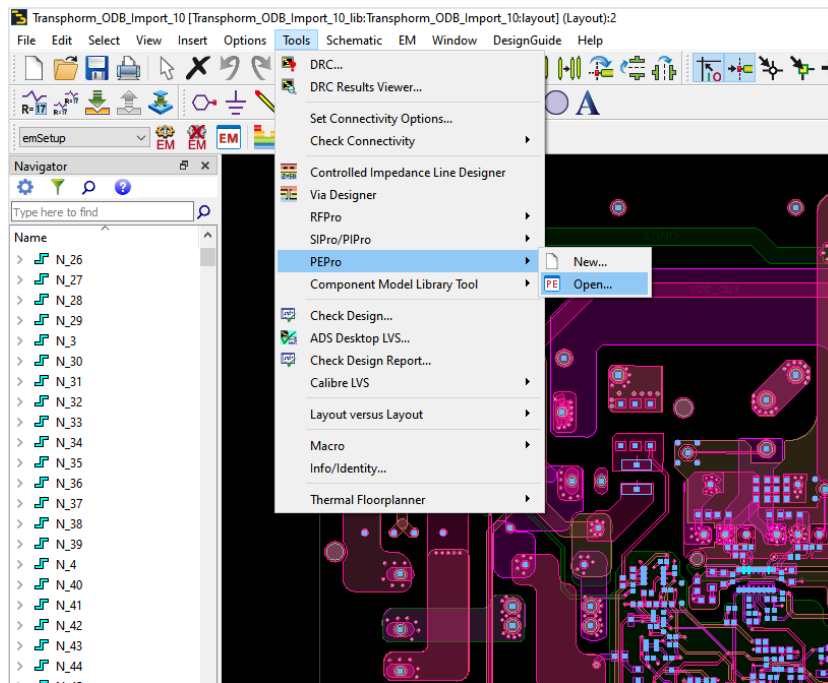


The AC input with the three pins is shown below.

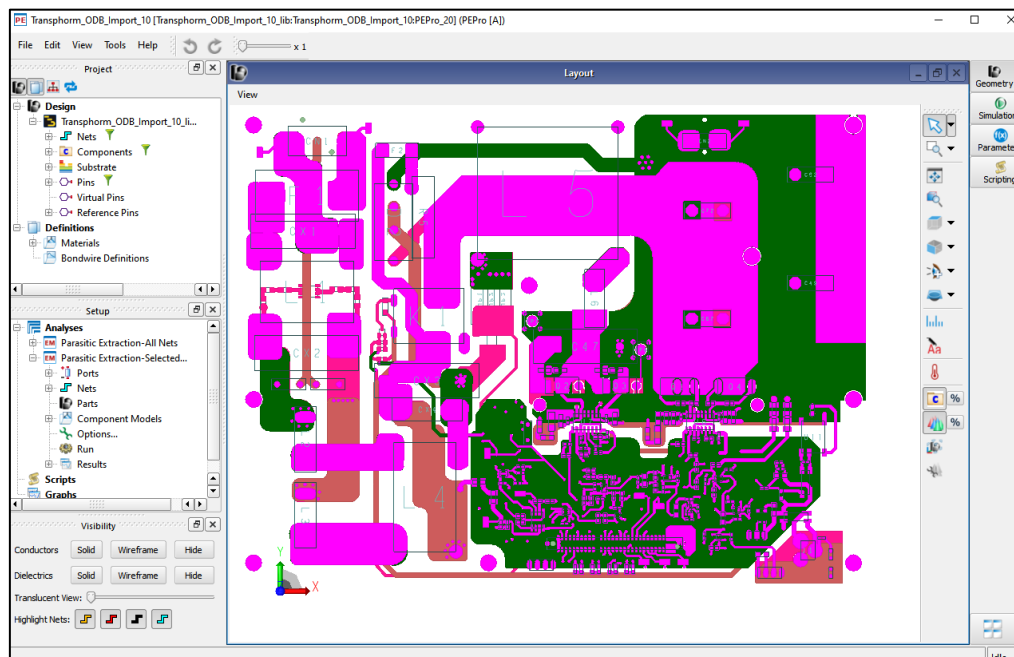


## PEPro setup

1. In the Layout window, click **Tools > PEPro > Open**



2. In the PEPro Main window, view the Project and Setup dockable sub-windows content.  
The Project sub-window contains all elements included in the layout that is nets, components, pins, and so on. The Setup sub-window is used for EM analysis of either entire design (Parasitic Extraction-All Nets) or only selected nets (Parasitic Extraction-Selected Nets).



## Component models, nets, options

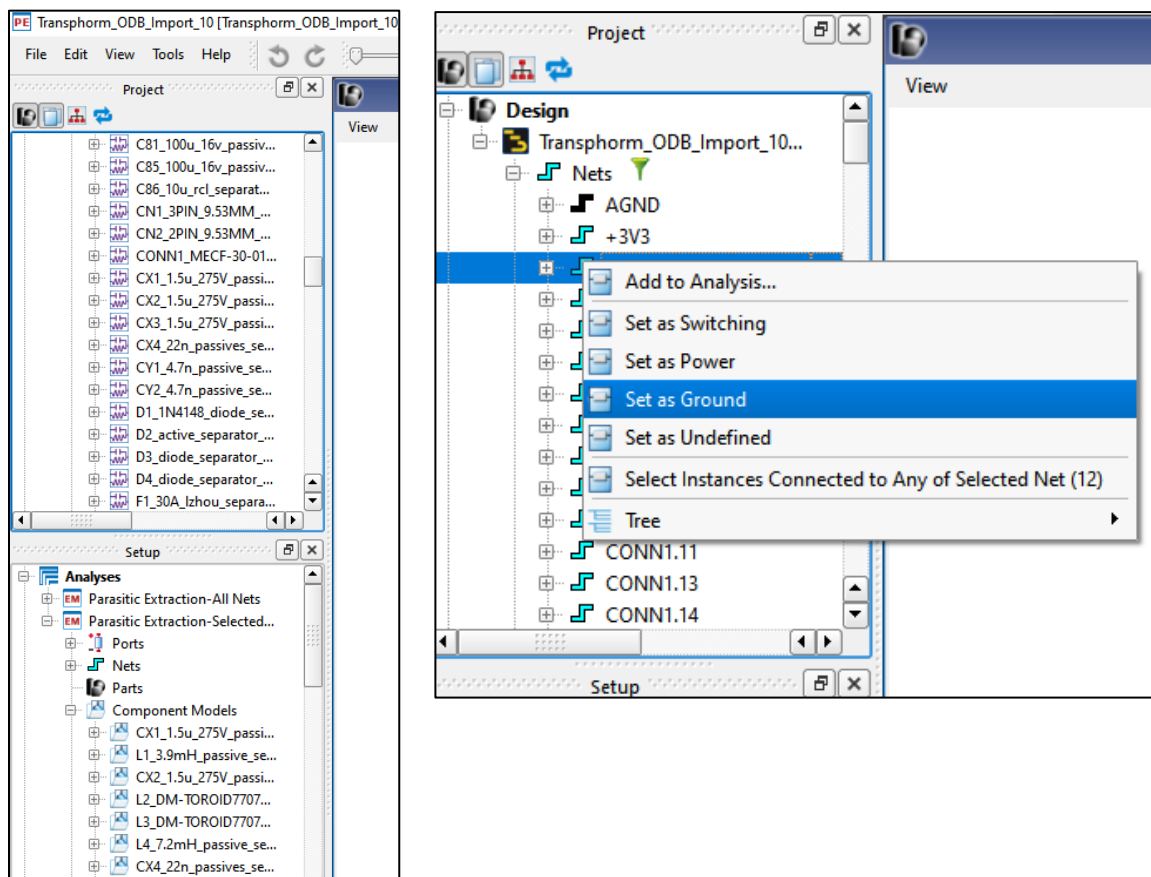
In the example, Ports, Component Models, Nets, Options have already been configured. You can double-click the **Run** button to run an EM Model Extraction. To understand the setup, read the details in the subsequent sections.

### Components setup

Select the component instances under Design > Components. Drag them to the Setup sub-window and drop onto Analyses.

### Nets setup

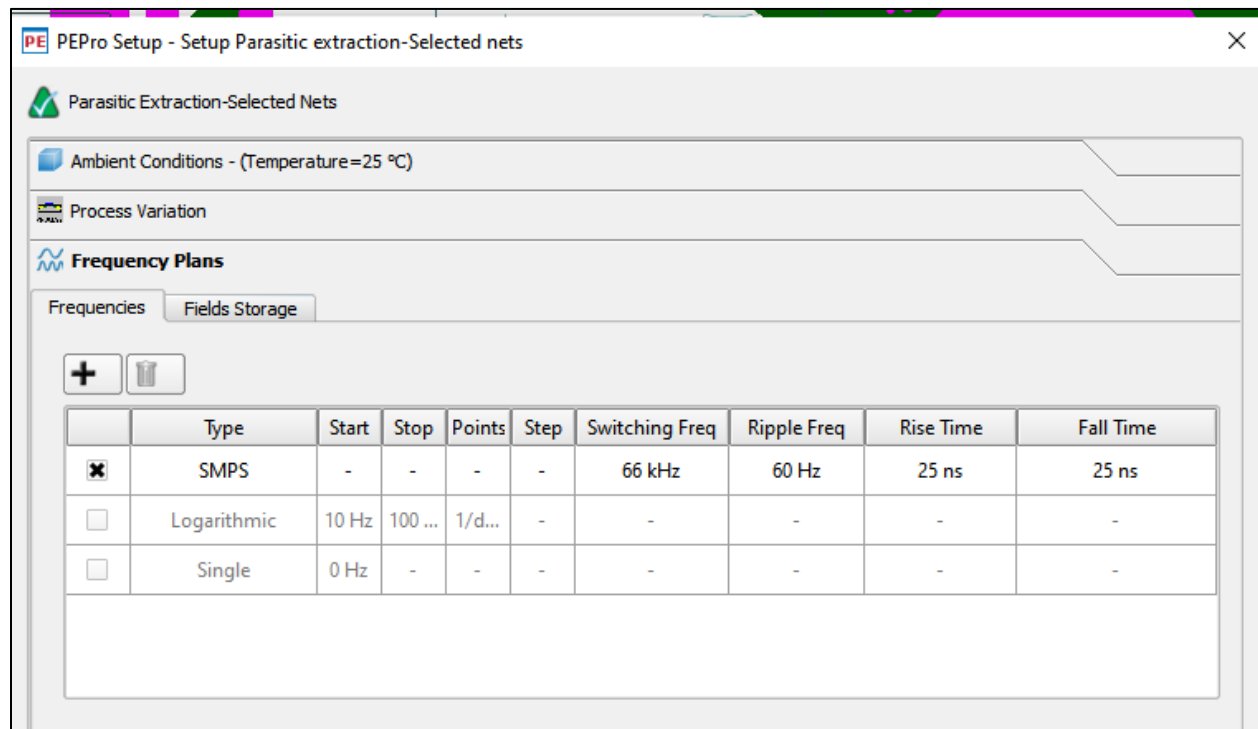
Select the nets under Design > Nets. Right-click and set them as Switching, Power, Ground or Undefined. Drag the selected nets to the Setup sub-window and drop onto the Analyses.



## Options setup

### Frequency plans

There are several types of frequency sweeps. For switched mode power converters, we use an automatic frequency plan for switched-mode power supplies (**SMPS**) in Power Electronics. It creates a composite frequency plan that can capture the most important EM features of a PCB in SMPS circuits. To use this plan, the user needs to provide circuit characteristics in the frequency plan table. Once the required input data is set, the frequency plan will be generated automatically and used in the subsequent EM simulation. For debugging, a simpler frequency plan can be chosen,

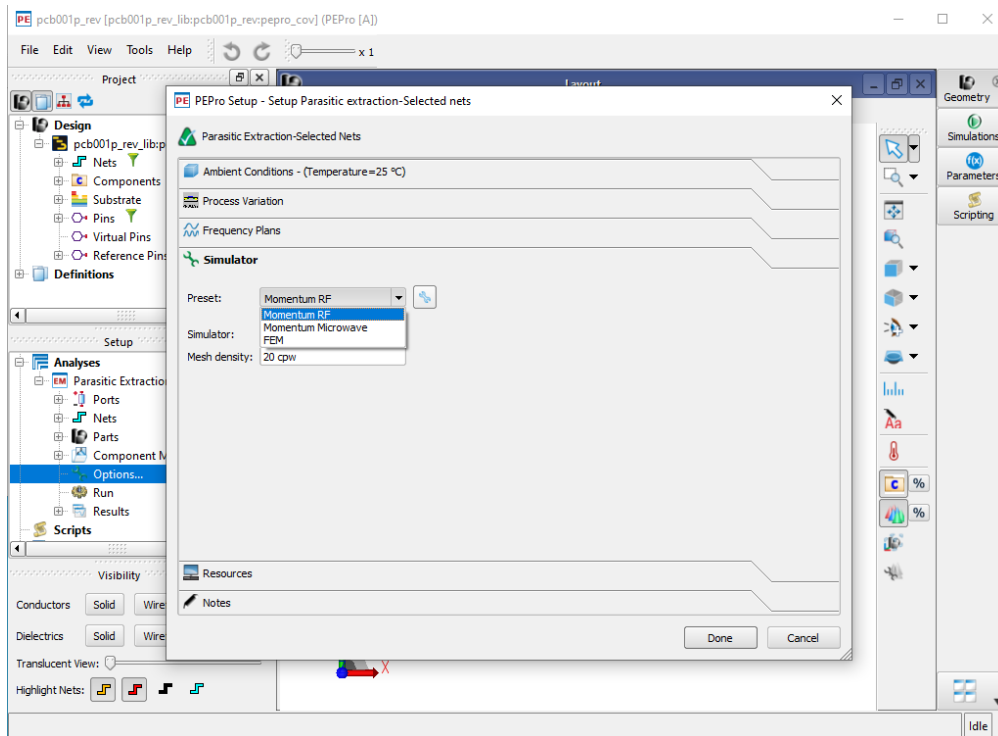


### Simulator

There are three **Simulator Presets** available:

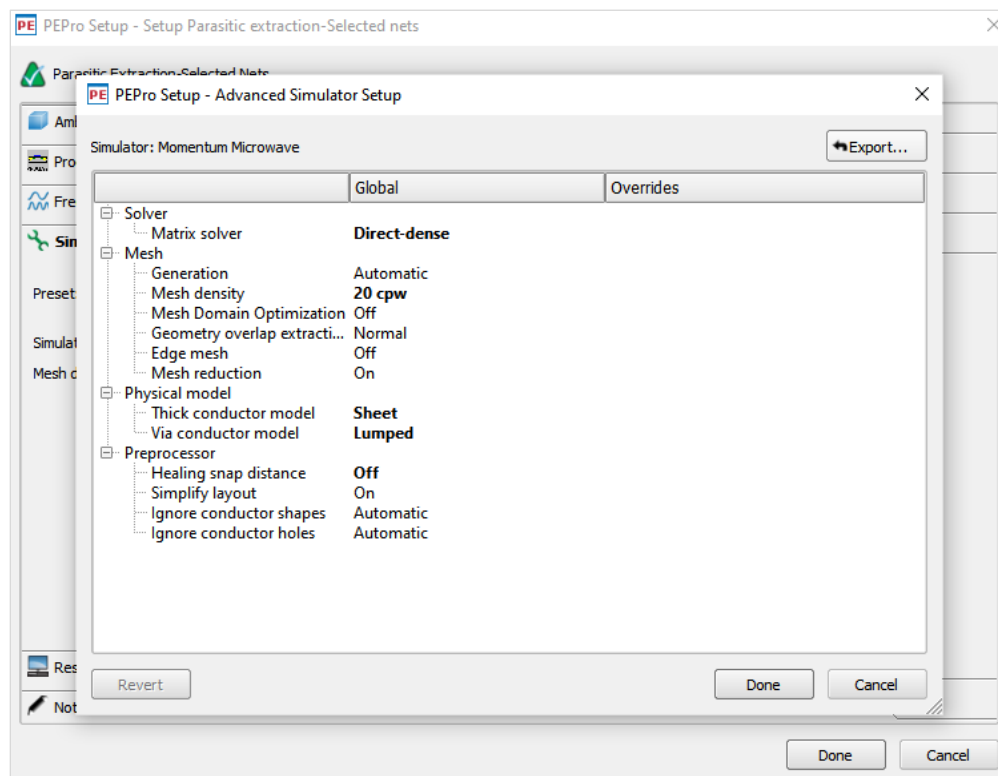
- Momentum RF
- Momentum Microwave
- FEM

Momentum RF provides the fastest EM simulation speed with good accuracy. Momentum RF is a fast, quasi-static 3D planar solver that is appropriate for SMPS PCBs and packages. The slower Momentum Microwave setting is intended for a different purpose, namely multi-gigahertz microwave circuits where the highest wavelength, that is, speed of light divided by highest frequency is physically much smaller than the size of the board. FEM is intended for objects with arbitrary 3D geometries such as connectors or boards with very high layer count.



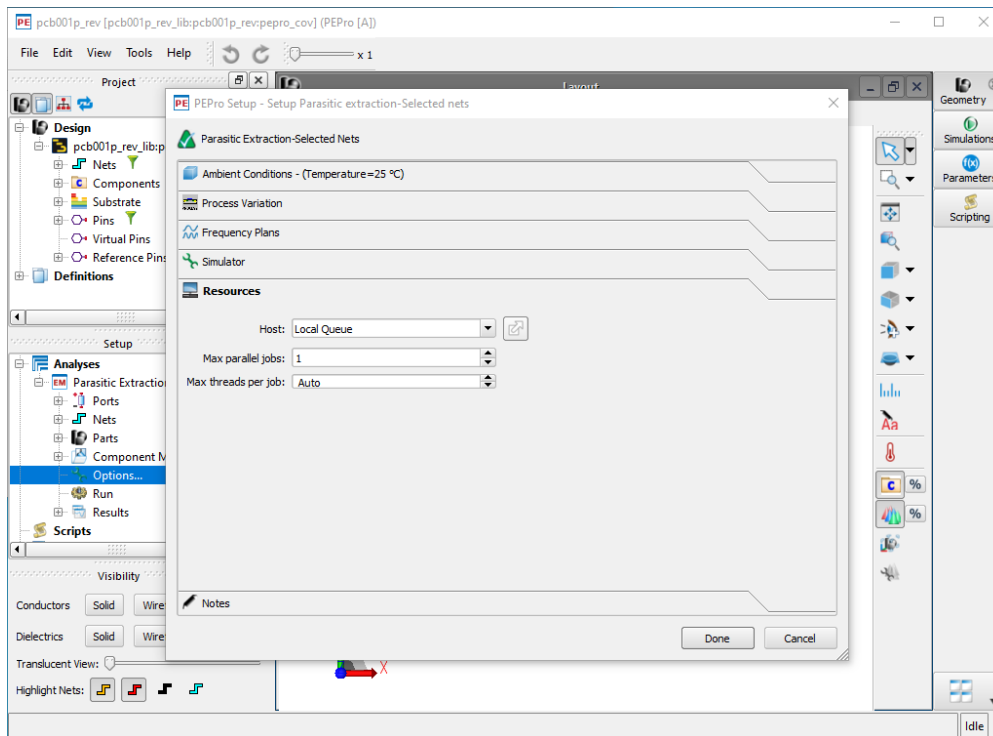
## Advanced simulator settings

Change the Physical model to “Thick conductor model -> **Sheet**” and “Via conductor model -> **Lumped**”



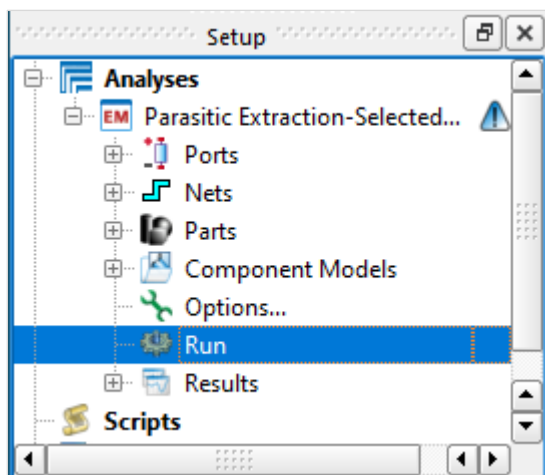
## Resources

You can run EM simulations on a local or remote host machine and benefit from faster simulation times.



## Running a PEPPro simulation

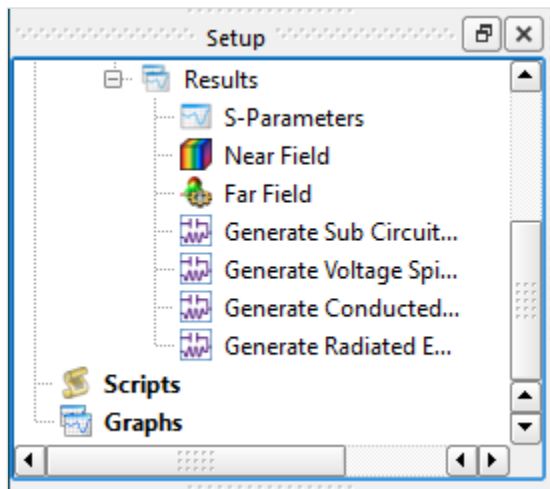
Double-click **Run** to start the EM simulation. The simulation takes several minutes depending on available computation resources. When the simulation completes, close the **Simulations** window.



## Results

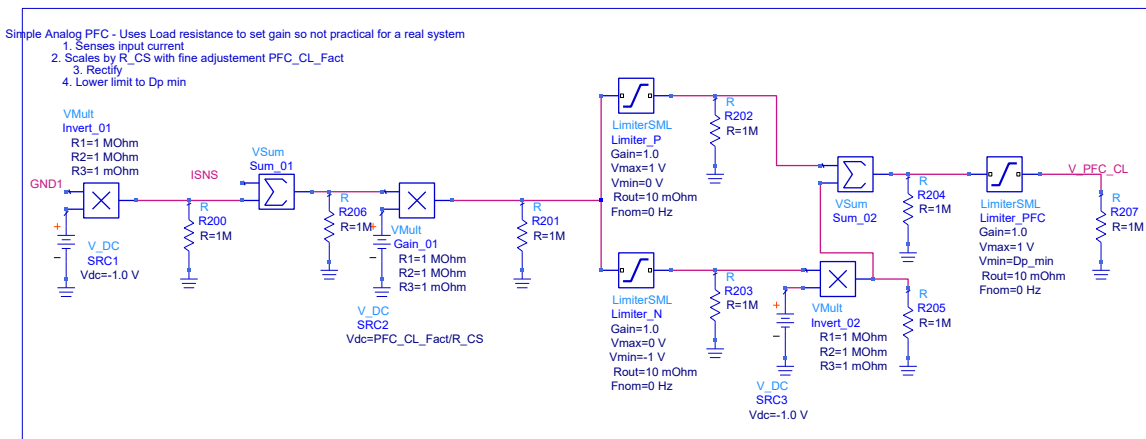
### Generate sub circuit

Once the simulation is complete, double click **Generate Sub Circuit** to generate an EM model that can be used in the EM-circuit co-simulation. If the sub circuit already exists in the workspace, it may overwrite with the new EM simulation data. The example already contains a sub-circuit named **schematic\_Parasitic\_Extraction-Selected\_Nets** and it will be overwritten(updated).

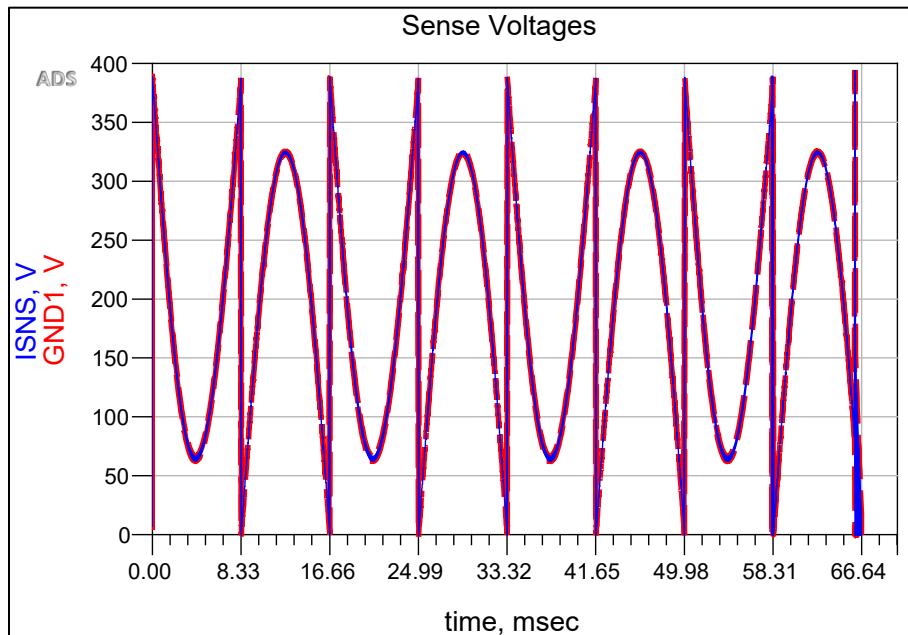


## Power factor control

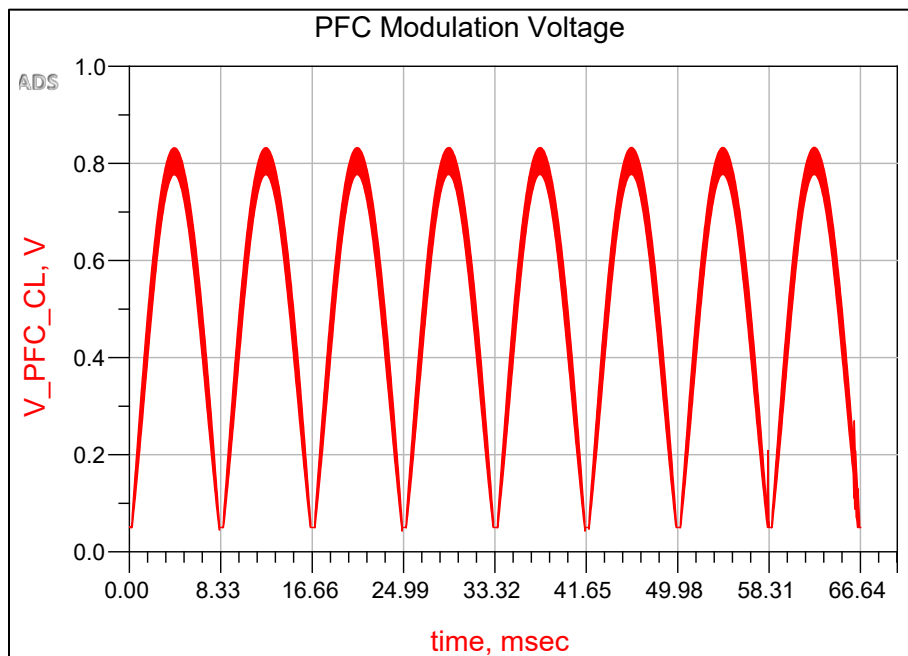
The AC-DC rectifier requires power factor control (PFC) to achieve high efficiency and low to total harmonic distortion (THD) on the AC current. The PFC is generally implemented with digital circuitry as is done on the Transphorm tdt4000w066c. However, simulating a mixed analog/digital circuitry would be even slower with SPICE models and parasitic extraction models. For faster simulation, an ideal analog PFC circuit was developed and is used in the test benches. This analog PFC works well at moderate and heavy loads. The ADS circuit is shown below.



Voltages on each side of the 4-milliohm sense resistor are



The generated PFC control voltage that is feed into the Pulse Width Modulator is



The PFC voltage peaks at the AC zero crossings and goes to a minimum at the peaks of the AC. The gain is proportional to the inverse of the sense resistor and a factor on the order unity. This factor is adjusted to insure a "flat" response over time.

Without PFC (constant PWM) the output is that of a diode bridge with a Power Factor of 0.69 and a Total Harmonic Distortion greater than unity.

## Theoretical efficiency – resistive loss only – CCM operation

Define the following variables.

|                |                                    |                                         |
|----------------|------------------------------------|-----------------------------------------|
| $V_{AC}^{RMS}$ | =                                  | AC Input Voltage (RMS)                  |
| $V_{AC}^{Pk}$  | $= \sqrt{2} V_{AC}^{RMS}$          | AC Input Voltage (Peak)                 |
| $F_{AC}$       | =                                  | AC Line Frequency                       |
| $T_{AC}$       | $= \frac{1}{F_{AC}}$               | AC Line Period                          |
| $D'_{min}$     | =                                  | Minimum value for AC zero crossing      |
| $D'_{max}$     | =                                  | Maximum value for AC peak voltage       |
| $D'_{RMS}$     | $= \sqrt{D_{min}'^2 + D_{max}'^2}$ |                                         |
| $D_{min}$      | $= 1 - D'_{max}$                   |                                         |
| $D_{max}$      | $= 1 - D'_{min}$                   |                                         |
| $D_{RMS}$      | $= 1 - D'_{RMS}$                   |                                         |
| $R_F$          | =                                  | Series Resistance in Common Mode Filter |
| $L$            | =                                  | Boost Inductor                          |
| $R_L$          | =                                  | Series Resistance in Boost Inductor     |
| $R_{QB}$       | =                                  | On Resistance of Boost Transistors      |
| $R_{QC}$       | =                                  | On Resistance of Commutator Transistors |
| $C$            | =                                  | Output Capacitor                        |
| $R_C$          | =                                  | Series Resistance in Output Capacitor   |
| $R_{Load}$     | =                                  | Load Resistance                         |
| $V_0$          | =                                  | Output Voltage                          |
| $V_{0,min}$    | =                                  | Minimum hold-up voltage ( 1 AC Cycle)   |

Then the efficiency due to the resistive losses is given by

$$\eta = \frac{1}{\left[ 1 + \frac{D'_{RMS} R_{Load} R_C + (D_{RMS} R_{QB} + R_{QC} + R_L + R_F)(R_{Load} + R_C)}{D_{RMS}^2 R_{Load}^2} \right]} \left( \frac{R_{Load} + R_C}{R_{Load}} \right)$$

This equation is implemented in the ADS data displays to compare with simulation.

The minimum gain ( $D'_{max}$ ) is set by peak AC voltage, the efficiency and the desired load voltage

$$D'_{max} = \frac{V_{AC}^{Pk} \eta}{V_0}$$

The maximum gain ( $D'_{\min}$ ) is set by the limitations of the PWM and is typically no more than  $\left(\frac{1}{0.05}\right)$

The average output voltage, inductor current and switch current are given by

$$V_0 = \frac{\sqrt{2}}{D'_{RMS}} V_{AC}^{RMS} \eta \quad I_L^{RMS} = \frac{1}{D'^2_{RMS}} \frac{V_{AC}^{RMS}}{R_{Load}} \eta \quad I_Q^{RMS} = D_{RMS} I_L$$

The AC input power and DC output power are given by

$$P_{in} = \frac{(V_{RMS}^{AC})^2}{D'^2_{RMS} R_{Load}} \eta \quad P_{out} = \frac{(V_{RMS}^{AC})^2}{D'^2_{RMS} R_{Load}} \eta^2$$

It is convenient to have the currents written in terms of the output power. This can be accomplished by first writing the load resistance as a function of output power and then substituting back into the current equations.

$$I_L^{RMS} = \frac{P_{out}}{V_{AC}^{RMS} \eta} \quad I_Q^{RMS} = \frac{D_{RMS} P_{out}}{V_{AC}^{RMS} \eta}$$

The power dissipated in the common mode filter resistance is given by

$$P_{R_{CMF}} = \frac{(V_{RMS}^{AC})^2}{D'^4_{RMS} R_{Load}^2} R_{CMF} \eta = R_{CMF} \left( \frac{P_{out}}{V_g \eta} \right)^2$$

The power dissipated in the inductor resistance is given by

$$P_{R_L} = \frac{(V_{RMS}^{AC})^2}{D'^4_{RMS} R_{Load}^2} R_L \eta = R_L \left( \frac{P_{out}}{V_g \eta} \right)^2$$

The power dissipated in the capacitor resistance is given by

$$P_{R_C} = \frac{D_{RMS} (V_{RMS}^{AC})^2}{D'^3_{RMS} R^2} R_C \eta = P_{out} \left( \frac{D_{RMS}}{D'_{RMS}} \right) \left( \frac{R_C}{R_{Load} + R_C} \right)$$

The power dissipated by each switch boost transistor's "on" resistance is given by

$$P_{R_{QB}} = \frac{D_{RMS} (V_{RMS}^{AC})^2}{2D'^4_{RMS} R_{Load}^2} R_{QB} \eta = R_{QB} D_{RMS} \left( \frac{P_{out}}{V_g \eta} \right)^2$$

The power dissipated by each commutator transistor's "on" resistance is given by

$$P_{R_{QC}} = \frac{(V_{RMS}^{AC})^2}{2D'^4_{RMS} R_{Load}^2} R_{QC} \eta = R_{QC} \left( \frac{P_{out}}{V_g \eta} \right)^2$$

The RMS input impedance is the ratio of the RMS input voltage to the RMS inductor current

$$Z_{I_{RMS}} = \frac{RD_{RMS}^2}{\eta} = \frac{(V_{RMS}^{AC})^2 \eta}{P_{out}}$$

The output impedance (open loop) is

$$Z_{O_{RMS}} = \frac{1}{D_{RMS}^2} (R_L + R_{CMF} + D_{RMS} R_{QB} + R_{QC} + R_{QC}) \eta$$

The voltage ripple due to the AC line frequency is given by

$$\Delta V_0^{AC} = \frac{P_{out}}{2\pi F_{AC} C V_0} = \frac{V_{AC}^{RMS} \eta}{D_{RMS}' 2\pi F_{AC} R_{Load} C}$$

This is easily inverted to provide the required capacitor for a given voltage ripple

$$C_{Ripple} = \frac{P_{out}}{2\pi F_{AC} V_0 \Delta V_0^{AC}} = \frac{V_{AC}^{RMS} \eta}{D_{RMS}' 2\pi F_{AC} R \Delta V_0^{AC}}$$

Another requirement that drives the capacitor size is the minimum allowed voltage after a specified length of time after loss of power. Typically, the hold-up time is specified in terms on one AC cycle (16.67 ms or 20.0 ms).

$$V_{0,min} = \sqrt{V_0^2 - \frac{2P_{out} T_{AC}}{C}} = V_0 \sqrt{1 - \frac{2T_{AC}}{RC}}$$

This is easily inverted to provide the required capacitor for a specified minimum hold-up voltage ( $V_{0,min}$ )

$$C_{Hold\_Up} = \frac{2P_{out} T_{AC}}{V_0^2 - V_{0,min}^2} = \frac{2T_{AC}}{R \left( 1 - \frac{V_{0,min}^2}{V_0^2} \right)}$$

The output capacitor is then the maximum of the two

$$C \geq \max(C_{Ripple}, C_{Hold-Up})$$

This large capacitor used to minimize the AC voltage ripple and maximize hold-up time will in general have a self-resonance below the switching frequency. Therefore, additional much smaller parallel bypass capacitors will be needed to minimize the switching frequency ripple on the output.

With modern semiconductors and low switching speeds the dominant loss in CCM is resistive. As the load gets higher and the power gets lower, over part of the AC cycle the boost converter circuit is operating in DCM. These equations are no longer valid and in general the efficiency will decrease.

## Notes:

- A. The main boost inductor (L5) in general has a large winding capacitance that can induce high frequency switching noise back up the common mode filter to the AC line. The way to minimize this coupling is to add a small series inductor (L6) which has a much smaller winding capacitance to block this noise.
- B. In this workspace, the initial voltage was set to a hard-coded value at each of the 4 output capacitors. This was done to reduce simulation time.

# Design Space Exploration and “What if...?” Analysis

In contrast to a sequence of expensive and time consuming “solder-and-see” physical prototypes, the virtual prototype is more cost-effective for exploring the design space and performing “What if...” analysis. For example, the reference design as-is may be close to what you need, but not an exact match. But if you modify it you run the risk of introducing unwanted side effects like excessive voltage spikes and EMI problems. The virtual prototype gives you insight on how to change it while minimizing side effects. Try replacing some of the components with lower cost, lower performance ones. An example would a capacitor with higher series inductance or resistance and hence a lower self-resonant frequency. Next try re-routing the PCB traces, especially those in the switched loop that has high di/dt trapezoidal waveforms. See how the ringing and EMI are affected.

## Conclusion

Virtual prototypes like this one are complementary to physical prototypes. Physical prototypes are the gold standard for compliance and measured characteristics of course but they have several drawback:

- Expensive and time consuming to design, build, and measure
- Vulnerable to catastrophic failure – the infamous smoke test that produces actual smoke
- Hard to get a measurement probe onto interior nodes so you can’t really see what is going on inside

In contrast, virtual prototypes are easy to change and while they do indicate device overstress, they never emit real smoke. The voltage, current, and fields at every spatial point in the 3D grid and every time step in the simulation can be recorded and made accessible for plotting, even point that are physical inaccessible in the real world such as inside a semiconductor package.