

Virtual Reference Design from Wolfspeed

PathWave ADS Workspace for
Wolfspeed Kit-CRD-HB12N-J1

This application note serves as a guide to use a PathWave ADS workspace to simulate a virtual version of a physical reference design from Wolfspeed Model CRD-HB12N-J1. This model showcases the Silicon Carbide (SiC) power transistors (C3M0032120J1 series) from Wolfspeed. This guide provides instructions on how to start building your next-generation switched-mode power supply. The reference design – in both virtual and physical forms - are a good starting point for your own project.

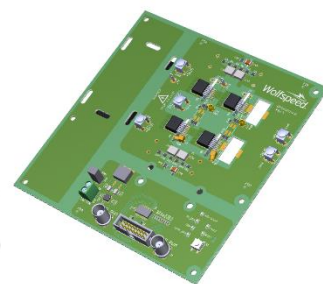


Figure 1. Wolfspeed CRD-HB12N-J1 Half-Bridge

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Dependencies/Pre-requisites from Keysight

Step 1: Download and Install the PathWave ADS binaries

1. Go to <http://www.keysight.com/find/eesof-ads-latest-downloads>.
2. Download the ADS installation file(s):
64-bit: ads_20XX_win_x64.exe
to any folder, for example C:\Temp.

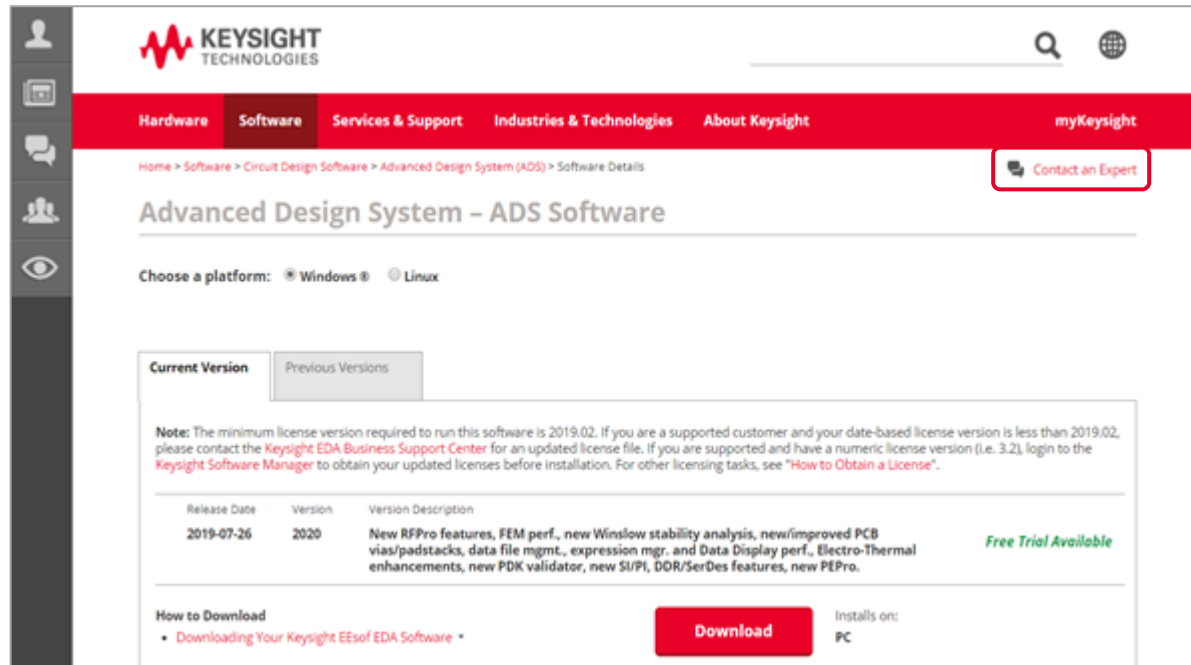


Figure 2. Downloading ADS software

NOTE: If you need any assistance, click Contact an Expert to reach out to an expert.

Step 2: Request a No-charge 45-days Evaluation License

Go to <http://www.keysight.com/find/eesof-ads-evaluation>.

Step 3: Download the workspace

Download the reference design workspace here.

Installing Advanced Design System (ADS)

To install Advanced Design System on Windows, follow these steps.

1. Run the downloaded installation file from the location where you saved it.
Before starting the installation, the installation file extracts all the necessary files in a temporary folder.
2. Select the language from the drop-down list of Installation window and click OK to continue.
3. On the Introduction screen, click Next to read the License Agreement. This is only a usage agreement and is not related to the licenses required to run the software.
4. On the License Agreement screen, accept the agreement and click Next.
5. On the Choose Install Set screen, choose any one of the two installation options:
 - **Complete:** For complete ADS installation. It requires about 4.5 GB of disk space and installs the ADS design environment, simulators, documentation, examples, and design guides. If you choose **Complete** installation, skip the next step.
 - **Custom:** For custom ADS installation where you can choose from the ADS items you want to install.
While you can choose which ADS items you want to install, the ability to run them is determined by the purchased licenses.
6. For custom installation, the next screen lets you choose the items you want to install. Click any item name to see the description of the same in the window. Select the items you want to install and click **Next**.

You must choose to install *ADS programs and tools* which includes *Layout, Simulators and Schematic Capture*; else ADS will not run properly. *Manuals & Help* is selected by default to install the entire ADS documentation set. If you uncheck this item, documentation and help files will not be available regardless of which other items you choose.

7. At the Choose Install Folder screen, click:
 - **Next** to install to the default folder. The installation program creates this folder if it does not already exist. One more option **Restore Default Folder** is also provided to restore the default folder after every uninstallation.
 - **Choose** to specify a different destination folder. If you specify a folder that does not already exist, the installation program will create it for you. The default folder for ADS installation is:
64-bit:"C:\Program Files\Keysight\ADS20XX"
You can change the default location and select your own desired path. Ensure that you must have permissions to write to the disk drive on which you want to install ADS. The installation also adds entries to your PC's Windows Registry, so ensure that you have permissions to do so.
8. At the Set Your Home Directory screen, click:
 - **Next** to accept the default.
 - **Choose** to select a different folder. The folder you specify will be the default startup folder for ADS. It will also be used to store the configuration data in a subfolder called hpeesof. For every single release and sub-release of ADS (such as ADS 2012.08, ADS 2013.06,

ADS 2014.01, ADS 2015.01 and ADS 2016.XX), you must choose a new *Home* folder for each version. For the best performance, choose a folder on your local, not network drive.

9. At the Choose Shortcut Folder screen:

- You can type a name in *Start Menu Folder Name* to have the same named folder in Start menu, by default it is Advanced Design Systems 2016.XX.
- If you want ADS icon on desktop, check the *Icon To Desktop* option.

10. At the Pre-Installation Summary screen, review your choices, and click:

- **Previous** to access previous screens to verify entries and make changes. This screen appears again if you go back to make other choices.
- **Install** to start the installation. Immediately after you click **Next**, the *Setup Status* screen appears, and the program configures the installation process. When the program determines that your system is ready for installation, it begins to install files. The status screen displays the files being installed and the progress.
- **Cancel** to exit the Setup without completing the installation.

11. After installation, click **Done** to quit the installer. The ADS License Setup Wizard starts automatically after this and check for the license status. Before launching ADS, you must complete the ADS license setup.

Setting Up Licenses on Windows

This section describes how to set up a node-locked license or a floating (network) license on Windows.

Both node-locked and floating licenses require license server to get installed and started. For a node-locked license, license server and the client machine are the same machine (that is, your local machine). For a floating license, these can be separate machines.

Setting Up Floating Licenses on Windows

Setting up floating licenses on Windows is a two-step process where both server-side setup and client-side setup are needed.

Step 1: License Server Setup

To setup a dedicated floating license server that has no Keysight EDA software installed, you will need to download and install the EEsof EDA License Server Software. This will install the license daemons and utilities needed to configure and start the license server.

Repeat the following steps for each license server you have.

Step 2: Client Setup

Once the license is configured successfully for all the license servers, configure each client computer to point to the network license server. **License Setup Wizard** offers the easiest method to get this done. Alternatively, you can perform this step manually by following step 3 of Setting up Node-locked License on Windows section. Make sure to specify the network license server in the format of **port@host.domain** or if no static TCP port is used on the license server, use the format **@host.domain**.

Examples

27001@myServer.myCompany.com
@myServer.myCompany.com

In case a license server is down or is running slow, it is recommended to remove it from the server list using the **License Setup Wizard** to avoid any performance degradation caused by the dead/slow servers.

Setting Up Node-locked License on Windows

On Windows, the License Setup Wizard offers the easiest way to set up your node-locked license. We strongly recommend you use the **License Setup Wizard**, especially when you have multiple Keysight EEsof products installed on one computer. For more information, refer to Quick Install-Windows. This section describes how to set up a node-locked license manually, should you decide not to use the **License Setup Wizard**.

Do not perform manual setup steps with the **License Setup Wizard**. Choose one method or the other. **License Setup Wizard** may not be able to replace what you set up manually due to Administrator Privilege differences.

The following instructions assume that you have already installed **Keysight EEsof Licensing Tools** in *C:\Program Files\Keysight\EEsof_License_Tools* folder. In case you have not yet installed the tools, run the Keysight EEsof Licensing Tools installer on the machine to which the license is tied to.

- If you have installed an EEsof product released before 1stAugust, 2014 on your system prior to installing an EEsof product released after 1st August 2014 then the default EEsof Licensing tools path will remain C:\Program Files\Agilent\EEsof_License_Tools. On the systems that only have EEsof products released after 1stAugust, 2014 installed then the default EEsof Licensing tools path will be C:\Program Files\Keysight\EEsof_License_Tools.
- Make sure to save the license file on the same machine where you install the Keysight software.

The following 3-step process shows how to manually set up a counted license that is tied to a CPU ID.

Step 1: Start License Server Managers

Start the FlexNet license server managers (**lmgrd** and **agileesofd**) on the computer to which the license is tied as follows:

1. Open the MS-DOS command prompt and change directory to the following path:*C:\Program Files\Keysight\EEsof_License_Tools\bin*.
2. Specify the full path and location of the license file and the license log file, respectively, by typing the following command:
lmgrd.exe -c <license file path> -l <license log file path> where,
 - <license file path> specifies one or more full pathnames to the license file(s).
 - <license log file path> is the full pathname to the debug log file.

The spaces in pathnames requires double quotes around the path-names.

Example

```
lmgrd.exe -c "C:\Program Files\Keysight\EEsof_License_Tools\licenses\license.lic" -l  
"C:\Users\Public\my_server_log.txt"
```

Step 2: Create Windows Service

To automate the restart of the license server managers upon PC reboot, configure a Windows Service as follows:

You must have Administrator Privileges to configure a Windows Service. The service will run under the Local System account.

1. Run the *lmtools.exe* from *C:\Program Files\Keysight\EEsof_License_Tools\bin*. The *lmtools* utility window is displayed.
2. In the Service/License File tab, select the Configuration using Services option.
3. Click the Config Services tab and enter the following details:
 - **Service Name:** Type the service name (for example, EEsof EDA License Server).
 - **Path to the lmgrd.exe file:** Click **Browse** and specify the path to the *lmgrd.exe* file on the license server (for example, *C:\Program Files\Keysight\EEsof_License_Tools\bin\lmgrd.exe*).
 - **Path to the license file:** Click **Browse** and specify the path to the license file on license server (for example, *C:\Program Files\Keysight\EEsof_License_Tools\licenses\license.lic*).
If you have multiple license files for serving multiple Keysight EEsof products, you should include them all.
 - **Path to the debug log file:** Click **Browse** and specify the path to the debug log file on license server (for example, *C:\Users\Public\my_server_log.txt*).
4. Select the **Use Services** option.
5. Select the **Start Server at Power Up** option.
6. Click **Save Service**.
7. To verify that the service is created, click the **Start/Stop/Reread** tab and observe that your service shows up in the **FlexNet license services installed on this computer** list.
To verify if the license managers are running, click again on the **Config Services** tab later and click **View Log**. A log window appears that confirms whether *lmgrd* and *agileesofd* are up and running.

Step 3: Set Product Environment Variable

Set the environment variable <PRODUCT>_LICENSE_FILE to point the machine running the license server managers (*lmgrd* and *agileesofd*).

1. Select **Start > Control Panel > System**. Click **Advanced system settings**. The **System Properties** dialog box appears, and the **Advanced** tab is selected by default).

2. Click **Environment Variables**.
3. In the **Environment Variables** dialog box, add the product specific environment variable <PRODUCT>_LICENSE_FILE as a new system variable. For example, for SystemVue, it is **SYSTEMVUE_LICENSE_FILE**, for ADS, it is **ADS_LICENSE_FILE**, for EMPro, it is **EMPRO_LICENSE_FILE** and so on.
4. In the **New System Variable** dialog box, set the value to be the same as what you specified in the --c argument when you start *Imgrd* . To use the example illustrated in **Step 1**, second bullet, this value would be *C:\Program Files\Keysight\EEsof_License_Tools\licenses\license.lic*.
5. Repeat 3 and 4 for each Keysight EEsof product you have installed on your computer.

Launching Advanced Design System (ADS)

To start Advanced Design System (ADS), click **Start > Advanced Design System 201x.xx** from the taskbar.

- For existing ADS users, ADS starts normally.
- For a new ADS user, The Welcome to the Advanced Design System screen is displayed with two options:
 - **New to ADS** - Starts ADS Quick Start, which enables new users to discover the basics of ADS quickly.
 - **Familiar with ADS** - Starts ADS in normal mode and enables you to explore all the powerful and advanced ADS capabilities.

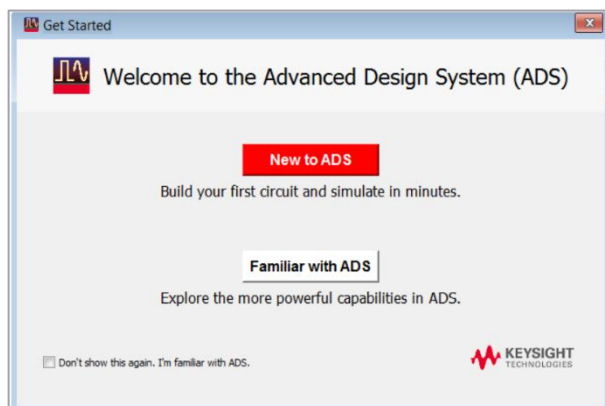


Figure 3. Getting started

ADS Quick Start Mode Highlights

- **First-time User Detection:** ADS Quick Start mode is enabled by default for the first time ADS users. It can be enabled or disabled in the ADS (Main) preferences.
- **Simplified Experience:** Skips all the startup screens and wizards of the standard mode.
- **Overlay Tips:** Provides quick steps for getting started effectively with circuit drawing, setting up simulation, and plotting/viewing results.

- Missing Step Detection: Displays messages when critical steps have been missed such as placing a Simulation Controller or in some case a Source.

Tips to Invoke ADS Quick Start Mode

For New User	For Existing User
When ADS starts, the Welcome to the Advanced Design System screen is presented. To turn off the screen: Check the "Don't show this again." on the lower left corner of the screen. or From ADS Main window, click Options > Preferences and uncheck the "Enable Quickstart" checkbox.	ADS starts normally. To enable ADS Quick Start: Type ads -quickstart from the command prompt. or Create a new ADS shortcut that calls ads -quickstart. or From ADS (Main) window, click Options > Preferences and check the "Enable Quickstart" checkbox

Download the Workspace

<https://www.keysight.com/find/wolfsspeed-workspace-download>

Unarchiving the Advanced Design System (ADS) Workspace

To unarchive the workspace:

1. Click File > Unarchive.
2. Click File > Unarchive.
The Select an Archive File browse window is displayed.

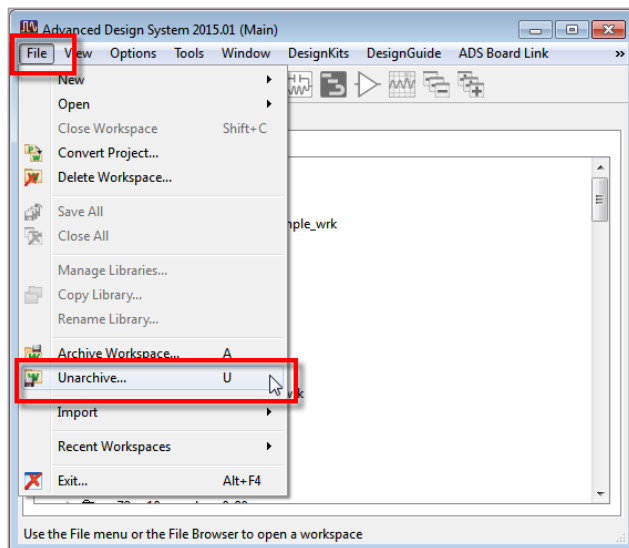


Figure 4. Select an Archive

3. Browse to the folder where you downloaded the workspace.
4. Click Open.
The Unarchive wizard is displayed.

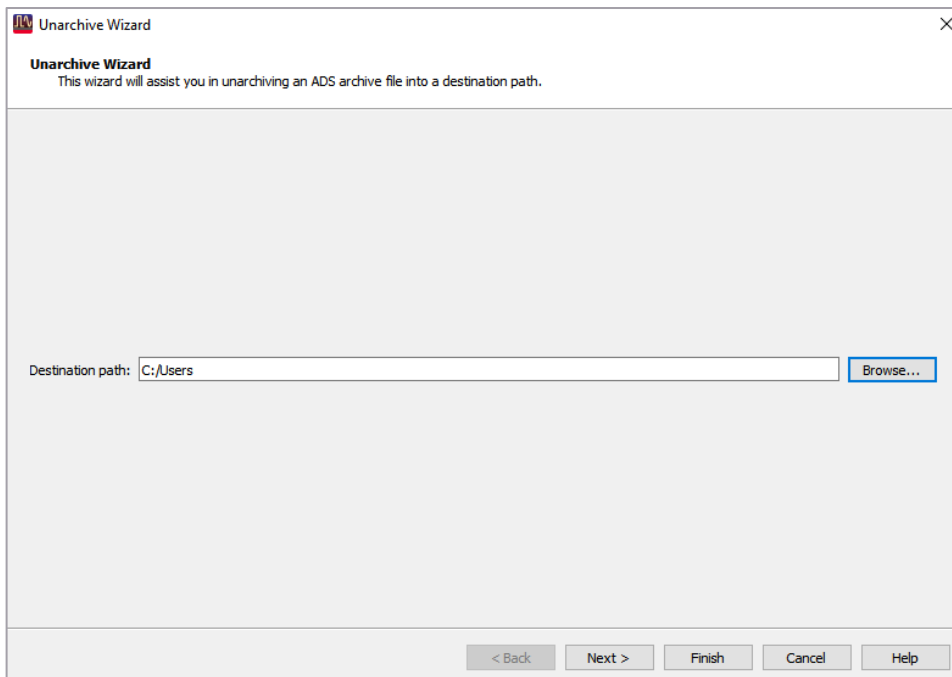
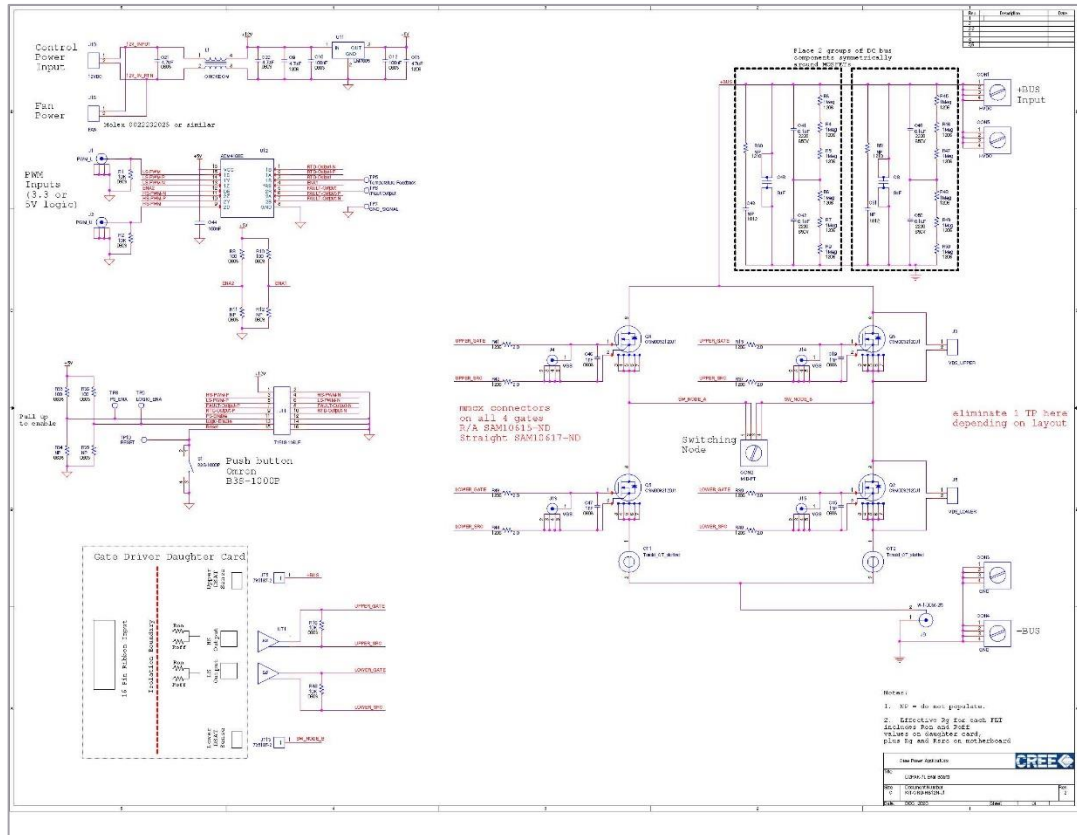


Figure 5. Unarchive wizard

5. Browse to select the destination folder.
6. Click **Finish**.

The Wolfspeed Half-Bridge

The Wolfspeed Model CRD-HB12N-J1 is a half bridge with two transistors in parallel for each side (four transistors total). The half bridge must be embedded into an outer circuit to operate. The analog portions are implemented in ADS. The gate drivers are replaced with ideal drivers. Additional circuitry must be provided to operate the half bridge. Two types of circuits are implemented. First a simple Boost converter which requires a DC source, Inductor, Capacitor, and Load. Second is a Clamped Inductive Switching Network which requires a DC source and an Inductor. This circuit is used to measure switching loss of the transistors and power balance between them,



Understanding the ADS Workspace

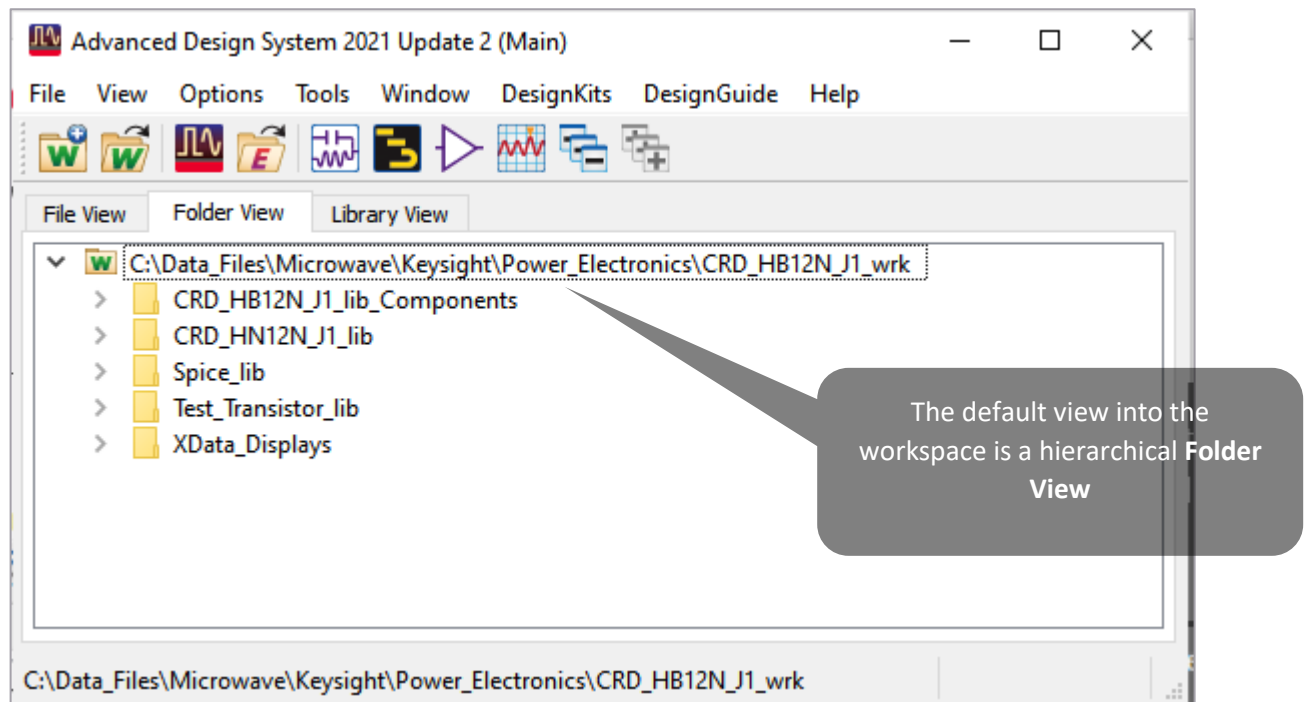


Figure 7. ADS Main Window

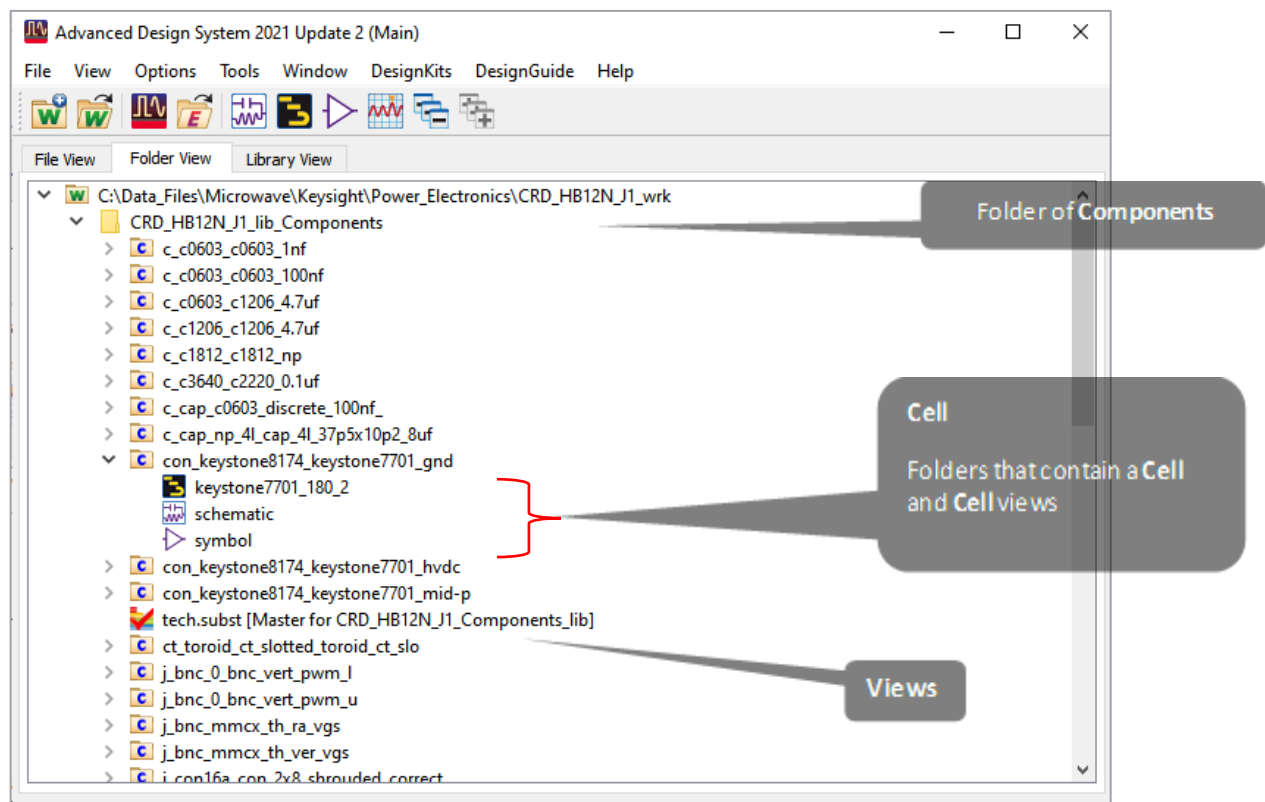


Figure 8. Folder of Components

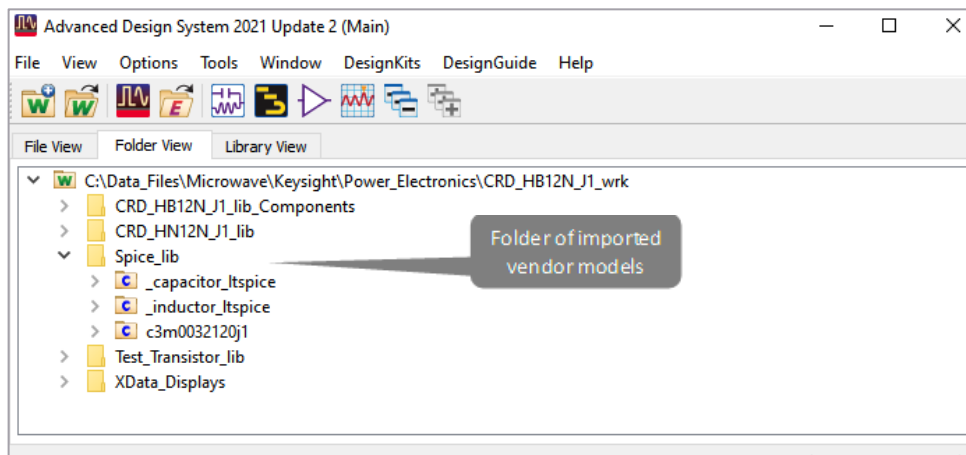


Figure 9. Folder of Imported Vendor Models

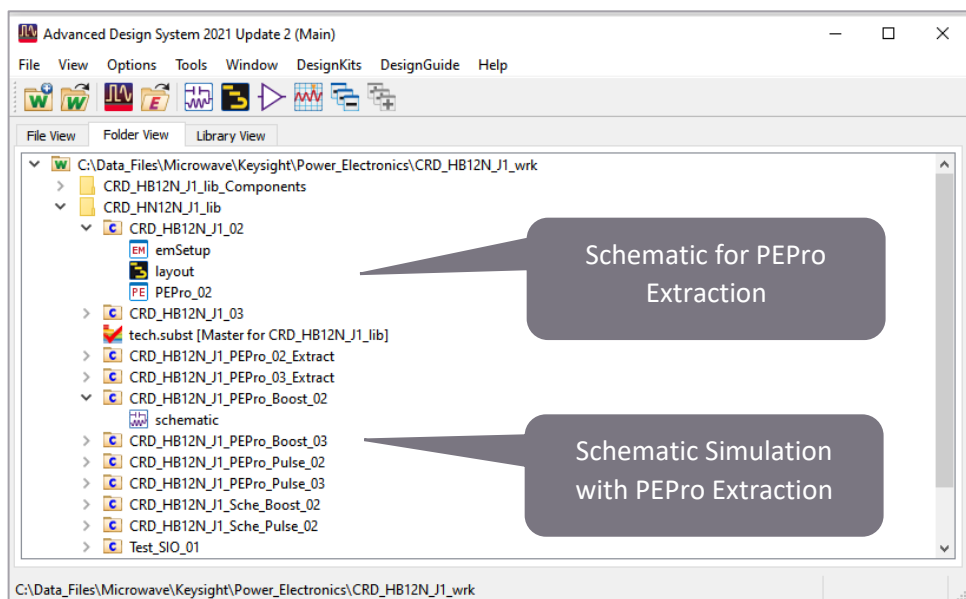


Figure 10. Folder of PEPro Extraction and Simulation

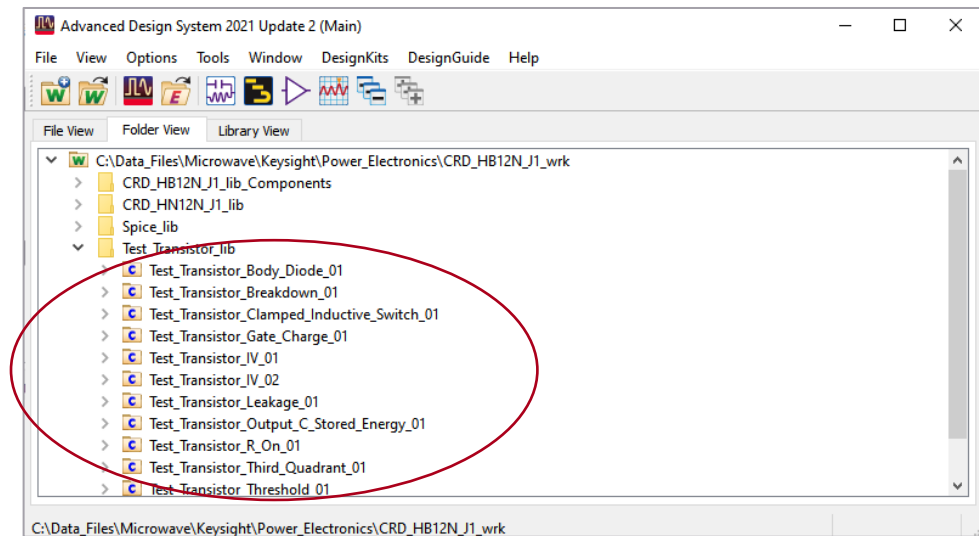


Figure 11. Folder of Simulations to Compare Transistor Model to Vendor Data Sheet

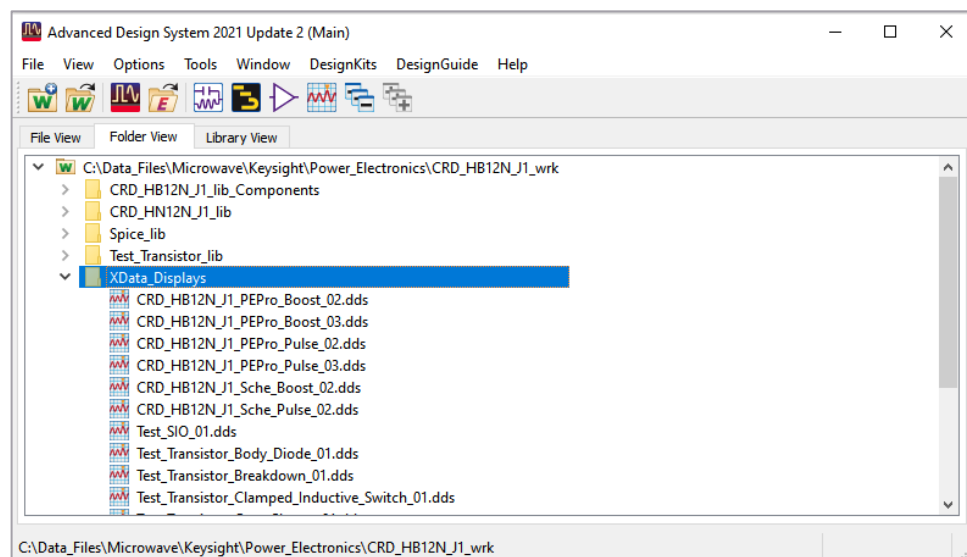


Figure 12. Folder of Data Displays

Running the Circuit Simulations “as-is”

The workspace contains circuit simulations with and without parasitics. The ones with parasitics have the letters “PEPro” in the cell name. The ones without parasitics have the letters “Sche” in the cell name. There are also two types of circuit topologies. The cells with “Boost” run use the half-bridge to run a DC-DC Boost converter. The cells with “Pulse” run a clamped inductive switching topology. They all use the vendor provided model for the transistors.

The circuit portion of the Boost converter can be modified by the user as well as the switching rate. As Boost L and C are increased the Stop Time will need to be increased to reach steady state. The simulations valid for both CCM and DCM. However, the formulas for the theoretical resistive losses are only valid in CCM.

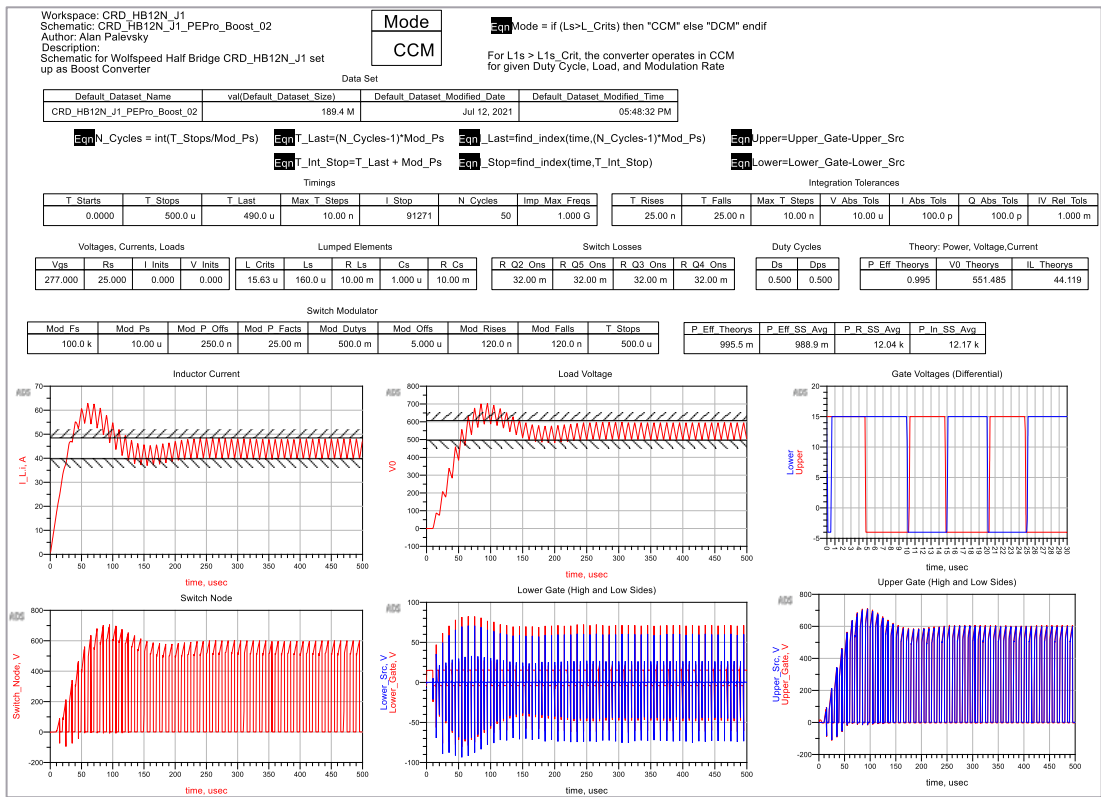


Figure 14. Summary Tab for Data Display: CRD_HB12N_J1_PEPPro_Boost_02

The Summary Tab lists all the inputs that control the simulation plus plots of the transient responses. The limit lines on the inductor current and load voltage are theoretical values derived from the circuit values and resistive losses in the transistors.

Workspace: CRD_HB12N_J1 Schematic: CRD_HB12N_J1_PePro_Boost_02 Author: Alan Palevsky Description: Schematic for Wolfsped Half Bridge CRD_HB12N_J1 set up as Boost Converter				Mode
				CCM
Data Set				
Default_Dataset_Name	val(Default_Dataset_Size)	Default_Dataset_Modified_Date	Default_Dataset_Modified_Time	
CRD_HB12N_J1_PePro_Boost_02	189.4 M	Jul 12, 2021	05:48:32 PM	
Voltages, Currents, Loads		Lumped Elements		Switch Losses
Vgs	Rs	I Inits	V Inits	
277.000	25.000	0.000	0.000	
L_Crits	Ls	R_Ls	Cs	R_Cs
15.63 u	160.0 u	10.00 m	1.000 u	10.00 m
R_Q2_Ons	R_Q5_Ons	R_QU_Ons	R_Q3_Ons	R_Q4_Ons
32.00 m	32.00 m	16.00 m	32.00 m	32.00 m
R_QL_Ons				
16.00 m				
Duty Cycles				
Dps	Ds			
0.500	0.500			
Voltages, Currents, Loads		Switch Modulator		ZO_Theory
Vgs	Rs	I Inits	V Inits	
277.000	25.000	0.000	0.000	
Mod_Fs	Mod_Ps	Mod_Dutys	Mod_Offs	Mod_Rises
100.0 k	10.00 u	500.0 m	5.000 u	120.0 n
Mod_Falls	T_Stops	Mod_P_Offs	Mod_P_Facts	
120.0 n	500.0 u	250.0 n	25.00 m	
				0.104
Theory				
P_In_Theory	I_L_Theory	P_RL_Theory	P_RQ_L_Theory/2	P_RQ_L_Theory/2
12220.915	44.119	19.465	7.786	7.786
P_RQ_U_Theory/2	P_RC_Theory	P_R_Theory	I_R_Theory	V0_Theory
7.786	4.864	12165.442	22.059	551.485
ZI_Dyn_Theory				
6.278				
Simulation				
P_In_SS_Avg	I_L_SS_Avg	P_RL_SS_Avg	P_Q2_SS_Avg	P_Q5_SS_Avg
12174.779	43.952	19.380	41.233	41.851
P_Q3_SS_Avg	P_Q4_SS_Avg	P_RC_SS_Avg	P_R_SS_Avg	I_R_SS_RMS
11.253	11.330	4.028	12039.964	21.945
V0_SS_RMS	ZI_SS_Avg			
548.634	6.302			
I_L_Rip_Theory	V0_Rip_Theory	P_Eff_Theory	P_Loss_Theory	
8.656	110.738	0.995	55.472	
I_L_Rip_SS	V0_Rip_SS	P_Eff_SS_Avg	P_Loss_SS_Avg	
8.608	99.588	0.989	129.074	

Figure 15. Steady State Tab for Data Display: CRD_HB12N_J1_PePro_Boost_02

The Steady Tab lists all the steady state values taken for the last switching period. The theoretical values are listed above the ones obtained from simulation. The theory does not take into account switching losses. As expected, the losses in simulation for the transistors is higher than that of theory. However, the overall efficiency is still high, 99.5% theory and 98.9% simulation.

- Double-click the schematic for CRD_HB12N_J1_PePro_Pulse_02.
- Click on the simulate icon  to run the simulation.
- The simulation takes about 1 minutes on a 3 GHz CPU
- The data display will automatically open: There are two tabs
 - Summary: Show Below
 - Formulas: Not Shown

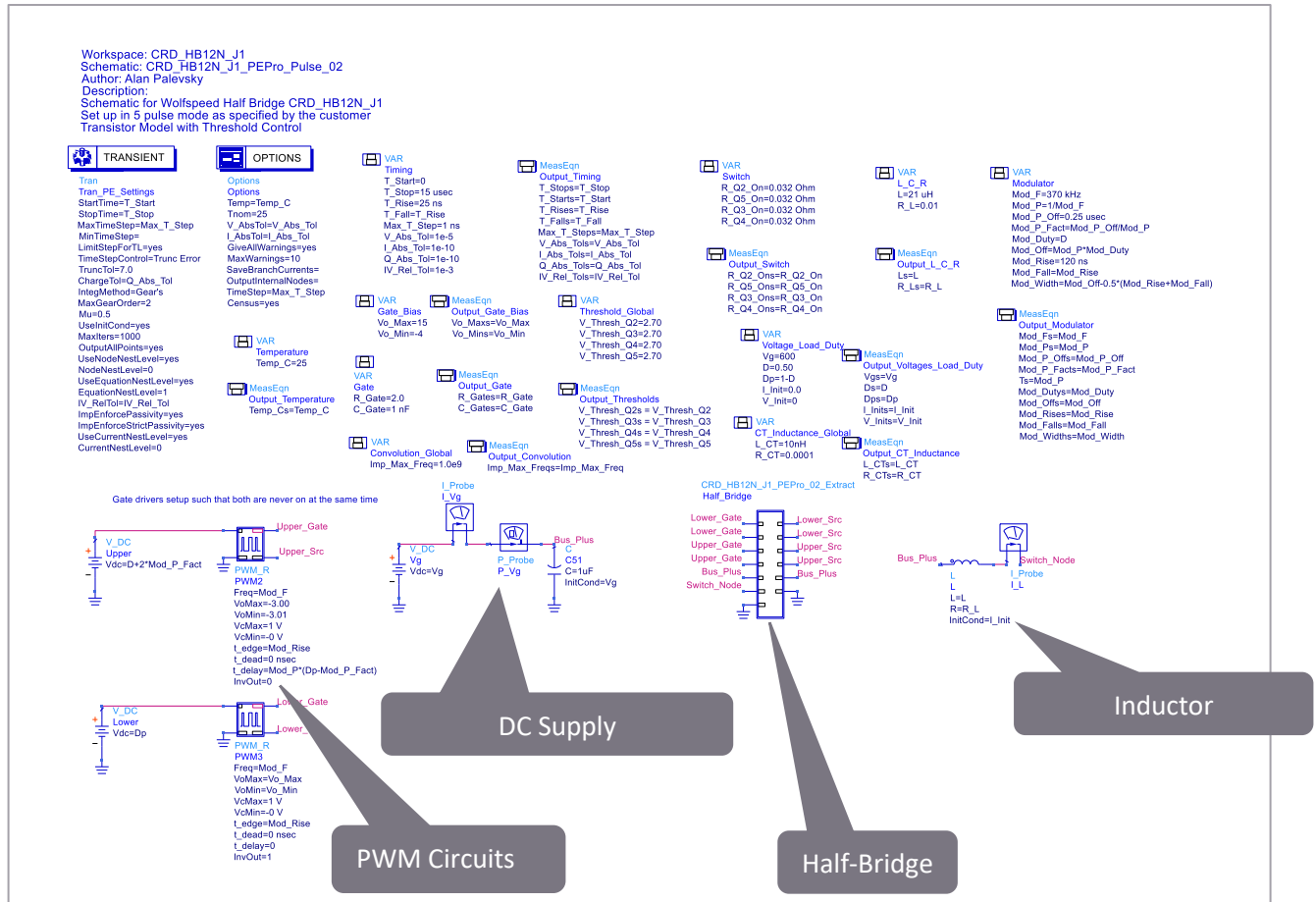


Figure 16. Schematic of CRD_HB12N_J1_PePro_Pulse_02

The Inductor value of 21 nH and the Modulation rate of 370 kHz was set to give pulses in 20-amp steps.

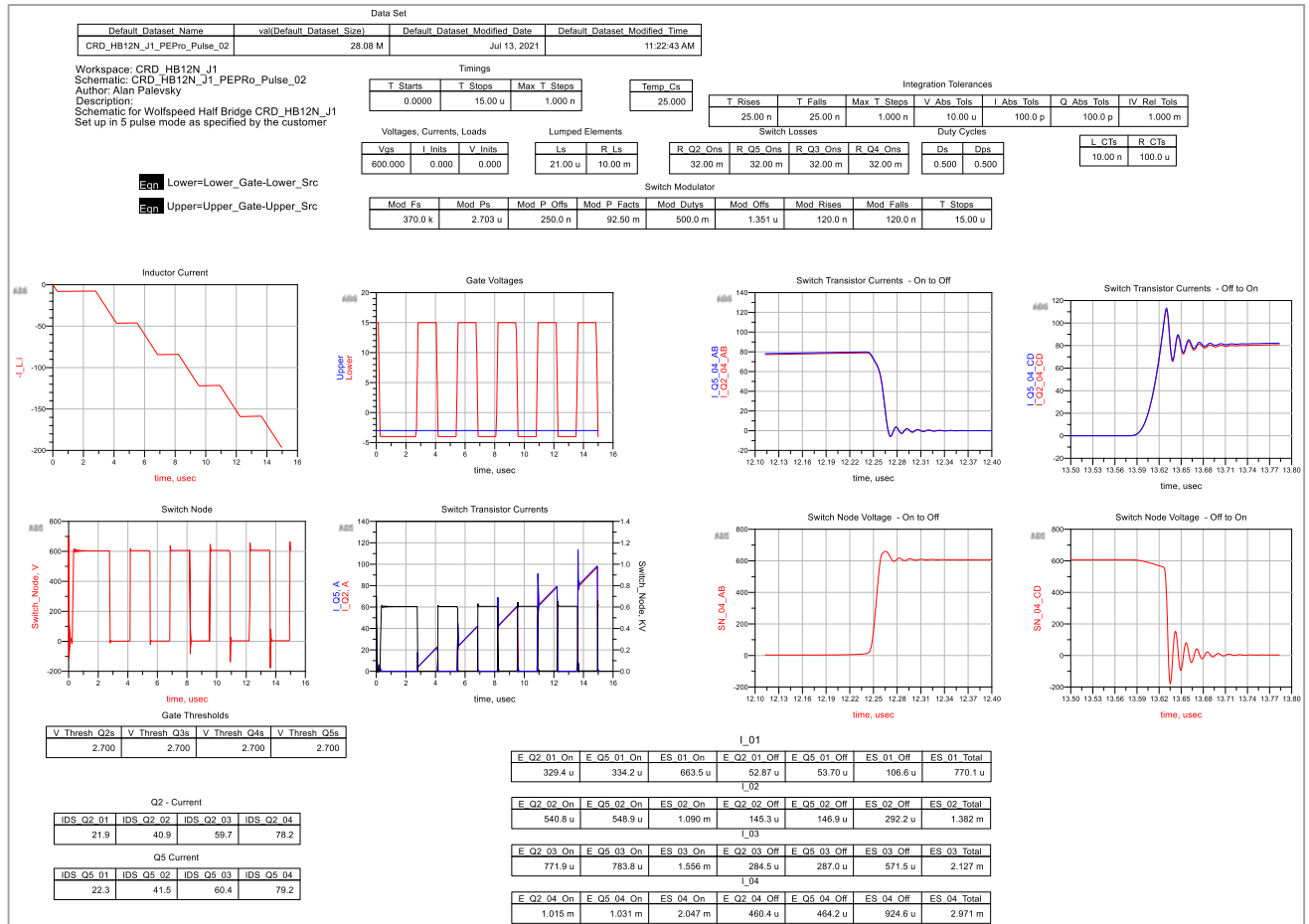


Figure 17. Summary Tab for Data Display: CRD_HB12N_J1_PEPPro_Pulse_02

The four plots on the left show the time evolution on a long-time scale of the voltages and currents. The four plots on the right show the expanded view of the voltages and currents about the fourth pulse transition. These values are integrated to calculate the power losses. The results are summarized in the Tables. Notice the two transistors (red and blue) in the plots have almost identical performance.

11. Double-click the schematic for CRD_HB12N_J1_PEPPro_Pulse_03.

12. Click on the simulate icon  to run the simulation.

13. The simulation takes about 1 minutes on a 3 GHz CPU

14. The data display will automatically open: There are two tabs

- Summary: Show Below
- Formulas: Not Shown



Figure 18. Summary Tab for Data Display: CRD_HB12N_J1_PEPPro_Pulse_03

This second extraction was performed with an asymmetric connection between the two lower transistors at the switching node. This results in an unbalance in current carried between the two transistors in parallel. This can be seen in the plots above

Viewing the details of the PEPro set-up

At the main ADS window

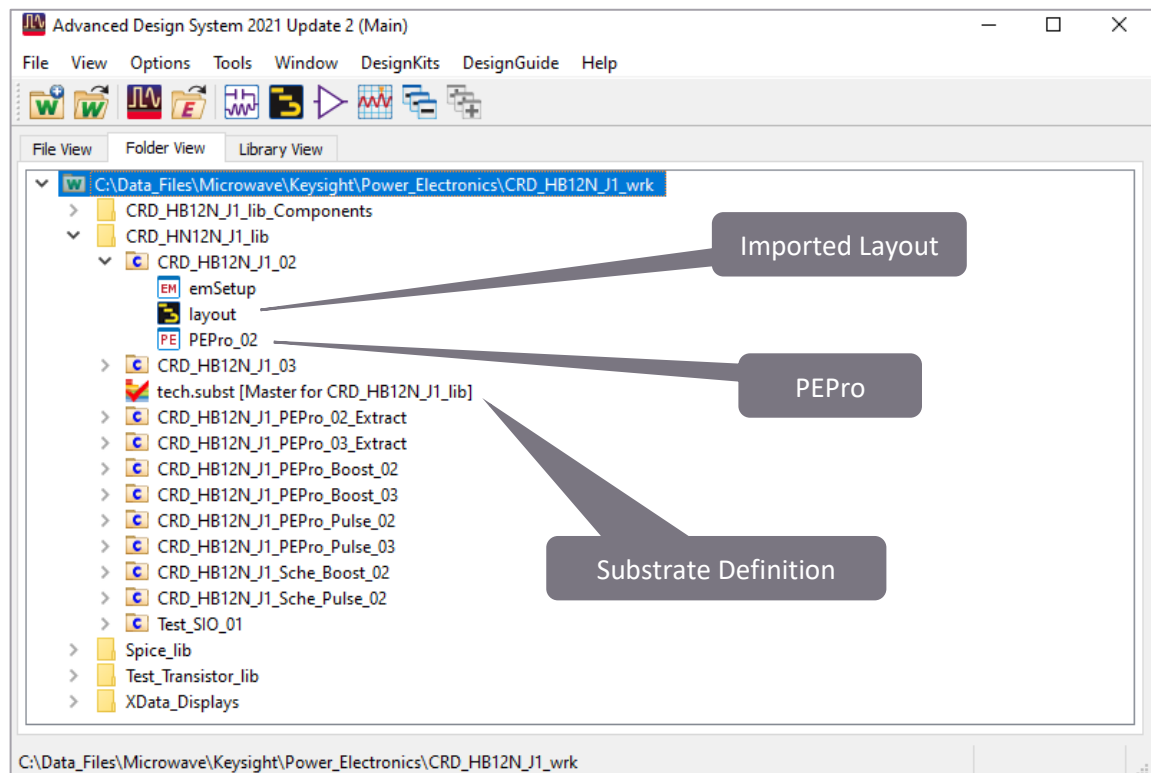


Figure 19. Main ADS window

The PEPro window is the layout after import into PEPro with the ports highlighted in red

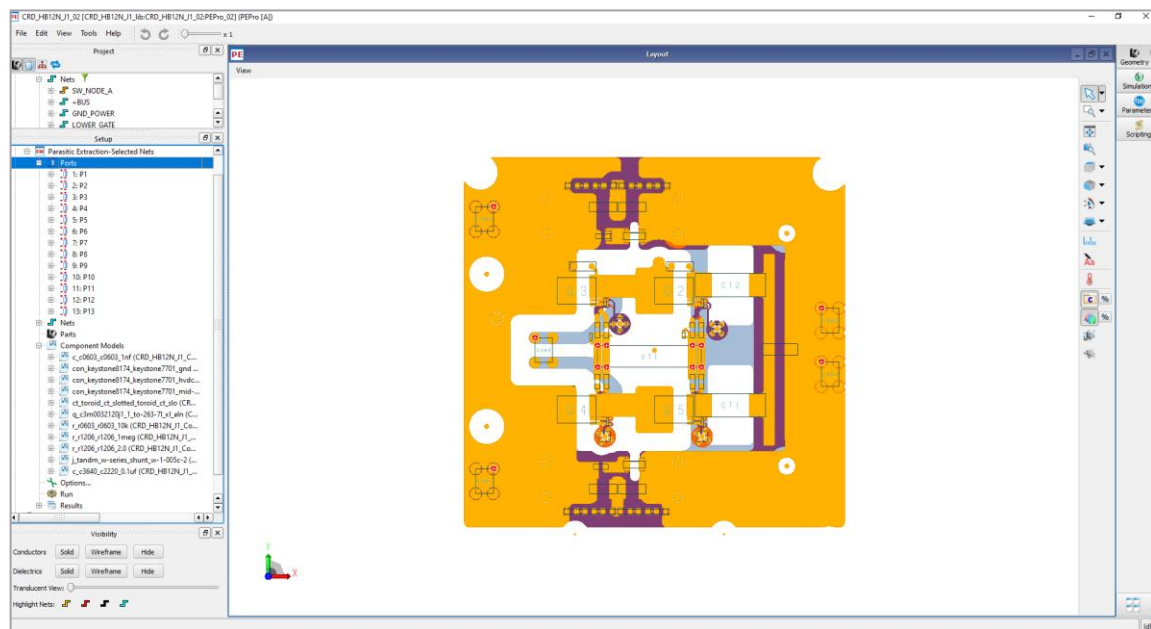


Figure 20. PEPro window

Import of Allegro BRD File

Create a new ADS workspace and then import the .brd file using the import menu from the main menu

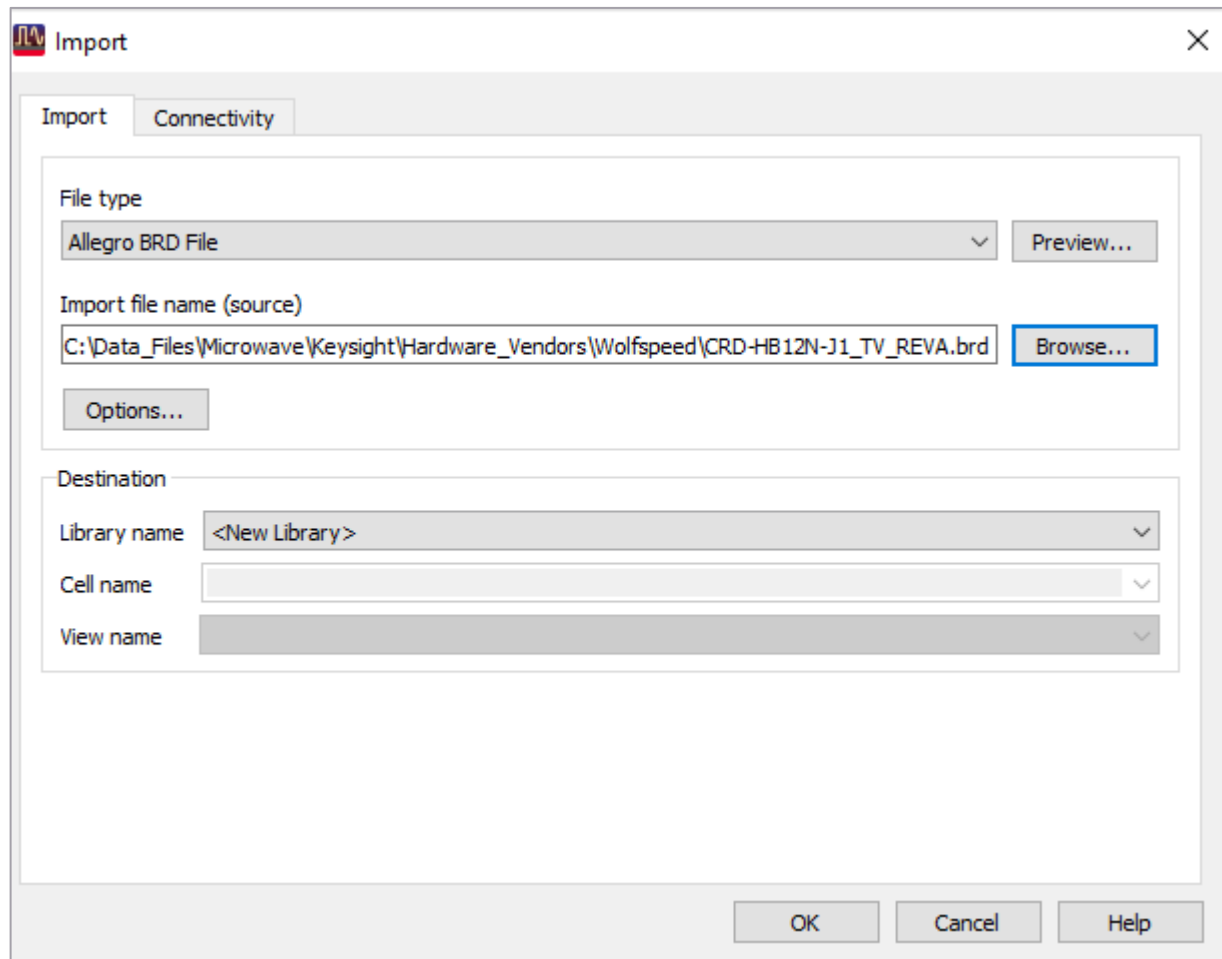


Figure 21. Import of Allegro BRD File

Note: See the ADS documentation for Allegro BRD import. Additional third-party software needs to be installed for the import to work

After the import is complete, the substrate needs to be modified. The bottom “Cover” ground plane needs to be added to provide the reference ground for the parasitic extraction. Also, the loss tangent for FR-4 needs to be changed from 0.04 to 0.02.

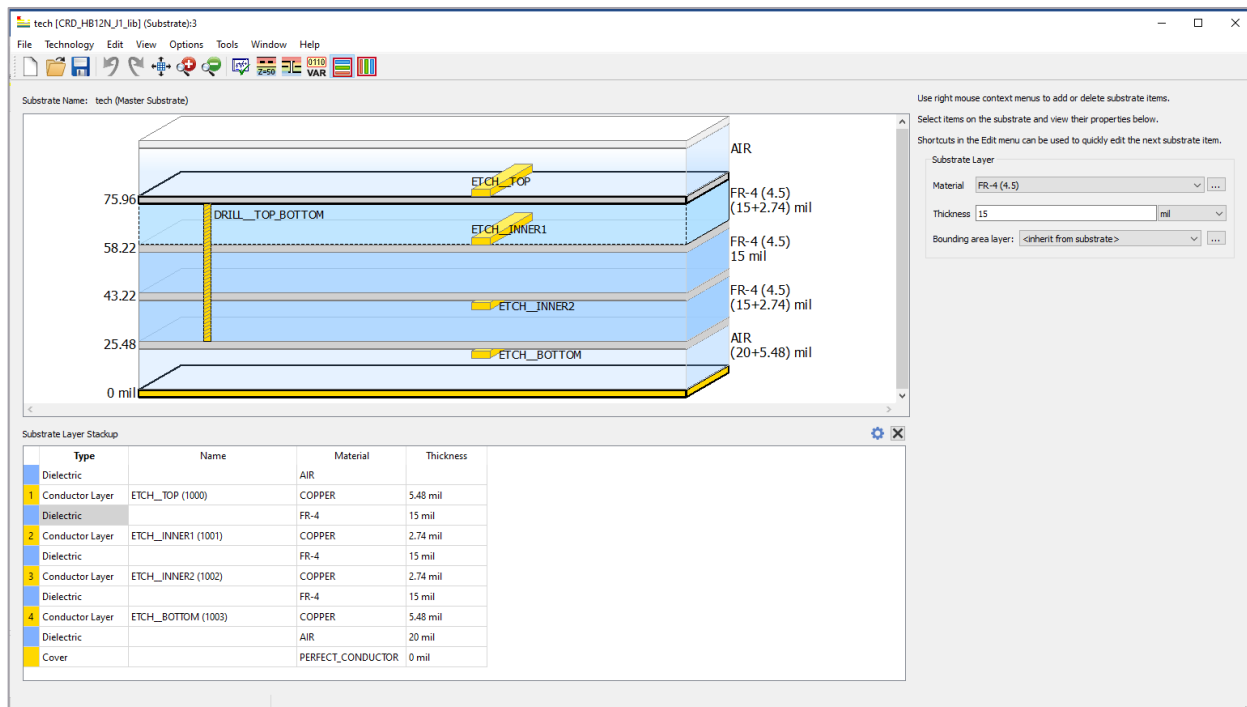


Figure 22. PCB layer viewer

The major issue with the import is that the component values are not “connected”. That is, when using PEPro and moving a component in the Design panel to the Component Values in the Analysis panel there is no model information. In ADS layout, for each imported component, there is a layout, a circuit and a symbol. However, the circuit is just a set of ports all open and the symbol is a generic box that does not correspond to the type of component (e.g., resistor, capacitor, ...). All the components must be updated for the component value. Values that need to be passed from the top schematic can be set using “global” parameters.

Click on the schematic icon of the component model to be updated and then add the component value between the port pins. An example of a 100nf capacitor is shown below. This process must be used for all the components that are to be selected for the PEPro analysis. For this Wolfsped example 11 components are used.

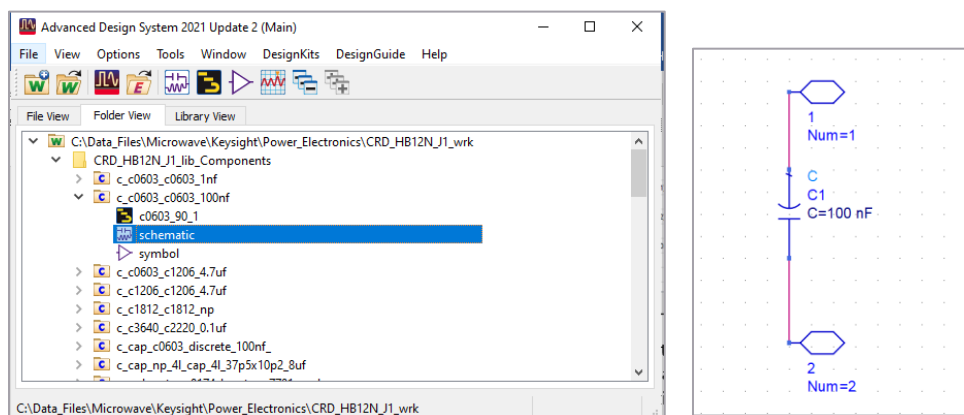


Figure 23. a) ADS main window, b) Schematic view of capacitor

Import of SPICE Transistor Model

The SPICE model for the MOSFETs must be imported separately. It is another component and is not part of the brd import. The transistor used in the half-bridge is a C3M0032120J1 Silicon Carbide Power MOSFET. The SPICE model is available for the website.

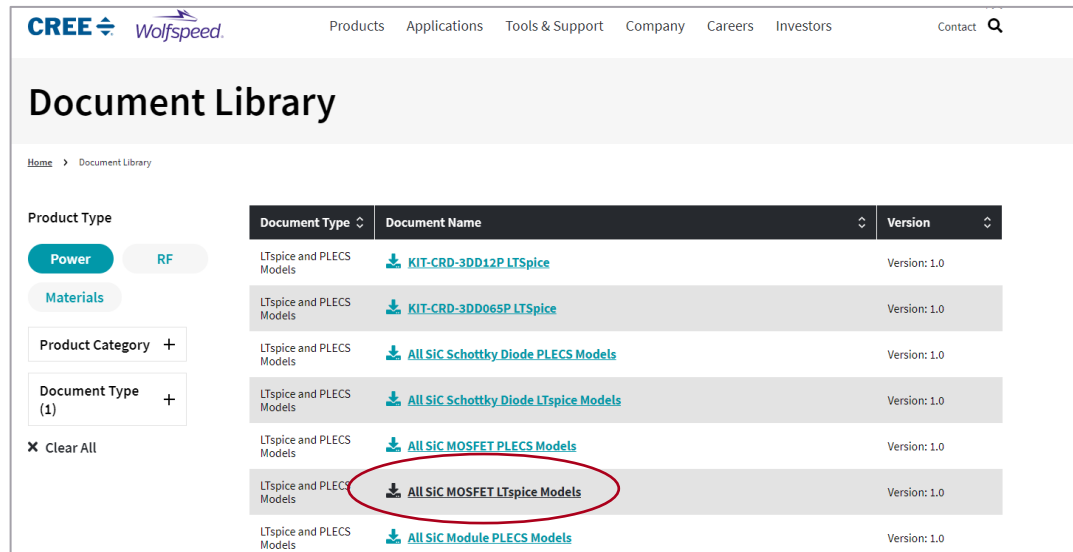


Figure 24. Import model

The import window with options is shown below. Notice that the SPICE “dialect” is set to LTSpice and the import is a Netlist, not a schematic.

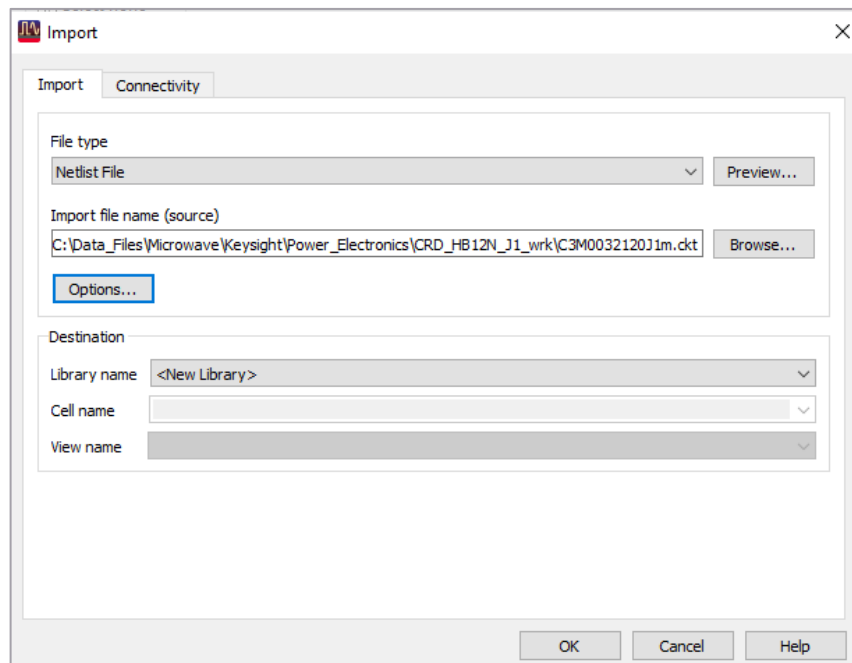


Figure 25. import options window

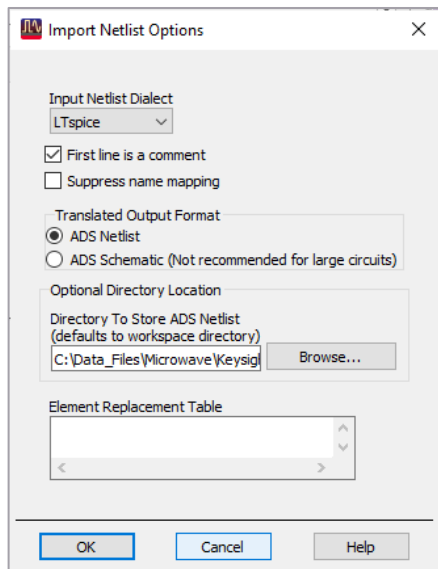


Figure 26. Import netlist options

The connections to the imported SPICE model are shown below. The names were added to the box to indicate usage.

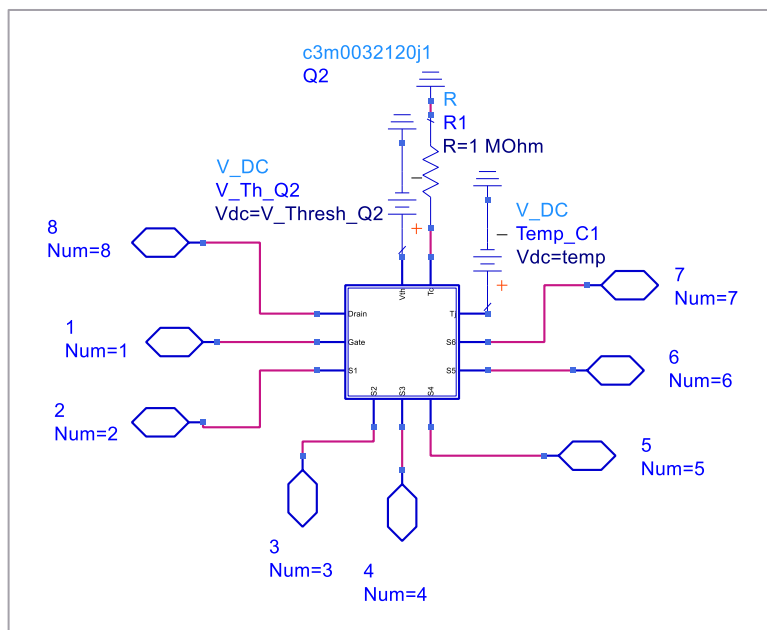


Figure 27. SPICE model with connections

1	2	3-7	8	Tj	Tc	Vth
Gate	Source - Kelvin	Source	Drain	Temperature	Thermal T.C	Gate Threshold

Ports 1 through 8 are circuit connections. Tj is the junction temperature set through a DC voltage source set to the ADS global temperature parameter “temp”. It is set in the ADS controller options block. The Tc

resistive connection sets the transient thermal time constant. Setting the value to 1 MΩ eliminates any thermal transient effects. The Vth connection uses a voltage to set the gate threshold. This allows for different gate values for the four transistors in the design. The value is set in a “global” VAR block in the top schematic.

Specifying Input/Output Pins

Finally, the Input/Output pins need to be inserted. These are the location in the layout that connect to the top-level schematic. Click on the Select-Pin Icon  in the layout menu and place the pin at the desired location. The location of Pins one and two are shown below. Pins are shown by the pink arrows

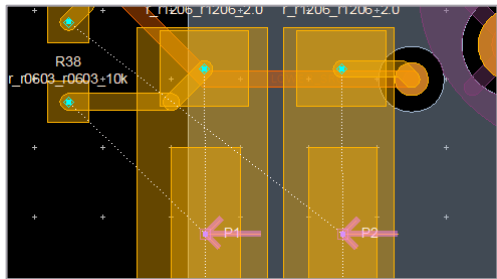


Figure 28. Input/Output pins configuration window

Thirteen Pins are required for the extraction. Their circuit locations are listed below.

P1	P2	P3	P4	P5	P6	P7	P8	P9, P10	P11	P12-13
Q2: Gate	Q2: Src	Q5: Gate	Q5: Src	Q3: Gate	Q3: Src	Q4: Gate	Q4: Src	Bus +	Switch Node	Ground

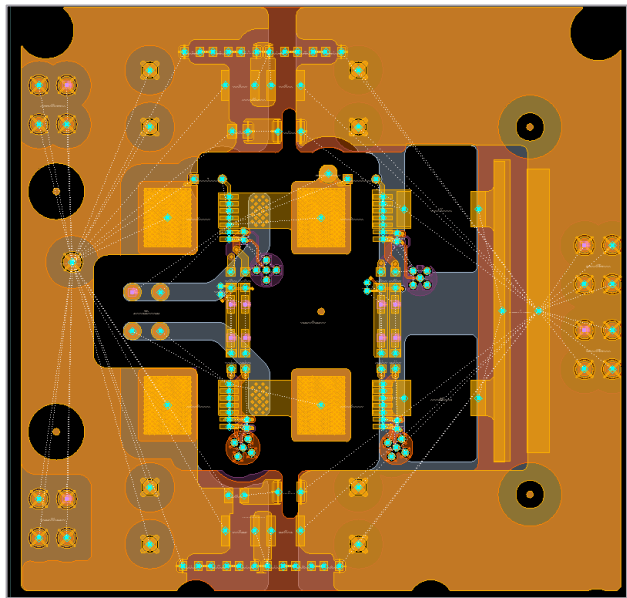


Figure 29. The thirteen port locations with the pink arrows are shown in the layout

Once all the above-mentioned steps are completed, PEPro can be invoked

PEPro Setup

In the layout window click **Tools > PEPro > Open**

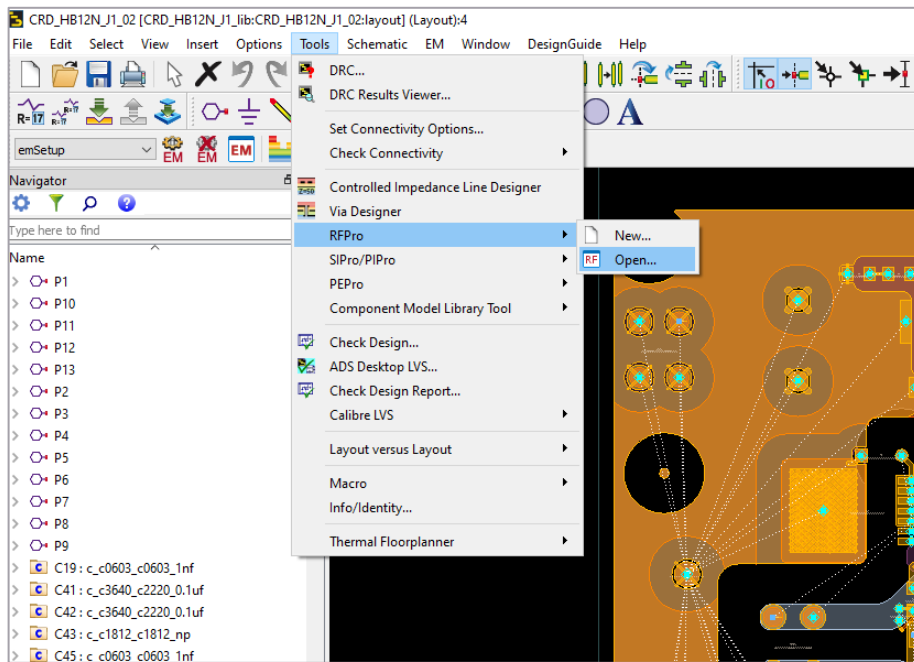


Figure 30. RFPro tools

In the PEPro Main window, view the Project and Setup dockable sub-windows content. The Project sub-window contains all elements included in the layout that is nets, components, pins, and so on. The Setup sub-window is used for EM analysis of either entire design (Parasitic Extraction-All Nets) or only selected nets (Parasitic Extraction-Selected Nets).

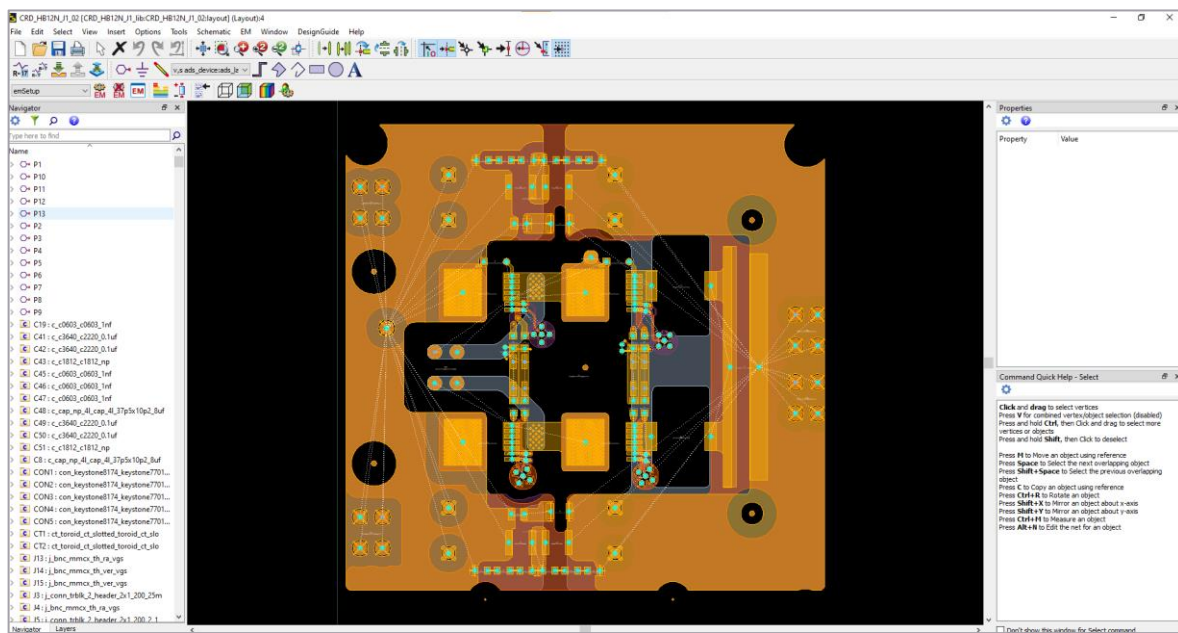


Figure 31. PEPro window

Component Models and Pins

In the example, Ports, Component Models, Pins, Options have already been configured. You can double-click the **Run** button to run an EM Model Extraction. To understand the setup, read the details in the subsequent sections.

Select the 11 used components under **Project > Components**. Drag them to the **Setup** sub-window and drop onto **Parameter Extraction-Selected Nets> Component Models**. Select all the pins under **Project > Pins** and drop them onto **Parameter Extraction-Selected Nets> Pins**.

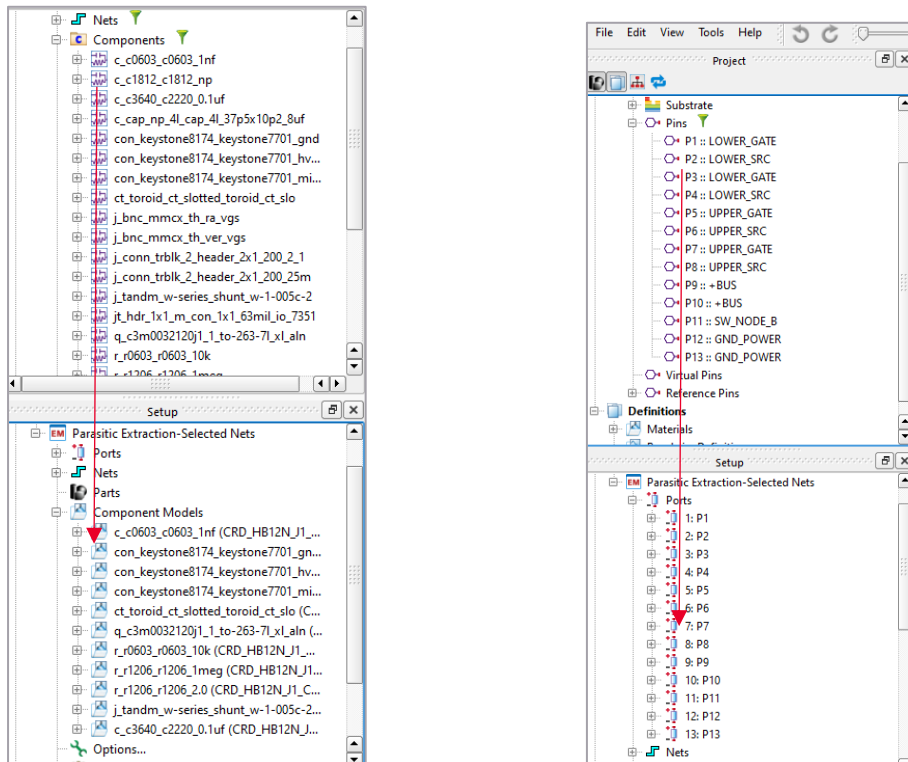


Figure 32. a) PEPPro configuration sub-window, b) PEPPro configuration sub-window

Options Setup

Frequency Plans

There are several types of frequency sweeps. For switched mode power converters, we use an automatic frequency plan for switched-mode power supplies (**SMPS**) in Power Electronics. It creates a composite frequency plan that can capture the most important EM features of a PCB in SMPS circuits. To use this plan, the user needs to provide circuit characteristics in the frequency plan table. Once the required input data is set, the frequency plan will be generated automatically and used in the subsequent EM simulation. For debugging, a simpler frequency plan can be chosen.

For this project a switching frequency of 100 kHz and a rise and fall time of 5 nsec was chosen. The 5 nsec is needed to resolve the voltage and current ringing during the switch transition. These settings result in maximum characterization frequency of 1 GHz

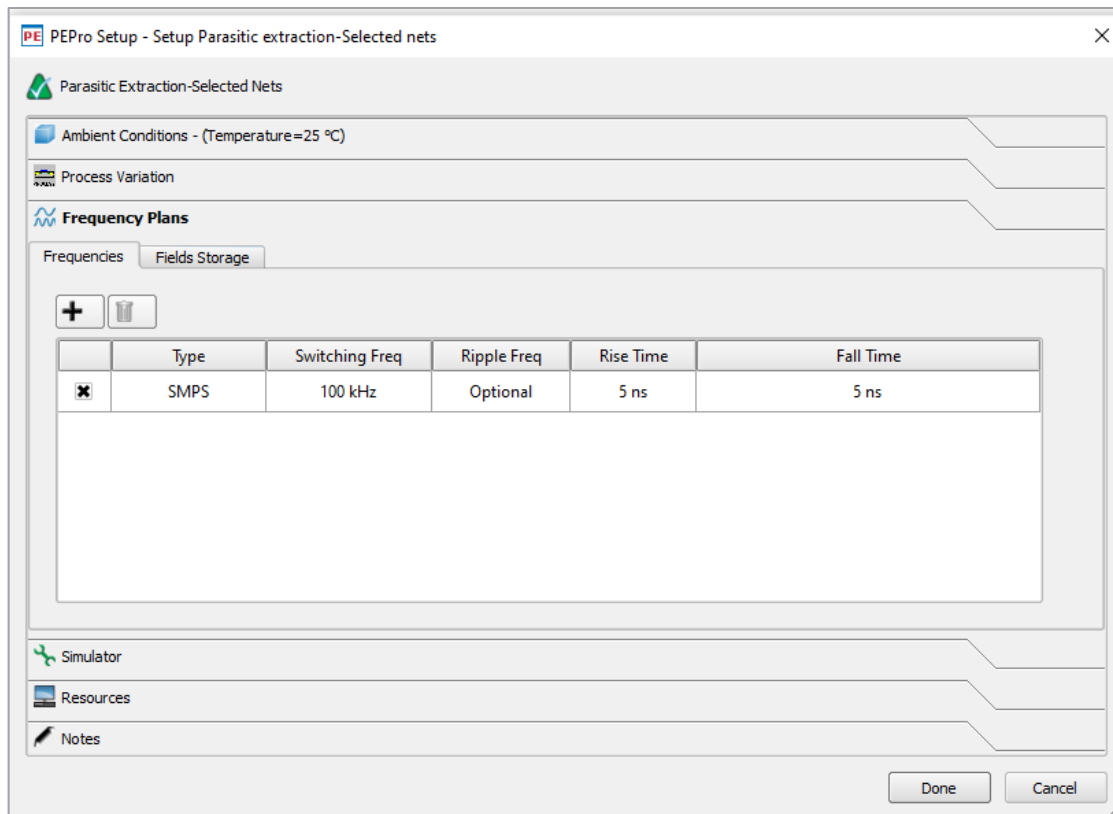


Figure 33. Set up parasitic extraction

Simulator

Momentum RF provides the fastest EM simulation speed with good accuracy. Momentum RF is a fast, quasi-static 3D planar solver that is appropriate for SMPS PCBs and packages. The slower Momentum Microwave setting is intended for a different purpose, namely multi-gigahertz microwave circuits where the highest wavelength, that is, speed of light divided by highest frequency is physically much smaller than the size of the board. FEM is intended for objects with arbitrary 3D geometries such as connectors or boards with very high layer count.

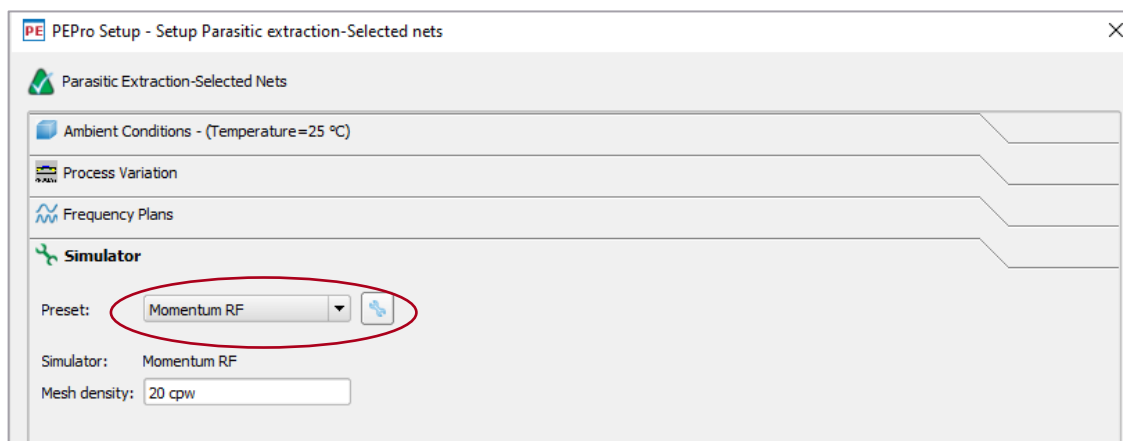


Figure 34. EM simulation preset

Advanced Simulator Settings

Change Matrix solver to “**Direct-Dense**”, the Thick conductor model to “**3D**”, the Via conductor model to “**Lumped**” and the Healing snap distance to “**Off**”.

Many SMPS board designs use large arrays of vias as thermal paths between layers. Meshing them as 2D or 3D objects increases the mesh size dramatically with no major effect of circuit performance.

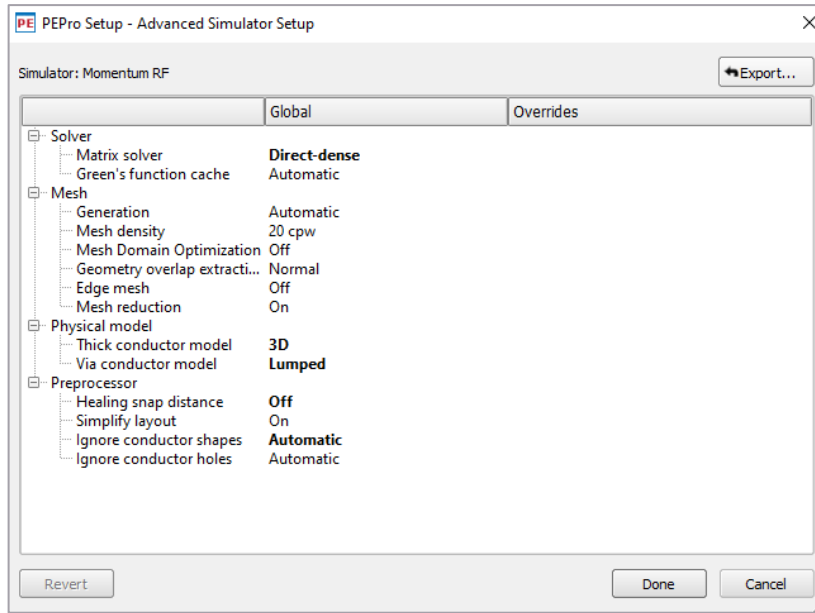


Figure 35. PEPro advanced simulation setup

Resources

You can run EM simulations on a local or remote host machine and benefit from faster simulation times.

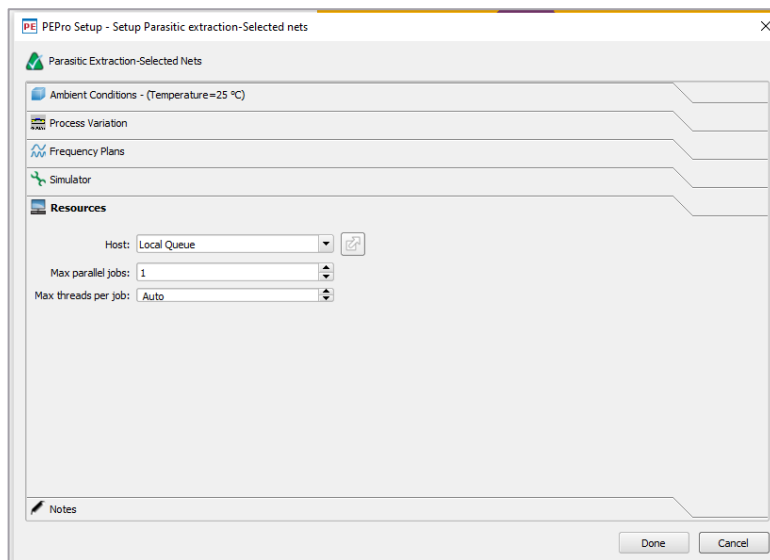


Figure 36. Simulation resources setup

Running a PEPro Simulation

Double-click **Run** to start the EM simulation. The simulation takes several minutes depending on available computation resources. When the simulation completes, close the **Simulations** window.

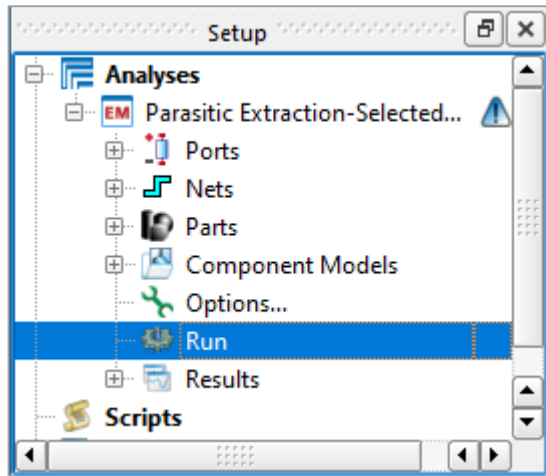


Figure 37. Simulation run button

Results

Generate Sub Circuit

Once the simulation is complete, double click **Generate Sub Circuit** to generate an EM model that can be used in the EM-circuit co-simulation. If the sub circuit already exists in the workspace, it may overwrite with the new EM simulation data. The example already contains a sub-circuit named **schematic_Parasitic_Extraction-Selected_Nets** and it will be overwritten(updated).

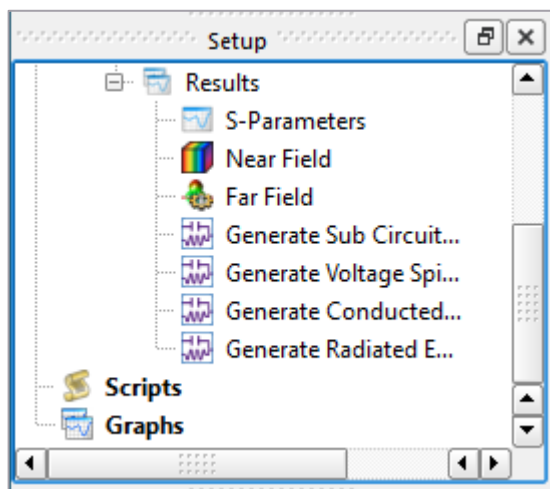


Figure 38. Simulation results run button

Theoretical Efficiency – Resistive Loss Only – CCM operation

Definition of Terms

$$\begin{aligned}
 R_L &= \text{Inductor Series Resistance} \\
 R_C &= \text{Capacitor Series Resistance} \\
 R_{QS} &= \text{Switch Transistors Parallel On Resistance} \\
 R_{QC} &= \text{Commutator Transistors Parallel On Resistance} \\
 R &= \text{Load Resistance} \\
 T &= \text{PWM Period} \\
 D &= \text{Duty Cycle} \\
 D' &= 1 - \text{Duty Cycle} \\
 V_g &= \text{DC Input Voltage}
 \end{aligned} \tag{A:1}$$

Efficiency due to Resistive Losses

$$\eta_R = \left[\frac{1}{1 + \frac{D'(RR_C + RR_{QC} + R_C R_{QC}) + (DR_{QS} + R_L)(R + R_C)}{D'^2 R^2}} \right] \left(\frac{R + R_C}{R} \right) \tag{A:2}$$

Output Voltage and Inductor Current

$$V_0 = \frac{1}{D'} V_g \eta_R \quad I_L = I_g = \frac{1}{D'^2 R} V_g \eta_R \tag{A:3}$$

Input and Output Power

$$P_{in} = \frac{V_g^2}{D'^2 R} \eta_R \quad P_{out} = \frac{V_g^2}{D'^2 R} \eta_R^2 \tag{A:4}$$

Power Dissipated in Inductor and Capacitor

$$P_{R_L} = \frac{V_g^2}{D'^4 R^2} R_L \eta_R^2 = R_L \left(\frac{P_{out}}{V_g \eta_R} \right)^2 \quad P_{R_C} = \frac{V_g^2 D}{D'^3 R^2} R_C \left(\frac{R}{R + R_C} \right) \eta_R^2 = P_{out} \left(\frac{D}{D'} \right) \left(\frac{R_C}{R + R_C} \right) \tag{A:5}$$

Power Dissipated in Switch Transistors

$$P_{R_{QS}} = \frac{D V_g^2}{D'^4 R^2} R_{QS} \eta_R^2 = R_{QS} D \left(\frac{P_{out}}{V_g \eta_R} \right)^2 \tag{A:6}$$

Power Dissipated in Commutator Transistors

$$P_{R_{QC}} = \frac{V_g^2}{D'^3 R^2} R_{QC} \eta_R^2 = D' R_{QC} \left(\frac{P_{out}}{V_g \eta_R} \right)^2 \quad (\text{A:7})$$

Input and Output Impedance

$$Z_I = D'^2 R \frac{1}{\eta_R} = \frac{V_g^2 \eta_R}{P_{out}} \quad Z_O = \frac{1}{D'^2} (R_L + D R_{QS} + D' R_{QC}) \eta_R \quad (\text{A:8})$$

Inductor Ripple

$$\Delta I_L \approx \frac{V_g T D}{L} \left[1 + \frac{(R_L + D R_{QS} + D' D R_{QC})}{D'^2 R} \right]^{-1} \quad (\text{A:9})$$

Output Voltage Ripple

$$\Delta V_0 \approx \frac{V_g}{R D'} \eta_R \left[\left(\frac{D T}{C} \right) + \left(\frac{R_C}{D'} \right) \right] = \frac{P_{in}}{V_g} \left[\left(\frac{T D D'}{C} \right) + R_C \right] \quad (\text{A:10})$$

Note: The actual efficiency will be less due to switching losses.

Design Space Exploration and “What if...?” Analysis

In contrast to a sequence of expensive and time consuming “solder-and-see” physical prototypes, the virtual prototype is more cost-effective for exploring the design space and performing “What if...” analysis. For example, the reference design as-is may be close to what you need, but not an exact match. But if you modify it you run the risk of introducing unwanted side effects like excessive voltage spikes and EMI problems. The virtual prototype gives you insight on how to change it while minimizing side effects. Try replacing some of the components with lower cost, lower performance ones. An example would a capacitor with higher series inductance or resistance and hence a lower self-resonant frequency. Next try re-routing the PCB traces, especially those in the switched loop that has high di/dt trapezoidal waveforms. See how the ringing and EMI are affected.

Conclusion

Virtual prototypes like this one are complementary to physical prototypes. Physical prototypes are the gold standard for compliance and measured characteristics of course but they have several drawbacks:

- Expensive and time consuming to design, build, and measure
- Vulnerable to catastrophic failure – the infamous smoke test that produces actual smoke
- Hard to get a measurement probe onto interior nodes so you can’t really see what is going on inside

In contrast, virtual prototypes are easy to change and while they do indicate device overstress, they never emit real smoke. The voltage, current, and fields at every spatial point in the 3D grid and every time step in the simulation can be recorded and made accessible for plotting, even point that are physical inaccessible in the real world such as inside a semiconductor package.

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