



Bringing Beamforming and mmWave to 5G UEs

Smart Mount automates MMIC 3D stack integration in 5G millimeter-wave designs ready for EM / circuit co-simulation

Deliver the Full 5G User Experience

5G technology promises a smooth multimedia experience on devices for content like 4K video and multiplayer gaming, demanding an order of magnitude more bandwidth than 4G and imperceptible latency, even in moderate network traffic. A crucial design goal for meeting increased user expectations, 5G beamforming fitted for UE (user equipment), is challenging.

Ultra-wideband 5G introduces millimeter-wave (mmWave) frequencies with new signal propagation, noise, and interference behavior. An array of 5G UE like smartphones, smartwatches, and tablets must handle mmWave behavior in tightly packaged devices with battery-supplied power and passive cooling. Success depends on creating dense board and module structures, like those in Figure 1, subject to layout and packaging parasitics, multi-domain RF effects, and performance-crushing interactions.

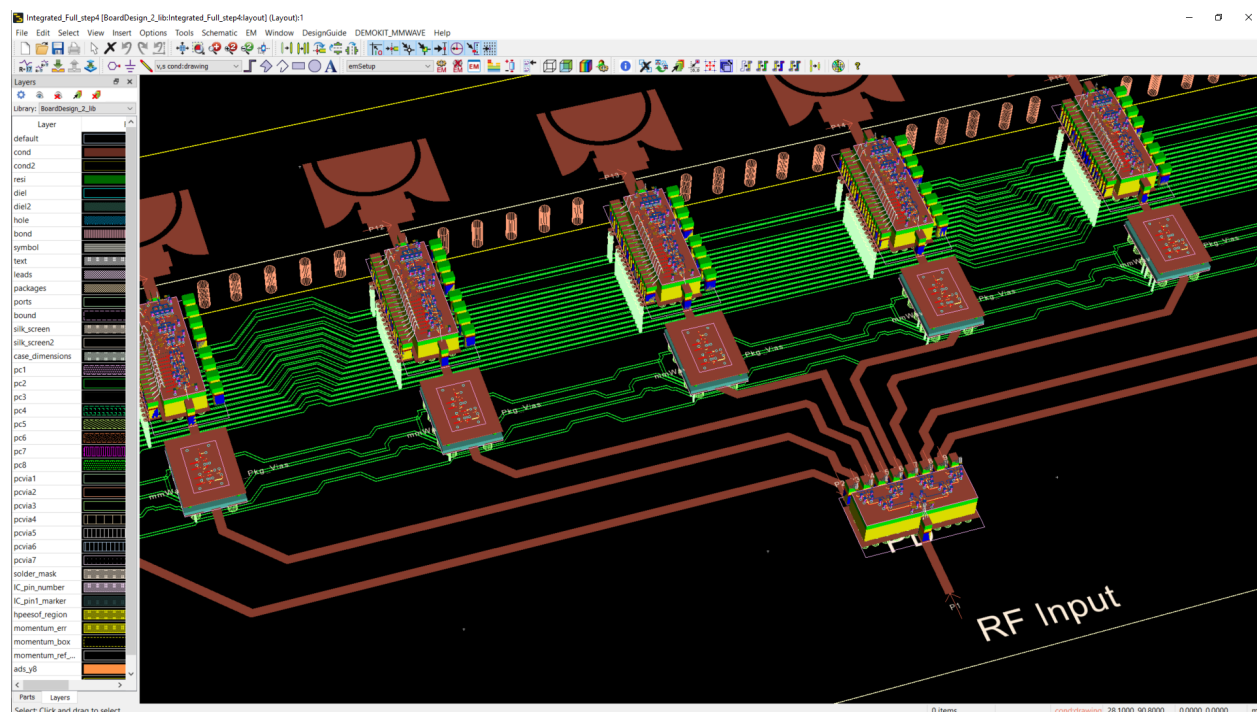


Figure 1. Transmit chain section of a mobile phone board reference design with integrated antennas

Dense mmWave designs require three core RF electronic design automation (EDA) capabilities working together for first-pass success. Cutting-edge RF designs need small structure layout tools with modeling details of board layers, components, and parasitics; drop-in multi-technology modules with associated behaviors flowing seamlessly into system designs; and electromagnetic (EM) / circuit co-simulation tools that yield accurate multi-domain results using modulated waveforms.

Keysight Advanced Design System (ADS) and RFPro with Smart Mount technology streamline the RF design workflow to meet the challenge. This environment enables the simulation of 5G mmWave behavior using authentic modulation, uncovering issues in the virtual space before moving to hardware prototypes. We will explore why 5G UE needs beamforming, how multi-technology helps achieve modularity in dense designs, and pivotal points in a beamforming design workflow using ADS.

Beamforming Increases UE Bandwidth

Traditional RF platforms, including earlier generations of mobile devices, transmit energy in a uniform circle pattern from a single antenna. However, this is a highly inefficient method as only a tiny slice of the total radiated energy from the transmitter gets to a receiver. Increasing the link margin by raising transmit power, which impacts UE battery life, is one way to overcome noise and interference.

Beamforming is a more reliable approach that shapes the energy of transmitted beams toward a receiver or target using multiple antennas. With beamforming, signal quality improves while reducing wasted power. Large-structure systems, like phased array radar, have used beamforming to increase range and detection resolution for years, but the concept is relatively new to small-structure systems.

Another approach to noise and interference is multiple-input multiple-output (MIMO), which uses spatial multiplexing on multiple antennas and channel knowledge gained via digital processing. In high-quality signaling environments, single-user MIMO (SU-MIMO) can transmit parallel data streams to one receiver, increasing adequate channel capacity.

5G NR (new radio) combines beamforming and MIMO, creating Massive MIMO. Each gNodeB (base station) uses a large antenna array, often starting at 64 x 64 elements and possibly up to 256 x 256, with subdivision capability for assigning smaller independent arrays. With an added beamforming array, a 5G mmWave UE can capture SU-MIMO for more device bandwidth. Eight-layer SU-MIMO optimizes gNodeB capacity and minimizes cross-UE interference. Shaping beams (Figure 2) improves channel metrics like signal-to-noise ratio (SNR) and error vector magnitude (EVM). Since the signal quality is good, engaging SU-MIMO can reduce the transmit power in each layer while maintaining reliable connections.

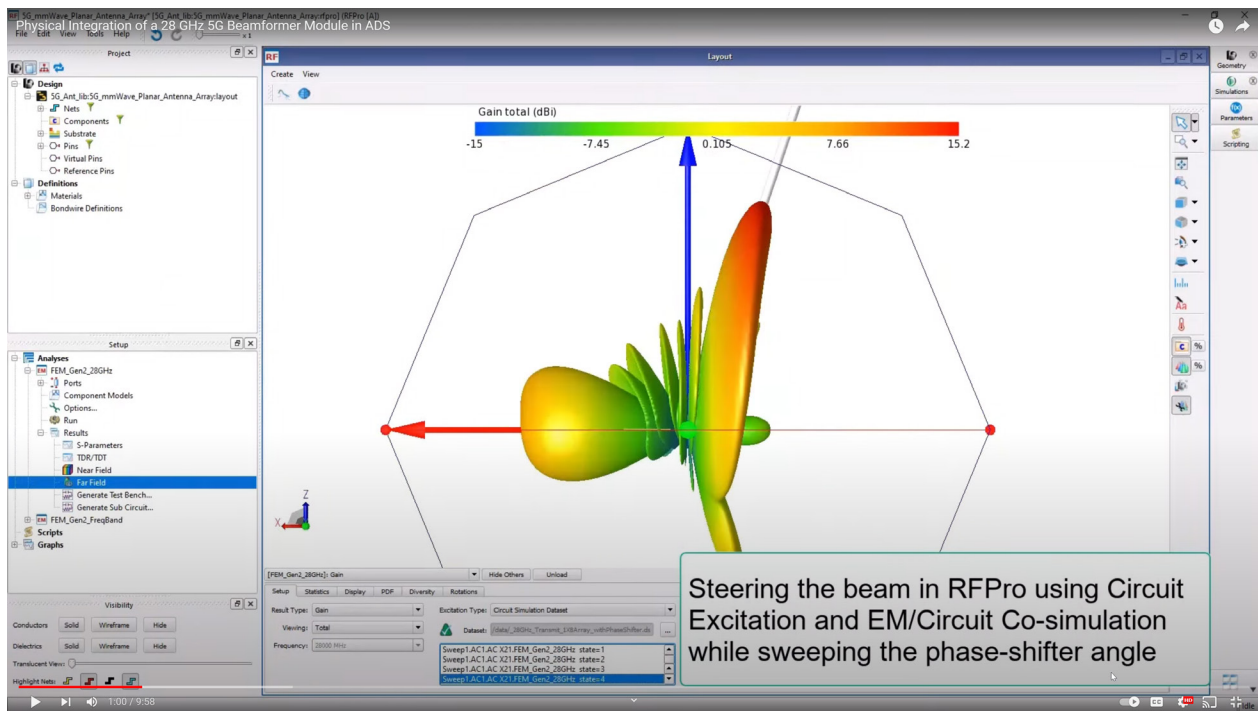


Figure 2. RFPPro far-field visualization of beamforming in an eight-cell patch-antenna SU-MIMO scenario for a 5G UE

Adding eight-layer SU-MIMO represents a compelling opportunity for UE designers, extending 5G mmWave UE battery life and delivering the throughput needed for 4K video and other experiences. Yet achieving it means packing eight antennas and 28 GHz RF signal processing for all antennas into an already-crowded space with denser, modular, higher-performance packaging techniques.

Multi-Technology Addresses Densification

UE dimensions have remained relatively constant with each generation, but payloads have increased dramatically. More processing power and storage, higher resolution displays, better cameras, and highly sophisticated RF chipsets supporting 5G, Wi-Fi, Bluetooth®, and earlier cellular networks are all expected to fit in one smartphone. If 5G UE were entirely digital, frequent semiconductor process shrinks would keep pace by putting more transistors to work in the same space. However, a 5G UE employs digital, analog, and RF electronics in a mixed-signal design, presenting a more complex challenge — densification.

Placing RF modules, antennas, passive components, and structures like board layers, planes, vias, and traces closer together introduces complicated interactions that intensify as frequency increases. Even simple structures like packaging leads and wire bonds highlighted in Figure 3 can start displaying complex EM behaviors. When introducing an RF module into a 5G mmWave UE design, the module may be unpredictable even if it passed manufacturer tests or is in a 4G UE design at lower frequencies.

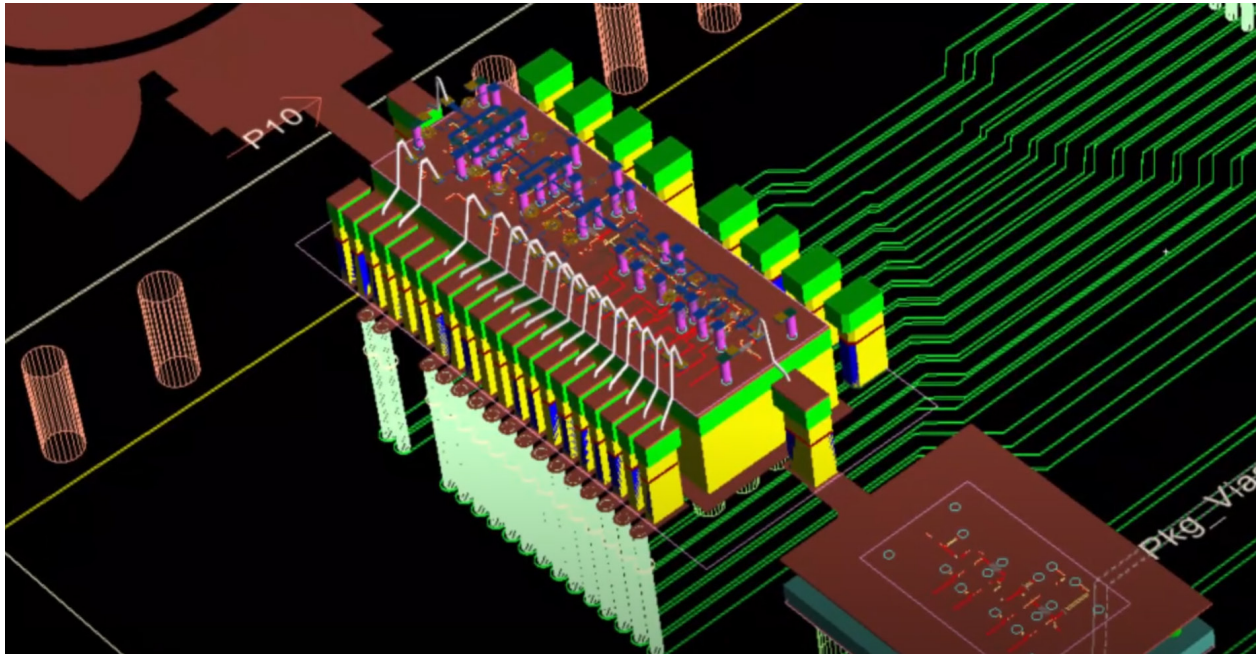


Figure 3. A mmWave RF module with pins and wire bonds, modeled in ADS for RFPPro simulation

Densification demands much higher model fidelity and robust simulation for understanding the inevitable cross-domain interactions that can easily elude simplified setups. Simulating with authentic 5G-modulated waveforms at sufficiently wide bandwidths and characterizing system EVM performance will uncover more design issues earlier in the cycle.

Multi-technology delivers fidelity and reusability. For example, teams can create and simulate structure, chiplet, and module designs, then map them into a complete system design with all their behavioral characteristics for EM / circuit co-simulation. Faster, denser designs become possible with less risk of hardware re-spins.

EM / Circuit Co-Simulation Crosses Domains

Mixed-signal circuit simulations evaluate design functionality, applying bias and signals while observing how outputs change as stimuli vary. Engineers have long used mixed-signal circuit simulations to understand critical portions of their designs but have often relied on hardware prototyping and physical measurements to complete evaluations. Accuracy and simulation times are significant factors for designers to trust the simulation process; if circuit simulations differ too much from measurements or take too long to obtain results in a complex system, engineers tend to run fewer simulations or skip them.

EM simulations evaluate how electromagnetic fields interact in and around designs in three dimensions, as the one visualized in RFPro in Figure 4. With densification in mmWave designs, signals have wavelengths similar to structure dimensions. Parasitics — resistance, capacitance, and inductance unintentionally resulting from semiconductors, packaging, and board layout — can alter circuit behavior. The influence of nearby circuitry or ground and bias planes due to mmWave coupling can also impact circuit behavior. These effects are difficult to anticipate, isolate, and measure in hardware prototypes. EM simulations with high-fidelity models and proper stimuli can reproduce them accurately before starting hardware prototyping.

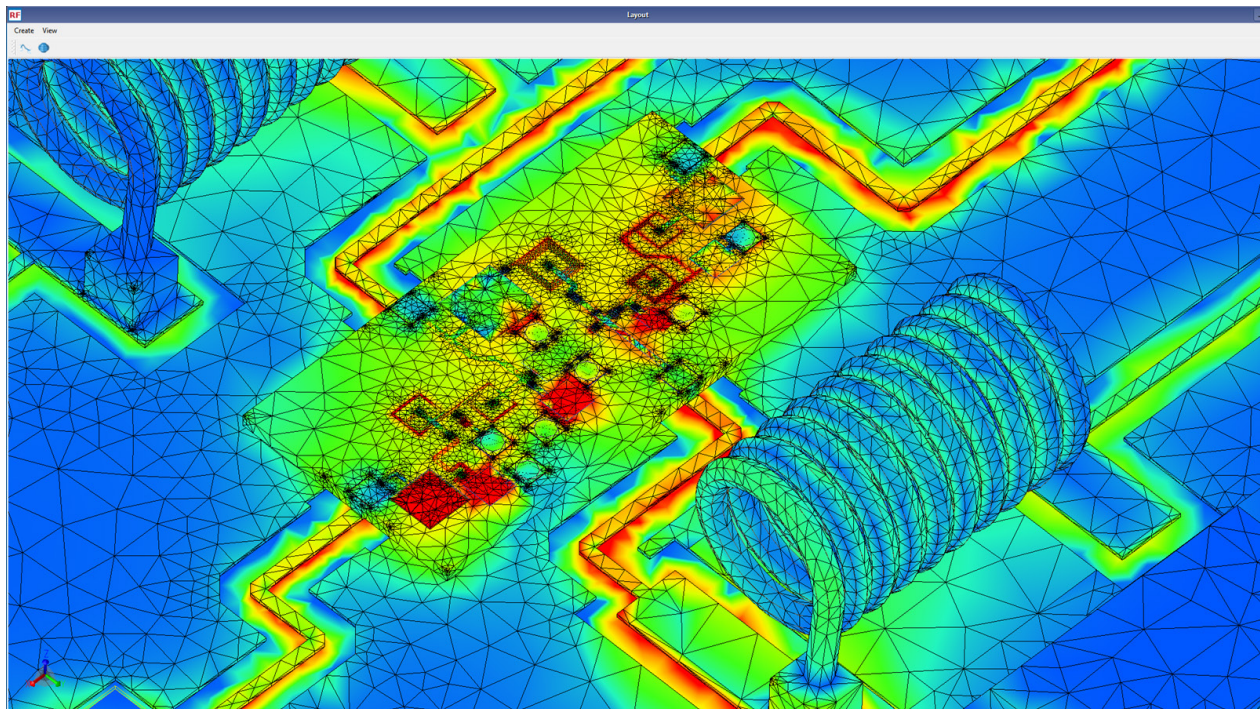


Figure 4. An EM simulation of RF circuitry with current flows visualized in RFPro

If separate tools run the circuit and EM simulation, a complex manual reformatting step converts the layout between the two. The conversion strips components and structures incapable of simulation from the layout, and the EM simulation creates S-parameter files and ports requiring proper reconnection to circuit nodes. If a single error in reconnection corrupts the simulation results, the process must repeat at every transition from circuit to EM simulation and back.

ADS and RFPPro automatically integrate the circuit and EM simulation formatting in one workspace (Figure 5). A 3D layout drives the workflow, and there are no back-and-forth conversions. Adding circuitry updates the appropriate modeling and keeps formatting consistent. Instead of batching up an extensive conversion effort for one EM run when a circuit design is nearly complete, EM / circuit co-simulation in ADS and RFPPro can run iteratively as often as designers choose while refining a design.

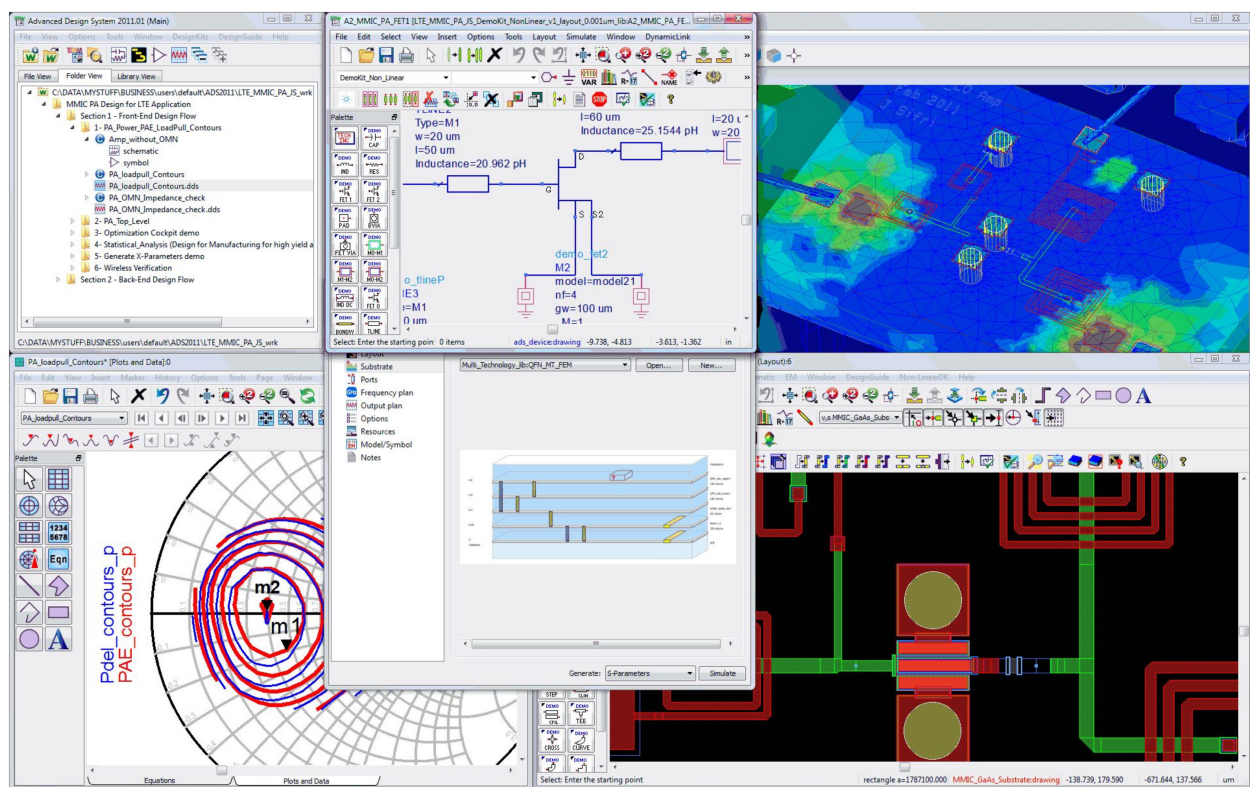


Figure 5. ADS workspace with a 3D layout, EM simulation from RFPPro, load-pull analysis, and more

Tight integration of EM / circuit co-simulation also enables multi-domain analysis. EVM analysis provides an excellent example of modulated signals, densification, power, and parasitic effects testing assumptions and exposing design weaknesses. Effects spread across domains, interacting with complex, hard-to-anticipate results. Two broad categories have different sources and implications.

- Quickly-varying effects are waveform-related, with dependencies in power, frequency, and time domains appearing as nonlinearity, ripple, memory, and charge trapping.
- Slowly-varying effects impact a design's operating point, with dependencies in thermal, load, and bias showing up as self-heating, distortion, and envelope tracking.

These effects appear in Figure 6 and are not entirely separable; complex wide bandwidth waveforms tend to excite all factors simultaneously. ADS and RFPro can efficiently sweep combinations of parameters in the presence of authentic wideband signals, which is hard to accomplish in physical hardware.

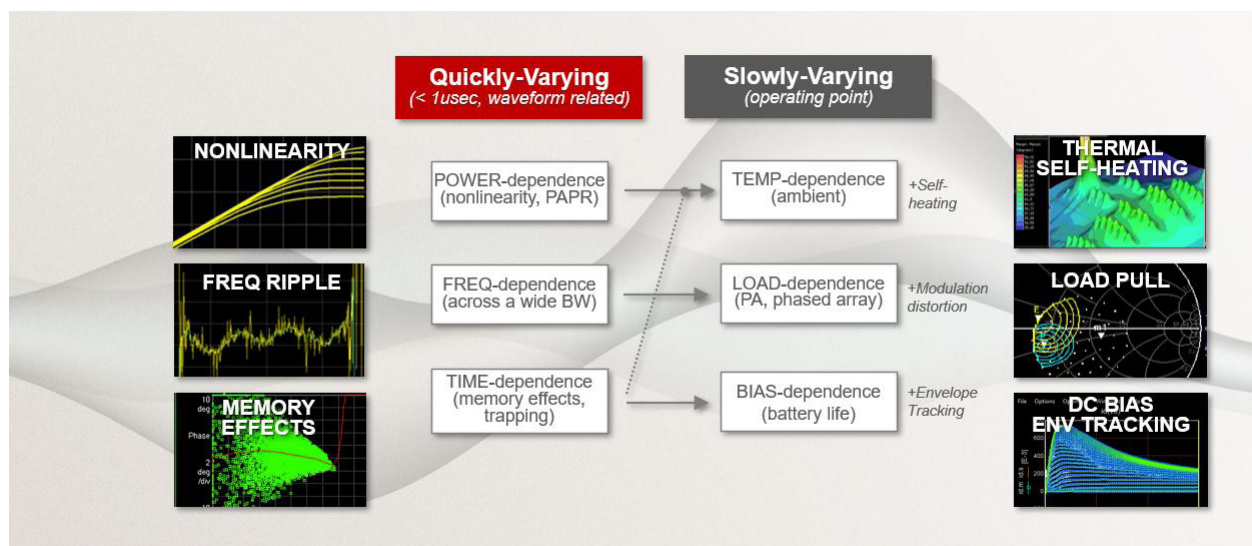


Figure 6. Cross-domain effects can individually or in combination degrade system EVM performance

Robust multi-domain simulation helps designers gain deeper insight into designs through virtual exploration. High-fidelity behavioral models in ADS and RFPro enable EM / circuit co-simulation to replicate real-world effects with hardware prototype-level accuracy.

Multi-Technology and Automatic Mapping

Simulating packaging technology requires understanding the details of materials for proper modeling. Engineers refer to this as "the stack," describing the composition, layers, and dimensions of materials in a chip or board. Introducing a chip package into a design with unknown substrates and wire bonding sends parasitic modeling into uncertainty, which can throw simulation results off enough to shake confidence.

An example of the challenge involved in using fan-out wafer-level packaging (FOWLP) appears in Figure 7. The illustration shows a Si transceiver chip in the left half and a GaAs filter chip mounted on a fan-out redistribution layer in a package on the lower right. This example has four different material stacks.

Computing an accurate 3D model with so many different stacks becomes a problem. With earlier design approaches, EDA solutions used nesting to blend the various substrates at their interface. Nesting requires several manual steps to map the multiple technologies together. It also requires modifying a base design with artificial characteristics inserted to make the blending work. ADS supports nested technology as a legacy method, but a new feature provides a better, more straightforward approach.

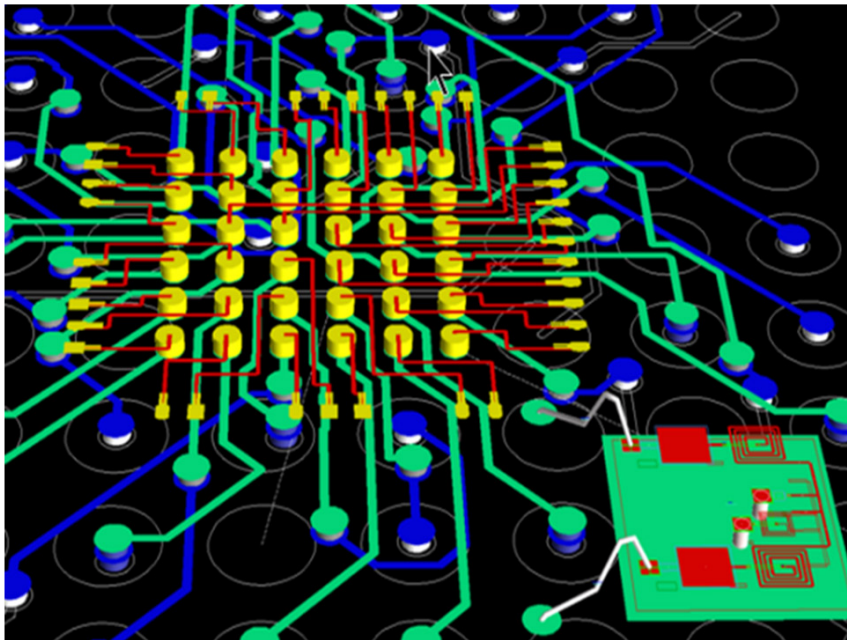


Figure 7. FOWLP reduces wire bonding through direct mounting on a redistribution layer

Smart Mount enables adding a component designed with one technology into a design using different technologies without manual steps, estimation, or modifying the base design. ADS layout automatically maps details from a Smart Mount component into the host design, meshing material parameters, layers, orientation, and alignment. This detailed mapping enables the creation of an accurate EM / circuit co-simulation model in RFPro, including accurate representations of parasitics.

The "drag-and-drop" capability in Smart Mount also creates options for designers, as shown in Figure 8. Optimizing component placements is much easier with automatic mapping following each drag-and-drop. Designers can experiment with stacks, flipping components for top or bottom mounting using a layer on the base as a substrate. Since the components are no longer black boxes but represented with detail in an ADS layout, performance gains may come through altering the design of a FOWLP before committing to chip fabrication. Stacks remap automatically for accurate simulation in any case.

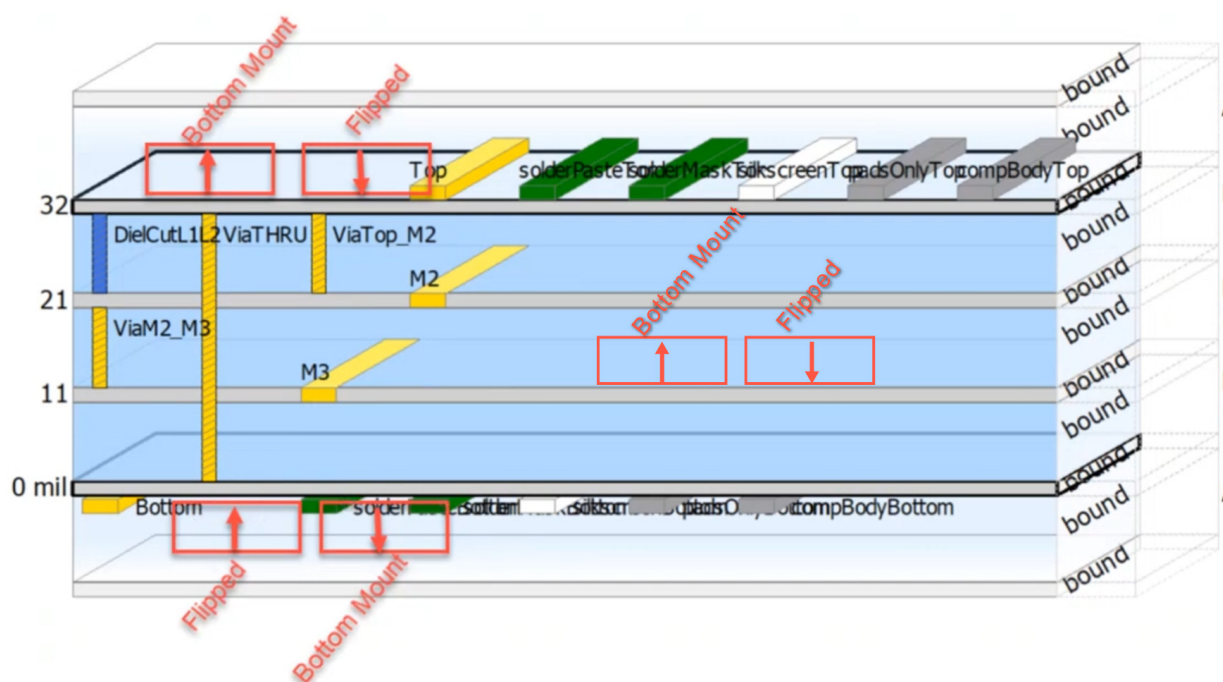


Figure 8. Chips can bottom mount or flip mount on any layer in the base stack using Smart Mount

Productivity gains with Smart Mount can be immense, avoiding the need to manually alter the base board layout every time a component is placed, moved, or deleted. Next, we will examine a common scenario that centers on optimally placing one Smart Mount component in a base layout and replicating the placement several times for additional signal paths. EM / circuit simulations gain accuracy with higher fidelity automated mapping of disparate stack layers with details to gauge cross-domain effects. Automatic mapping of stacks also improves accuracy for thermal modeling and simulation.

Keysight ADS, RFPro, and Smart Mount Provide a Streamlined RF EDA Workflow

Against this backdrop, we will turn to pivotal steps in executing a 5G UE beamforming solution targeted for 28 GHz operation and incorporating eight-layer SU-MIMO. The RF EDA environment for this solution is Keysight's W3608B, bundling the Keysight ADS Core with Smart Mount technology, RFPro, a set of Virtual Test Bench (VTB) libraries, and a new 5G mmWave design kit.

The VTB libraries unify Keysight measurement science between RF EDA simulation tools and test and measurement equipment, which is essential for obtaining accurate results via simulation. The 5G VTB includes authentic 5G waveforms that can source ADS simulations or physical signal generation equipment. The 5G VTB also has the same measurement engine found in the Keysight Vector Signal Analysis (VSA) (89600 VSA), so an analysis of key metrics like EVM or adjacent channel power ratio (ACPR) applies the same algorithm running in virtual or physical space. The VTB libraries also provide a bridge to model-based system engineering tools such as Keysight System Design for working on architectural concepts.

The 5G mmWave design kit, available in the ADS2024 installation, provides a process development kit (PDK) for GaN transistor behavioral models (including Advanced SPICE HEMT and Angelov FET models) operating up to 50 GHz. In addition, it has models for passive components and trace, via, and microstrip discontinuity structures with three metal levels. These models fully integrate into ADS, supporting schematic, layout, EM simulation, thermal simulation, and verification.

The heart of the 5G UE beamforming solution is the RF transmit chain shown in Figure 9 with an array of eight patch antennas, eight combined mmWave phase shifters and power amplifiers, eight flip-chip mmWave small-signal amplifiers, and an 8:1 divider for a total of 17 mmWave integrated circuits (MMICs).

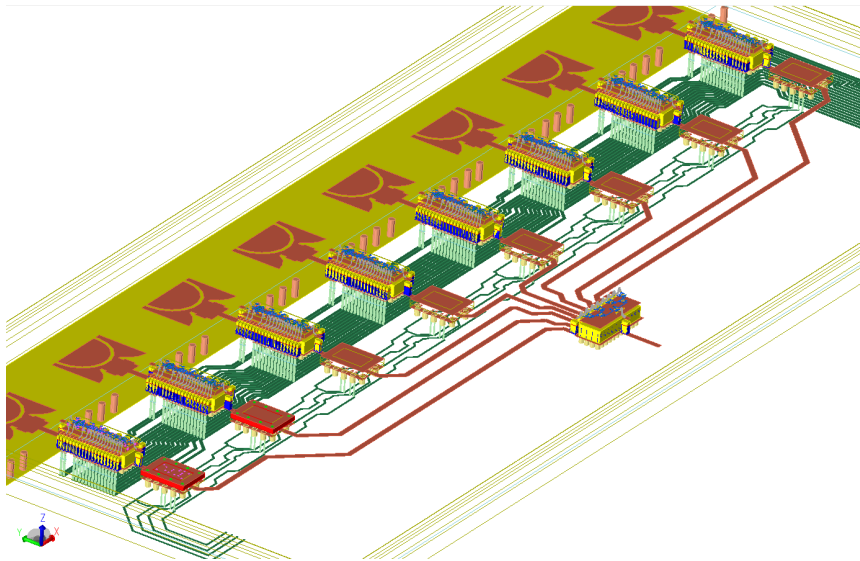


Figure 9. ADS layout for a 5G UE beamforming array with eight antennas and 17 MMICs

Smart Mount technology is essential for the layout and assembly of this transmit chain. A three-layer FR4 circuit board hosts all MMIC components on its top layer, with a ground plane in the middle layer and power / bias planes on the bottom layer. The antenna patches are on the top layer, and a dedicated antenna ground plane on the bottom layer connects with cylindrical vias to the primary ground plane.

The combined phase shifter and power amplifier chip were designed separately into a quad flat no-lead (QFN) package and integrated into the design as a Smart Mount module from a saved ADS design library. Figure 10 shows the ADS layout for this MMIC.

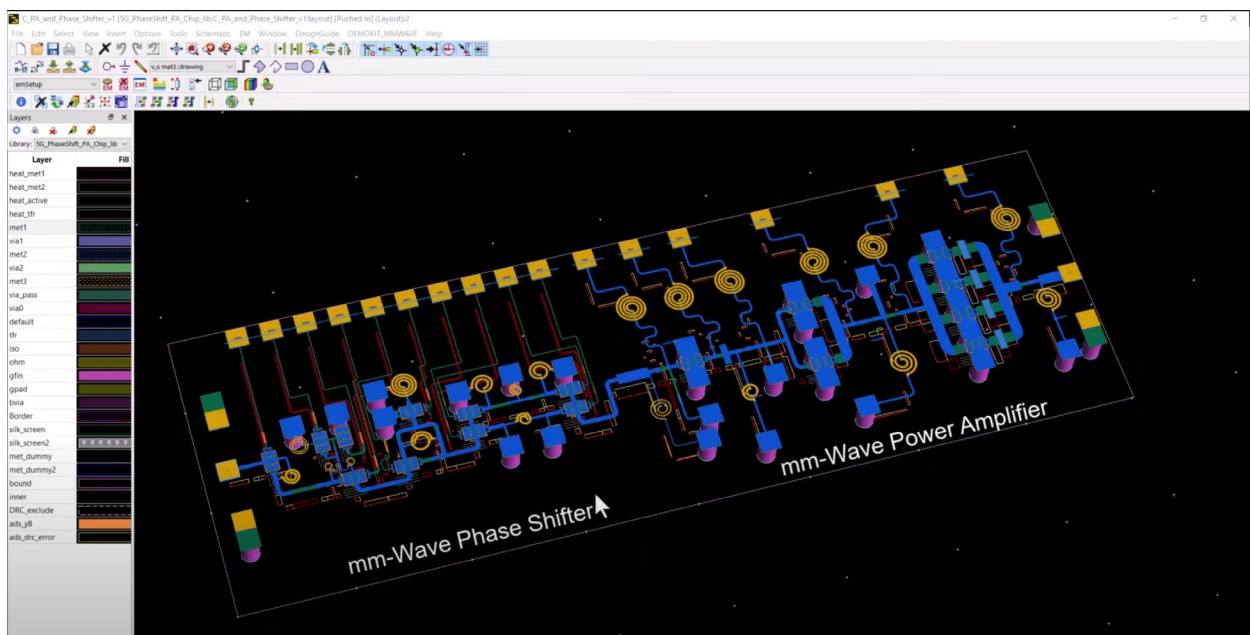


Figure 10. ADS layout for a combined phase shifter and power amplifier MMIC

The QFN chip is bottom-mounted, facing up on the top layer of the base board, with one Smart Mount selection in ADS (Figure 11). The other seven chips are placed similarly at their respective locations.

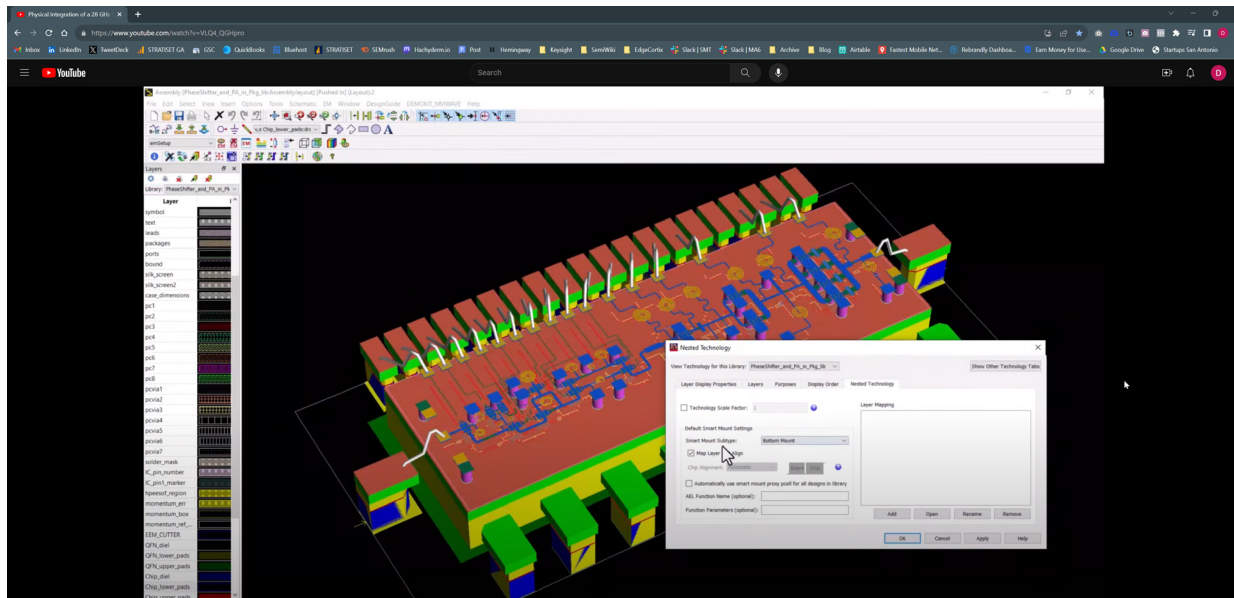


Figure 11. The combined phase shifter and power amplifier MMIC placed using Smart Mount

The eight small-signal amplifier MMICs are slightly different since they are QFN flip chips, handled in Smart Mount by choosing an alternative drop-down option shown in Figure 12. The flip chip ground cover is on top (Figure 13); ADS recognizes the flipped orientation and handles it accordingly.

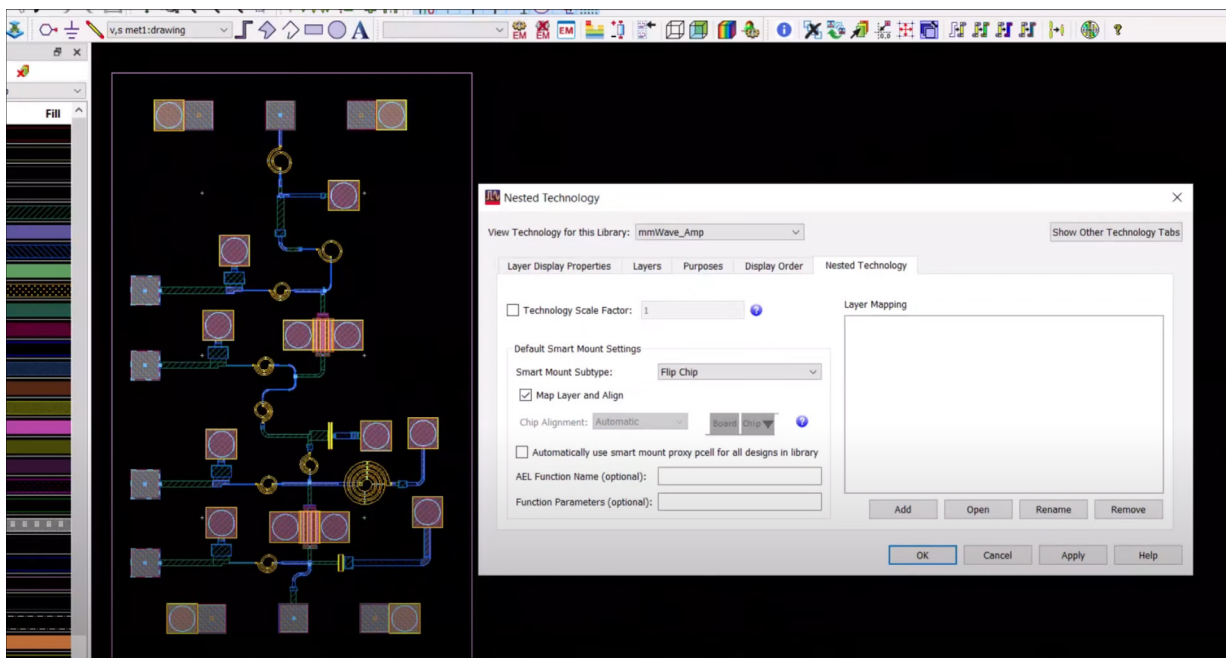


Figure 12. Smart Mount with a flip chip mounting option for the small-signal amplifier MMIC

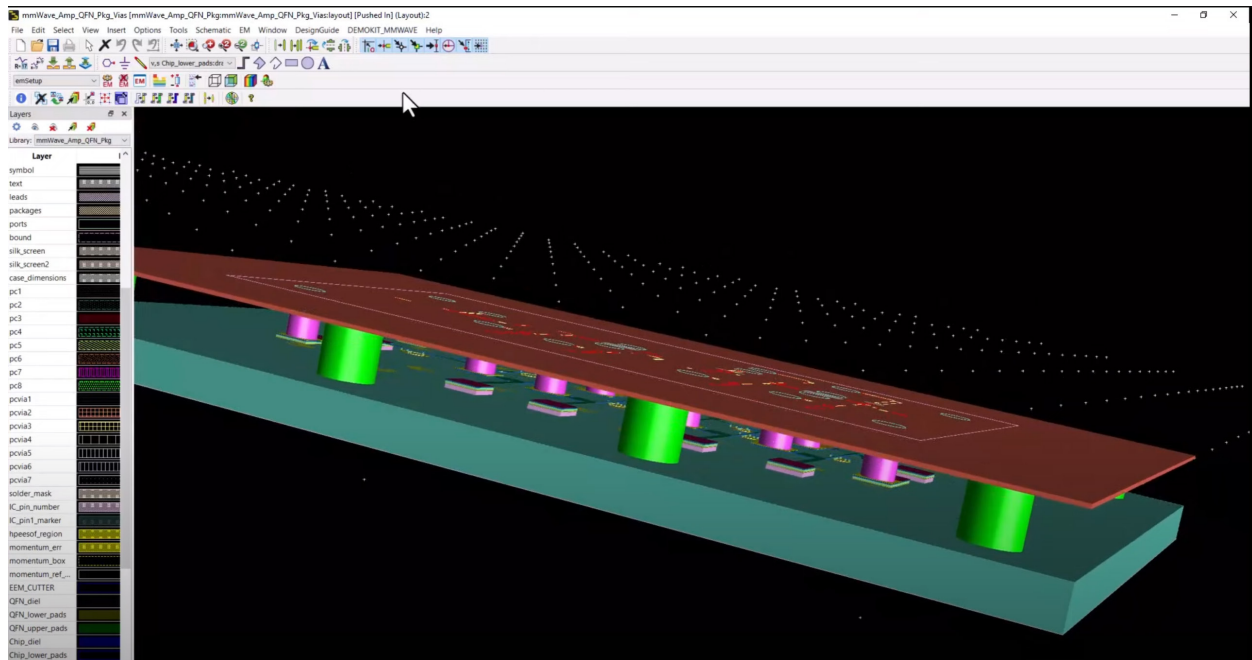


Figure 13. Flip chip with the ground layer on top (brown) and connecting vias (green) through the MMIC's circuit layer

The 8:1 divider MMIC appears on the design similarly, using Smart Mount. The antenna patches, their ground plane, and vias are laid out directly in ADS.

Everything in the streamlined workflow runs in a single ADS workspace and uploaded libraries without manual formatting steps or database conversions. Each placed 3D component assembly meshes with the base board layout in ADS, which then computes layers, orientation, and location, producing a detailed model of the entire stack representing each MMIC and the base board, ready for EM simulation in RFPro.

The same steps would be highly labor-intensive and error-prone without Smart Mount technology. Properly inverting the flip chip alone would be problematic in other EDA environments. This automated solution in ADS places MMICs quickly and accurately, retaining the full model fidelity needed for accurate EM / circuit co-simulation with authentic 5G waveforms and GaN transistor behavioral models.

Coping with 5G mmWave Design Complexity

5G mmWave frequency applications have high-density multi-technology integration and complex digital modulation schemes that push the limits of packaging assemblies for EM and circuit simulations. Keysight's ADS software solution enables 3D layout and assembly for multi-technology RF modules, including RFIC, MMIC, wafer-level packaging, and printed circuit boards (PCBs). The 3D layout avoidance routing and assembly with interactive electromagnetic circuit co-simulation and system analysis accurately account for packaging EM effects during the design phase. These unique design solutions are examples of how RF EDA technology is evolving to improve the predictability of the RF design process and reduce the complexity of design cycles. Now is the time for teams to review their RF EDA workflow, address these critical challenges, and master essential cutting-edge design practices to help compete for 5G design wins.

For more information on these Keysight RF EDA solutions, please visit:

- [What's New in RF and Microwave Design | Keysight](#)
- [Keysight Advanced Design System \(ADS\)](#)
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