WHITE PAPER

Accelerating Semiconductor Innovation through Machine Learning-Driven Modeling

KEYSIGHT

Executive Summary

The semiconductor industry is undergoing a profound transformation as traditional scaling approaches reach their physical and economic limits. Innovation is increasingly driven by advanced device architectures such as Gate-All-Around (GAA) transistors, wide-bandgap materials like GaN and SiC, and heterogeneous integration strategies including chiplets, 3D stacking, and System-in-Package (SiP) designs. These developments demand tighter Design Technology Co-Optimization (DTCO), where process, device, and system-level performance are closely coupled to accelerate iteration and maintain competitiveness.

In this rapidly evolving field, device modeling has become a critical driving force. While traditional physics-based frameworks provide foundational support, they increasingly struggle to capture the nonlinear dynamics, quantum effects, and Multiphysics interactions inherent in modern devices. Simplified equations often fail to account for nanoscale phenomena such as quantum tunneling, self-heating, and variability, thereby reducing predictive accuracy for emerging technologies.

Parameter extraction adds another significant bottleneck. As model dimensionality grows, tuning hundreds or thousands of interdependent parameters becomes a slow, iterative, and error-prone process. Manual workflows struggle to adapt to variations in geometry, temperature, and process conditions, while reliance on domain experts and limited data availability compounds inefficiency.

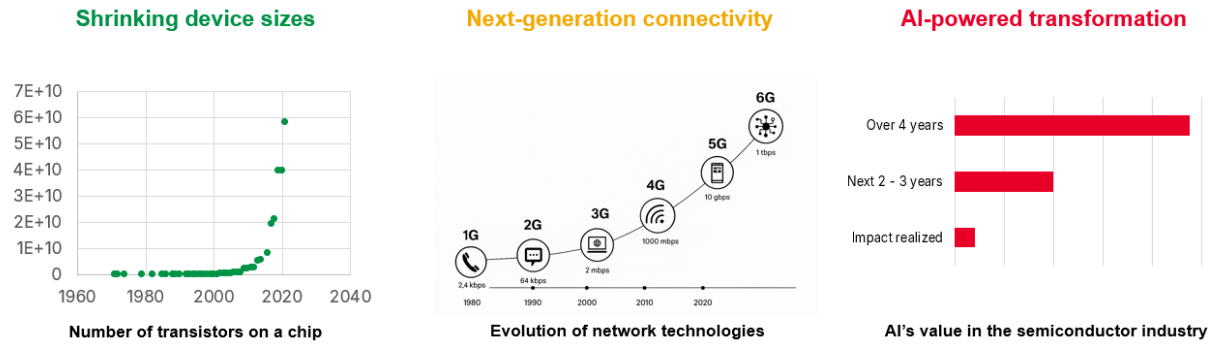

Figure 1. Key Industry trends driving innovation: shrinking device sizes with exponential transistor growth, rapid evolution of network technologies from 1G to 6G, and AI-powered transformation unlocking significant value in the semiconductor industry [1].

Artificial intelligence (AI) and machine learning (ML) are reshaping this domain by offering speed, scalability, and predictive precision [2][3]. Neural networks and hybrid architectures facilitate the rapid development of surrogate models for advanced technologies, eliminating the need for extensive parameter extraction. Additionally, ML-driven extraction focuses on simplifying modeling workflows by reducing the number of extraction steps from hundreds to fewer than ten. These methods deliver high-fidelity modeling across DC, RF, and large-signal domains, while benchmark studies show modeling timelines shrinking from weeks to days. Additionally, AI-driven workflows eliminate manual iterations, improve robustness, and accelerate the delivery of Process Design Kits (PDKs).

In parallel, Large Language Models (LLMs) are emerging as powerful tools within Electronic Design Automation (EDA). Their ability to interpret and generate technical content supports model template creation, simulation scripting, documentation, and parameter-tuning strategies. When integrated with cloud-based platforms, LLMs further enable real-time collaboration and workflow automation, enhancing accessibility and efficiency across global design teams.

Together, these challenges create a scalability ceiling that slows innovation, increases costs, and underscores the urgent need for smarter, more adaptive modeling frameworks capable of automating extraction, generalizing across conditions, and supporting modern DTCO environments.

In this paper, we will discuss how AI and ML revolutionize semiconductor device modeling by replacing slow, manual workflows with fast, automated solutions. We present neural network-based and hybrid modeling approaches that capture nonlinear behaviors directly from data, as well as ML-driven extraction techniques that reduce hundreds of steps to just a few. Benchmarks demonstrate significant gains in accuracy, scalability, and speed across DC, RF, and large-signal domains. These advances enable faster PDK delivery, improved design-technology co-optimization, and a more agile response to rapid technological evolution.

AI/ML for Device Modeling

AI and ML are transforming semiconductor device modeling by offering fast, data-driven alternatives to traditional physics-based workflows. Deep learning, in particular, has become a powerful tool for capturing the highly nonlinear relationships in device behavior. Instead of solving differential equations, neural networks approximate IV, CV, and QV characteristics with high accuracy and reduced computational cost. Several architectures are widely used in device modeling:

- **Feedforward Neural Networks** are simple yet powerful architecture for semiconductor device modeling. It maps operating conditions to electrical outputs through layers of nonlinear transformations, using a one-way flow without feedback loops. This makes FNNs efficient for capturing complex static relationships, often outperforming traditional compact models in accuracy and flexibility [4].

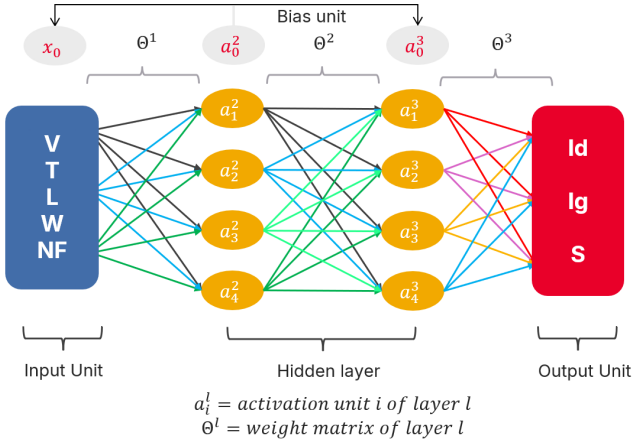

Figure 2. Neural network structure: inputs define operating conditions, hidden layers model nonlinearities, and outputs predict key electrical characteristics.

- **Physics-Informed Neural Networks (PINNs)** embed equations such as Poisson's or continuity equations into the loss function, ensuring physical consistency even with limited or noisy training data [5].
- **Recurrent Neural Networks (RNNs)** are specialized for sequential data, where the output at each step depends on previous inputs. In semiconductor modeling, RNNs are useful for capturing time-dependent behaviors, such as transient responses or dynamic switching events. Their architecture includes feedback loops that allow the network to retain memory of past states, enabling it to model processes that evolve over time [6].

Parameter extraction, a major bottleneck in modeling, also benefits greatly from AI/ML. Modern compact models can include thousands of parameters, making traditional iterative tuning slow and sensitive to initialization. ML-based extractors provide faster, more scalable alternatives:

- **Neural Network-Based Parameter Mapping** learns a direct relationship between device curves and model parameters, avoiding derivative-based optimization and improving robustness against local minima. One promising architecture is the autoencoder-based extractor [2][7], which compresses device data into a latent space and then reconstructs it while simultaneously linking the latent representation to model parameters.
- **Gradient-Based Methods** incorporate ML techniques into numerical optimization, using gradients to efficiently minimize error between measured and modeled characteristics. These methods are fast but require careful regularization to handle highly nonlinear regions.
- **Derivative-Free Optimizations (DFO)** are well-suited for parameter extraction when gradients are unavailable or unreliable in highly nonlinear or discontinuous spaces. Instead of relying on derivatives, these methods use iterative search strategies that handle non-smooth objective functions and complex compact models with strong robustness to local minima. Although generally more evaluation-intensive than gradient-based methods, DFO techniques effectively support multi-objective extraction and offer reliable performance across challenging parameter landscapes [8].

Reinforcement Learning (RL) is well-suited for solving sequential decision-making problems, where an agent interacts with an environment by taking actions to maximize cumulative long-term reward. Unlike supervised learning, RL must handle uncertainty, delayed rewards, and the exploitation trade-off. It is widely applied in domains such as robotics and autonomous driving, where environments are dynamic and short-term rewards may not clearly indicate optimal behavior [9]. Currently, as with many AI algorithms applied to model parameter extraction, the high dimensionality of the number of parameters involved remains a major bottleneck.

In summary, AI/ML introduces powerful, scalable solutions for both device behavior modeling and compact model parameter extraction, dramatically reducing manual effort, improving robustness, and enabling faster deployment of next-generation technologies.

AI/ML Applications in Device Modeling

Neural Network-Based Modeling

Neural network-based modeling is emerging as a powerful solution for advanced semiconductor technologies, especially during early development stages when no mature compact models are available. Neural network models eliminate the need for complex analytical derivations and manual parameter extraction by learning directly from experimental data, enabling faster and more flexible model creation.

Applications of neural network-based modeling, such as NeuroFET [10] and DynaFET [11], have demonstrated strong performance. In parallel with these developments, neural network-based modeling has evolved into a versatile framework that can be applied across a broad range of device types. For example, in the case of GaAs pHEMT devices, separate neural network circuit components were trained by measured data to model the drain and gate currents and charges, then seamlessly integrated into a Verilog-A framework. Figure 3 shows excellent agreement between simulation and measurement. Both the IV characteristics and small-signal parameters exhibited highly consistent and accurate matching, confirming the robust potential of neural network-based modeling for compound semiconductor devices.

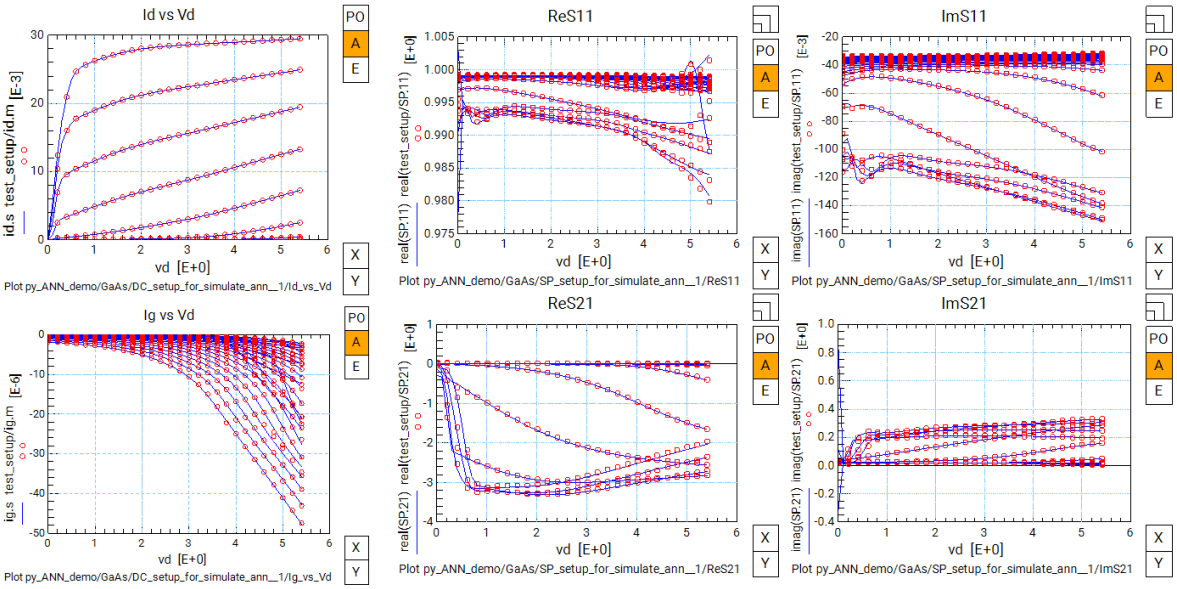

Figure 3. IV characteristics and S-parameters predicted by the neural network model, demonstrating accurate modeling of the GaAs device across multiple bias conditions.

The main insight from this case is that it enables rapid model generation for fast device and circuit evaluation while capturing complex nonlinear behavior directly from data, eliminating the need for explicit physical equations.

Hybrid Neural Network Modeling

For hybrid neural network applications, numerous publications [12][13] and practical use cases have demonstrated their effectiveness in modeling advanced devices such as power MOSFETs, III-V transistors, and FinFETs. This approach can address the limitations of industry-standard models and significantly improve modeling accuracy within a shorter development cycle. Unlike a purely data-driven neural network, the hybrid neural network method retains the physical foundation of traditional models, offering better interpretability of device characteristics and enhanced stability when dealing with device scaling challenges.

Building on the hybrid neural network concept, a practical application is modeling the reverse recovery behavior of IGBT devices under various bias conditions [12]. This phenomenon, validated using the industry-standard Double Pulse Test (DPT), is critical for accurately predicting transient current surges during device switching.

Conventional models describe reverse recovery with nonlinear differential equations, which struggle to maintain accuracy across varying biases and temperatures, as shown in Figure 4. To address this, a hybrid approach is employed: neural networks are used to model key parameters (such as charge storage and release time constants) as functions of voltage, current, and temperature. These neural network modules are then incorporated into the compact model, enabling them to adapt dynamically to different operating conditions.

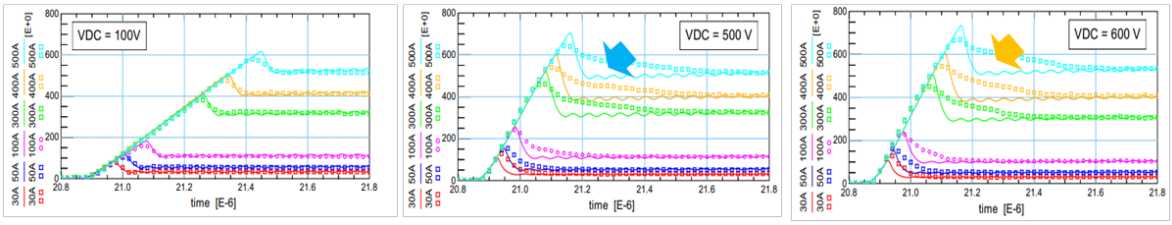

Figure 4. Reverse recovery fitting results for the IGBT model at different biases and room temperature. The model accurately fits the reverse recovery behavior at VDC = 100V, but struggles to achieve precise fitting at higher voltages, specifically VDC = 500V and 600V.

Figure 5 illustrates how the hybrid IGBT neural network model significantly improves the fitting of the reverse recovery waveform, particularly the rising edge, peak current, and falling behavior, across a wide range of voltages. Notable improvements are observed at high voltages, such as 500 V and 600 V. This demonstrates that the hybrid neural network approach is a powerful and practical method for enhancing the accuracy and robustness of device modeling.

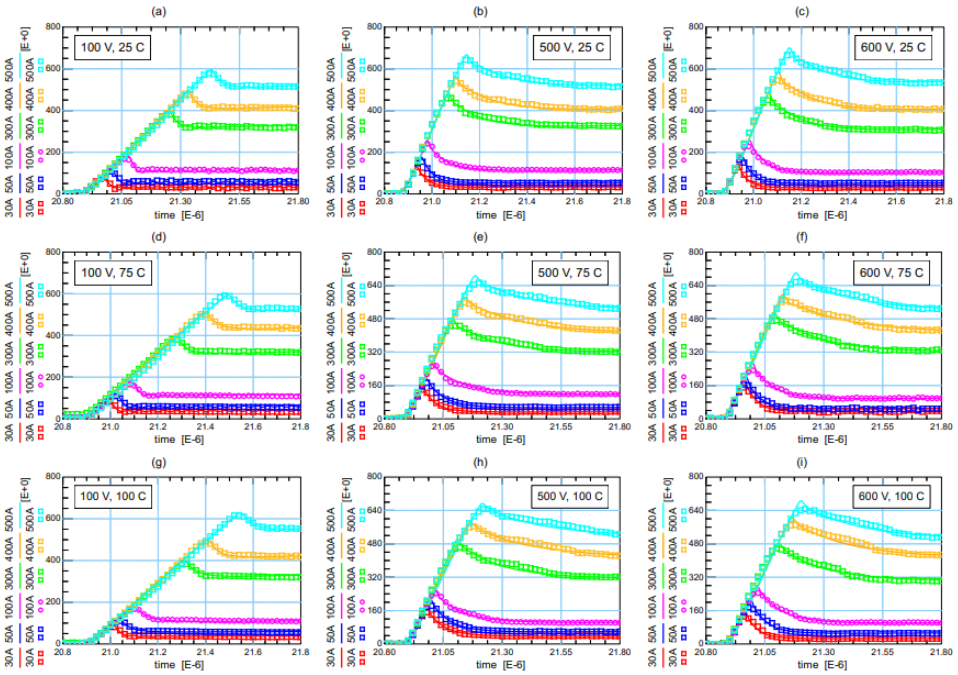

Figure 5. Reverse recovery fitting results using the hybrid neural network approach. The model achieves accurate fitting for VDC = 100V, 500V, and 600V under different temperatures.

From this use case, several key takeaways can be highlighted:

- Combines physics-based models with data-driven learning to capture complex effects beyond traditional formulations.
- Improves fitting accuracy for highly nonlinear and transient behaviors.
- Significantly shortens model development time and effort.

ML-Driven Model Parameter Extraction

ML-driven modeling is a versatile tool for device modeling, simplifying the process even for users with limited experience. As device dimensions shrink, short-channel effects and other complex phenomena become more pronounced, significantly increasing the complexity of the modeling process. Engineers must strike a careful balance between extraction, accuracy, and their expertise, often relying on years of experience to navigate these challenges effectively.

In light of these challenges, one critical objective remains: achieving a repeatable and reliable extraction flow that minimizes development time. Automated, streamlined workflows not only reduce the risk of manual errors but also accelerate the entire modeling process, enabling faster and more consistent device development across generations of technology.

Unlike traditional gradient-based algorithms, which can get stuck in local minima, the derivative-free algorithms explore the entire parameter space to find the best global solutions. They apply to a wide range of device types, provided the underlying model captures key characteristics, automating the search for optimal parameters. This reduces manual tuning and enhances both accuracy and robustness, speeding up modeling workflows.

To demonstrate the effectiveness of the new ML-driven modeling, a comprehensive MOSFET modeling workflow is created using the BSIM4 model. The project covers 36 different device sizes and remarkably requires only 5 to 6 streamlined steps, compared to traditional modeling flow, which often involves over 100 steps. During model fitting, more than 80 model parameters are simultaneously optimized to capture device characteristics, including Id-Vd, Id-Vg, and gm-Vg. As shown in Figure 6, the results demonstrate robust performance across all device sizes, highlighting the workflow's efficiency, repeatability, and capability to handle complex device scaling with minimal development time.

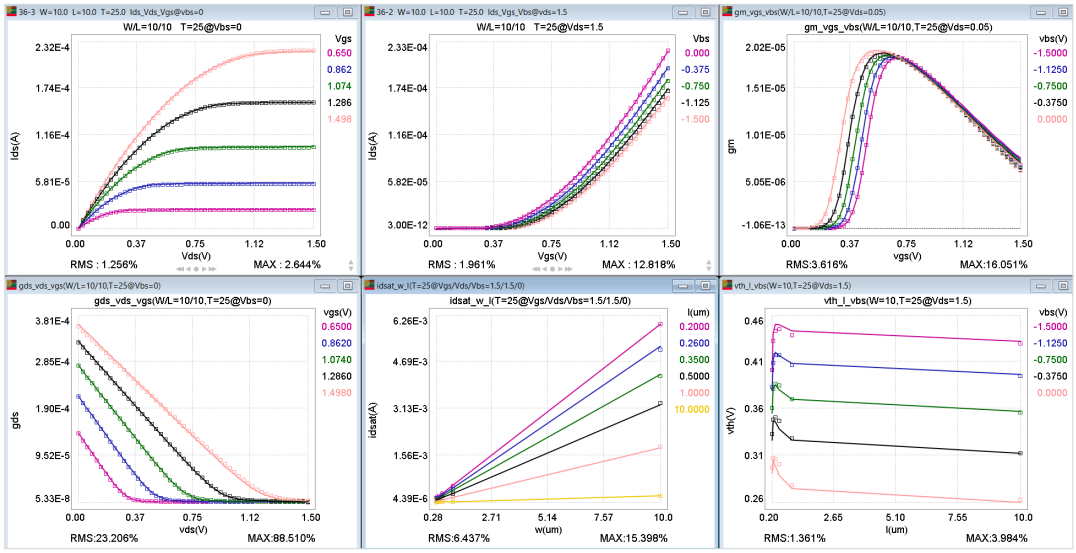

Figure 6. Final fitting results with BSIM4 of key characteristics and scaling plots for the large device, obtained through global optimization across 36 device sizes.

Another powerful application of advanced device modeling is the use of the VBIC model for bipolar transistors. Traditional modeling of such devices requires numerous interdependent parameters and fragmented extraction steps, resulting in a complex and time-consuming process. By applying ML optimization, this workflow is streamlined into just three key steps. This approach efficiently locates the global optimum in a single day, reducing manual intervention and enhancing accuracy. Additionally, the ML-driven method is highly adaptable to a wide range of devices and models, including types such as III-V and FinFET, offering a more efficient and consistent modeling process with minimal effort.

From the new ML-driven modeling, several key takeaways can be highlighted:

- Simplifies extraction steps from hundreds of steps to 5-6.
- Automates modeling with minimal manual effort and errors, enabling stable, repeatable modeling.
- Adapts easily to different device types and compact models.
- Reduces dependency on user expertise, allowing both beginners and experts to achieve high-quality fits.

Performance Benchmark

DynaFET Model

To demonstrate the advantages of the neural network-based model, a benchmark was established based on the DynaFET model, focusing on its predictive accuracy, robustness, and simulation efficiency using a comprehensive measurement. The benchmark employed a 150 nm, 6 × 60 µm GaN HFET from Raytheon Integrated Defense Systems, a device optimized for power amplifier, low-noise amplifier, and switch applications across the 1 to 40 GHz frequency range. Model extraction utilized large-signal data at 100 MHz and S-parameter data at 3.5 GHz obtained from the NVNA setup [11].

Results and Comparison

DC validation: The DynaFET model reproduces measured DC characteristics at 55 °C with high fidelity, accurately capturing nonlinear drain current, gate leakage behavior, and turn-on characteristics. These features, typically difficult for analytical compact models to reproduce, are inherently captured through the neural network's ability to learn coupled electro-thermal and trap-related dynamics.

Broadband S-parameters: The model exhibits excellent agreement with measurements from 0.5 GHz to 50 GHz. This demonstrates the accuracy of the neural network model across the frequency spectrum, as dynamic charge and dispersion effects are implicitly learned from the training data.

Large-signal and power performance: The comparison of gain compression, bias current, Power-Added Efficiency (PAE), and harmonic distortion under large-signal excitation. The DynaFET model accurately predicts both the magnitude and shape of the compression and harmonic trends up to 7 dB of gain compression, while traditional models typically diverge at high power due to fixed functional assumptions and missing dynamic terms.

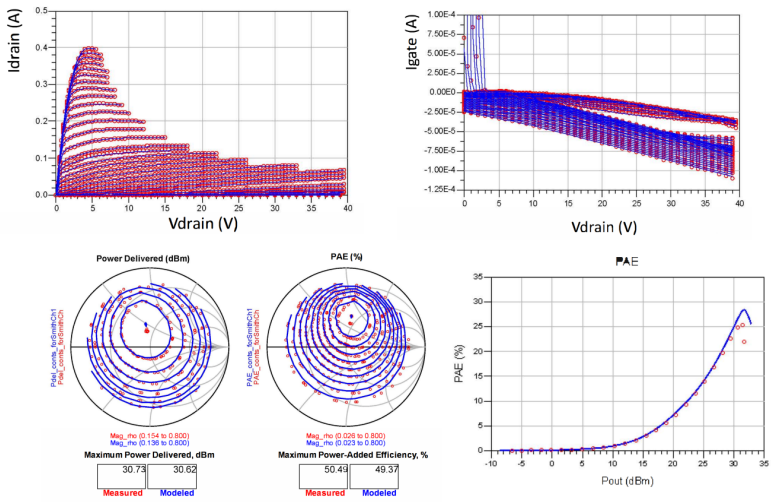

Figure 7. Drain and gate currents (DC), PAE at V = 20 V, I_d = 54 mA, f = 10 GHz, and contours of power delivered and PAE at V_d = 12 V, I_d = 54 mA, Pin = 24 dBm, f = 10 GHz. Modeled (blue) vs. measured (red) [11].

Two-tone intermodulation and load-pull: Modeled and measured results for third- and fifth-order Intermodulation Distortion (IMD) and load-pull metrics confirm that the neural network-based model captures complex nonlinear interactions and dynamic self-heating effects without any additional parameter re-extraction. The agreement extends over a wide range of bias conditions and frequencies, highlighting the robustness and adaptability of the approach.

Key Takeaways

The benchmark highlights that the neural network-based DynaFET model provides superior accuracy, robustness, and usability with 150 nm, 6 × 60 µm GaN HFET. By directly learning complex device behavior from measurement, it eliminates repetitive tuning cycles, improves predictive capability across a wide operating range, and streamlines RF and power electronics design workflows.

Hybrid ASM-HEMT Model

This benchmark compared a hybrid modeling workflow that combines a neural network module with the ASM-HEMT physical model against a baseline using ASM-HEMT alone. The objective was to evaluate the overall improvements in fitting accuracy.

Results and Comparison

The benchmark is conducted on a GaN-on-SiC HEMT device featuring a gate length of 150 nm and a total gate width of 4 × 50 µm. The simulation using the ASM-HEMT model (version 101.4) provides accurate DC fitting while maintaining strong physical interpretability. Under the biased conditions of V_D to 25 V and V_G = –3 to –1 V, and within a frequency range of 250 MHz to 50 GHz, the S-parameter fitting exhibits noticeable deviations, as shown in Figure 8(a). In the figure, the red dots denote measured data, while the blue solid lines represent simulation results.

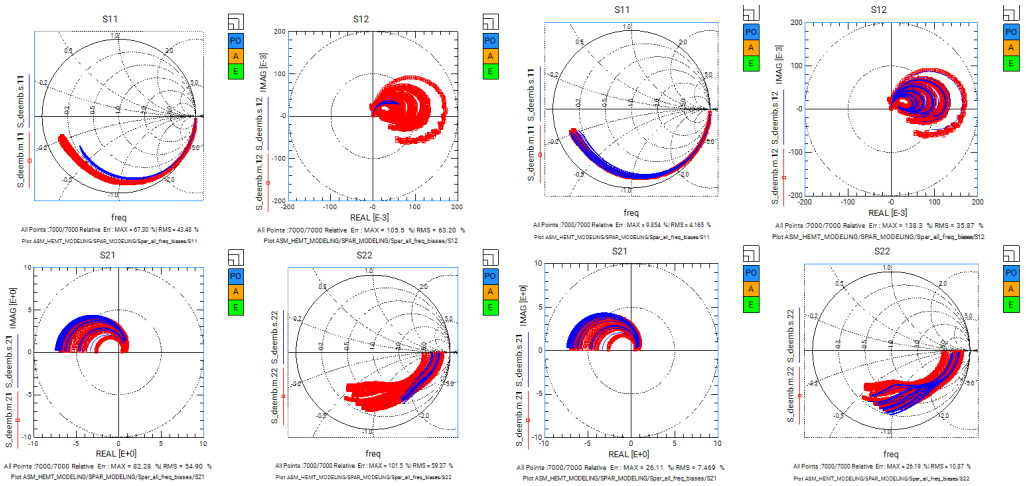

Figure 8. (a) Fitting of S-parameters without neural network. The simulation is done with ASM-HEMT 101.4. (b) Improved fitting of S-parameters with the hybrid ASM-HEMT neural network model.

To enhance high-frequency accuracy, a hybrid ASM-HEMT with neural network model was developed by introducing three additional capacitances and two resistances into the ASM-HEMT baseline. As illustrated in Figure 8(b), this hybrid model significantly improves the agreement between measured and simulated S-parameters, achieving excellent fitting accuracy across the entire frequency range.

Figure 9 illustrates the measured and simulated Pout, PAE, and dynamic load lines (ΔP_{in} = 3 dBm) at a fundamental frequency of 10 GHz with Z_S = 50 Ω and Z_L = 87.2 + j71.3 Ω and biased at V_D = 20 V and V_G = -2 V. The simulation using load-dependent X-parameters with the hybrid ASM-HEMT neural network model aligns well with the nonlinear measurements obtained from NVNA measurements. In contrast, the baseline ASM-HEMT model (without modifications) is less accurate regarding the gain curve and dynamic load lines. This is also evident in the case of S-parameters across a wide range of biased conditions [13].

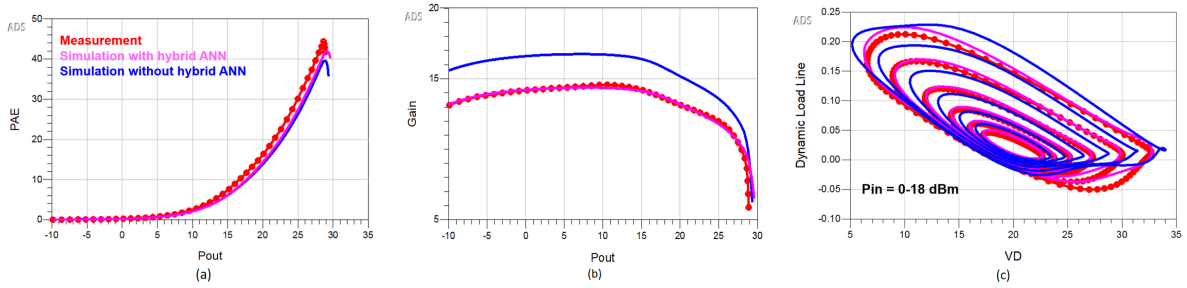

Figure 9. Large-signal simulation results compare measurement, the model without neural network parameters, and the hybrid neural network model. (a) PAE, (b) Gain, and (c) Dynamic Load Line. The hybrid neural network model shows improved agreement with measurement across all metrics, demonstrating its effectiveness in capturing nonlinear large-signal behavior.

Key Takeaways

Hybrid neural network modeling combines the data-driven adaptability of neural networks with the robustness of physical models, offering a scalable and flexible solution to modern device modeling challenges. It enables faster model development, improved accuracy, and preservation of physical integrity.

ML-Driven BSIM4 Modeling

To evaluate the performance of the ML-driven modeling flow, a benchmark was conducted using the BSIM4 model. The objective was to assess improvements in extraction complexity, fitting accuracy, and workflow robustness across different device geometries and operating conditions.

Both optimization flows were tested under identical initial conditions using the same measured IV datasets and parameter initial settings. 36 devices with both large and small sizes and 80+ parameters are included in the flow. The ML-driven modeling applied a gradient-free global search strategy, while the traditional flow used a gradient-based local optimization algorithm. Each flow aims to achieve the best fitting of Id-Vd, gds-Vd, Id-Vg, and gm-Vg characteristics over multiple bias regions and device sizes.

Results and Comparison

Performance	ML-driven Modeling Flow	BSIM4 Traditional Modeling Flow
How many steps	5-6 steps	200+ steps
Sensitivity to Initial Guess	Not sensitive	Sensitive
Multi-Objective Handling	Efficiently optimizes multiple objectives simultaneously, 120+ plots in one step; extraction flow is simple	Poor at handling multiple objectives, few plots in one step; extraction flow is complex
Parameter Correlation Management	Handles parameter correlation well; 80+ parameters can be included in a single step	Poor at handling parameter correlation; only a few parameters can be tuned per step
User Intervention / Manual Tuning Effort	Easily finds global optimum; minimal manual tuning required	Requires many iterations and significant manual tuning
Ease of Setup	Easy to build a modeling flow without extensive prior experience with better accuracy	Requires deep modeling knowledge and experience
Parameter Bound Control	Parameter boundaries are important, but more flexible	Highly sensitive to parameter boundaries
Reusability of Settings	Easy to reuse the created flow for other technologies	Difficult to reuse; requires extensive adjustments

Key Takeaways

- **Streamlined modeling process:** Automates parameter extraction and reduces flow complexity, enabling an intuitive, efficient workflow that boosts productivity.
- **Rapid technology adaptation:** Allows engineers to quickly reuse or adapt modeling flows for new or similar device types, accelerating deployment.
- **Flexible global optimization:** Supports easy definition of parameter ranges, initial values, and fitting regions to efficiently achieve stable, globally optimal results.
- **Reduced expertise dependence:** Minimizes the need for deep modeling knowledge, allowing engineers of all experience levels to achieve high-quality, consistent outcomes.
- **Seamless python integration:** Enables easy automation and customization of extraction flows within Keysight's EDA platform, without requiring advanced programming skills.

Business Impact - Enhancing Competitiveness Through Smarter Modeling

As semiconductor technologies advance and process nodes evolve rapidly, delivering accurate and timely PDKs has become a critical differentiator. Faster, more reliable model development directly influences PDK release schedules, customer adoption timelines, and ultimately, the commercial success of New Production Introduction (NPI). In this environment, adopting AI/ML-driven modeling is not merely a technical enhancement; it is a strategic business imperative.

AI-enhanced compact modeling significantly shortens development cycles by automating traditional manual and iterative extraction workflows. By reducing hundreds of extraction steps to fewer than ten and minimizing reliance on expert-intensive tuning, engineering teams can accelerate model delivery from weeks to days. This compressed cycle time enables earlier design starts for customers, faster validation of new technology nodes, and increased competitiveness in securing early market share.

The improvement in modeling accuracy and predictive fidelity also reduces costly redesigns and post-silicon surprises. High-quality models that closely reflect real device behavior strengthen customer confidence, reduce performance gaps between simulation and silicon, and improve first-pass success rates. For foundries and Integrated Device Manufacturers (IDMs), this translates into more efficient PDK adoption and stronger engagement with ecosystem partners.

Beyond operational efficiency, AI/ML-based modeling enables scalable reuse and repeatability across process nodes, device geometries, temperatures, and corner conditions. Automated optimization and seamless integration with measurement and data-processing workflows allow engineering teams to manage increasing complexity without expanding resources. This creates a sustainable path to innovation, allowing organizations to respond quickly to technological shifts and customer requirements.

Ultimately, intelligent modeling powered by AI/ML enhances productivity, lowers development risk, and accelerates time-to-market—delivering measurable strategic and financial value. By adopting these capabilities today, semiconductor companies position themselves for leadership in a rapidly evolving industry landscape.

Conclusion

As the semiconductor industry advances into an era defined by heterogeneous integration, novel device architectures, and system-level co-optimization, the demands placed on modeling frameworks have grown exponentially. Traditional modeling approaches are increasingly challenged by the complexity, scale, and speed required in modern design environments.

This white paper has outlined how AI and ML are advancing the landscape of semiconductor device modeling. From neural network-based models that eliminate the need for manual parameter tuning to hybrid neural network architectures that blend physical insight with data-driven adaptability and ML-powered modeling workflows, these technologies are enabling faster, more accurate, and more scalable modeling solutions.

The applications and benchmarks presented demonstrate that AI/ML-based modeling not only improves predictive accuracy across DC, RF, and large-signal regimes but also reduces development time, enhances generalization across device variants, and lowers the barrier to entry for model developers. These capabilities closely align with the principles of DTCO, enabling tighter integration among devices, circuits, and system design.

In this rapidly transforming landscape, embracing intelligent modeling frameworks is not just an opportunity; it is a necessity for staying competitive, agile, and future-ready.

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