

Computationally Efficient Design and Optimization

UCle-Based Chiplet Interconnects with Hatched
Ground Planes

Executive Overview

The semiconductor industry is rapidly transitioning from monolithic System-on-Chip (SoC) designs to chiplet-based architectures to meet increasing demands for performance, scalability, and manufacturing efficiency. Standards such as UCIe (Universal Chiplet Interconnect Express) enable high-bandwidth die-to-die communication, but they also introduce significant challenges in interconnect design and modeling.

Unlike traditional on-chip interconnects, UCIe links must deliver extremely high data rates over short physical distances. At these speeds, signal rise times become comparable to propagation delays, causing interconnects to behave as transmission lines rather than simple lumped-element structures. As a result, interconnect design has evolved from a secondary routing concern into a critical determinant of overall system performance.

Compounding this challenge, modern packaging technologies increasingly rely on **hatched or patterned ground planes** to address manufacturing constraints and yield considerations. These non-ideal reference structures disrupt return current paths, introduce spatial impedance variations, and create frequency-dependent electromagnetic effects. At UCIe operating frequencies, the dimensions of these patterns are no longer negligible, invalidating traditional modeling assumptions that treat ground planes as continuous or electrically uniform.

Accurate modeling of these effects requires full-wave electromagnetic (EM) simulation. However, applying full-wave methods across complete multi-lane interconnect buses is computationally costly due to rapidly increasing mesh complexity, memory usage, and simulation time. This limitation restricts design exploration, forcing engineers to make early design decisions without sufficient insight into performance trade-offs.

This whitepaper presents a computationally efficient methodology for the design and optimization of UCIe-based chiplet interconnects with hatched ground planes. The approach combines selective full-wave EM simulation for Vertical Interconnect Access (VIAs) with scalable cross-sectional modeling for uniform interconnect regions. By leveraging the periodicity of patterned ground structures, the method captures essential electromagnetic effects while significantly reducing computational cost.

Implemented within a pre-layout design environment, this methodology enables rapid evaluation of interconnect geometries, materials, and ground plane configurations. Validation against silicon interposer and PCB measurements demonstrates strong correlation with real-world behavior, while achieving substantial reductions in simulation time and memory requirements.

By bridging the gap between accuracy and computational efficiency, this approach empowers designers to perform early-stage, system-level optimization of chiplet interconnects — ultimately enabling more reliable, high-performance designs in next-generation heterogeneous integration systems.

Emerging Challenges in Chiplet Interconnect Design

Electrically Long Interconnects at High Data Rates

In UCIe-based systems, the demand for high data throughput necessitates fast signal transitions across die-to-die interconnects. Although these interconnects are physically short, their electrical behavior is governed by the relationship between signal rise time and propagation delay. As these two quantities become comparable, the interconnect exhibits transmission line characteristics, where reflections and losses must be considered. This shift introduces signal integrity challenges such as managing reflections, impedance discontinuities, and increased susceptibility to crosstalk, thereby elevating interconnect design to a primary performance concern.

Non-Ideal Ground Reference Structures

Advances in packaging technology, particularly in silicon interposers, have led to the widespread adoption of hatched or patterned ground planes. These structures are primarily driven by manufacturing considerations, including stress management and yield optimization. However, they fundamentally alter the electrical reference environment of the interconnect. Unlike continuous ground planes, patterned structures introduce discontinuities that disrupt the natural flow of return currents. Instead of traveling directly beneath the signal trace, return currents must detour around openings in the ground plane, often constricting through narrow conductive regions.

This altered current distribution results in spatially varying impedance along the interconnect. Furthermore, the periodic nature of the ground pattern can introduce frequency-dependent resonances. At UCIe operating data rates, the dimensions of these patterns are no longer negligible relative to the signal wavelength, rendering traditional assumptions of a uniform or averaged reference plane invalid.

Complex 3D Interconnect Topologies

Modern chiplet interconnects are inherently three-dimensional, spanning multiple layers and incorporating a variety of vertical and horizontal transitions. Signals traverse redistribution layers, through-silicon vias, micro-bumps, C4 bumps, and interposer routing structures, creating a highly heterogeneous electromagnetic environment. These transitions introduce strong coupling effects not only between adjacent signal traces but also across different layers of the stack.

In the 32- or 64-lane UCIe buses, the complexity is further amplified by close physical proximity between lanes. This results in both near-end and far-end crosstalk, as well as intricate interactions between signal and return paths. Accurately capturing these effects requires detailed modeling of both geometry and material properties across the entire interconnect path.

Limitations of Full-Wave Electromagnetic Simulation

Full-wave Finite Element Method (FEM) electromagnetic simulation is the most rigorous method for analyzing complex interconnect structures, as it captures all relevant field interactions in spatial elements without simplifying assumptions. However, its application to chiplet interconnect design is severely limited by computational scalability. As geometric detail increases — particularly when modeling fine-grained ground plane patterns — the required spatial elements grow rapidly. This leads to a dramatic increase in both memory consumption and simulation time.

In practical scenarios, even a single interconnect segment of moderate length can require several hours of simulation time and hundreds of gigabytes of memory. When extended to full multi-lane UCIe buses, which require simultaneous modeling of coupling effects across all lanes, the computational burden becomes prohibitive. As a result, design iterations are significantly constrained, often forcing engineers to freeze geometries early in the design process without fully exploring the available design space.

Methodology: Mixed-Domain Electromagnetic Modeling

To balance the trade-off between accuracy and computational efficiency, we propose a mixed-domain **modeling methodology** that partitions the interconnect into regions based on electromagnetic complexity.

Region-Based Decomposition

A typical interconnect is divided into three regions:

Via regions (High complexity)

- Includes vias, bumps, and breakout regions
- Modeled using full-wave FEM simulation

1. Uniform propagation regions (Long interconnects)

- Includes long traces over patterned ground planes
- Modeled using a 2D cross-sectional solver

2. System-level integration

- Results from both regions are combined to form a complete interconnect model

Unit-Cell Based Cross-Sectional Modeling

For patterned ground planes, the interconnect is analyzed using a **unit cell approach**:

- A representative segment of the periodic ground structure is modeled
- Electromagnetic properties are extracted using a quasi-static solver
- Results are extrapolated across the full interconnect length

This approach captures key effects such as:

- Return current redistribution
- Impedance variation
- Frequency-dependent behavior

while avoiding the computational burden of full 3D simulation over long distances.

Selective High-Fidelity Simulation

Full-wave EM simulation is reserved for regions where:

- Geometry is highly non-uniform
- Field interactions are strongly three-dimensional
- Simplified models would introduce significant error

This targeted application ensures accuracy without unnecessary computational overhead.

Tool Implementation: 3D Interconnect Designer

The mixed-domain modeling methodology is implemented in a pre-layout design environment known as 3D Interconnect Designer [Figure 1]. This tool is specifically developed to support the design, simulation, and optimization of chiplet-based interconnect systems in advanced packaging technologies. It provides an end-to-end workflow that allows engineers to move from high-level system intent to full electromagnetic characterization of die-to-die communication paths.

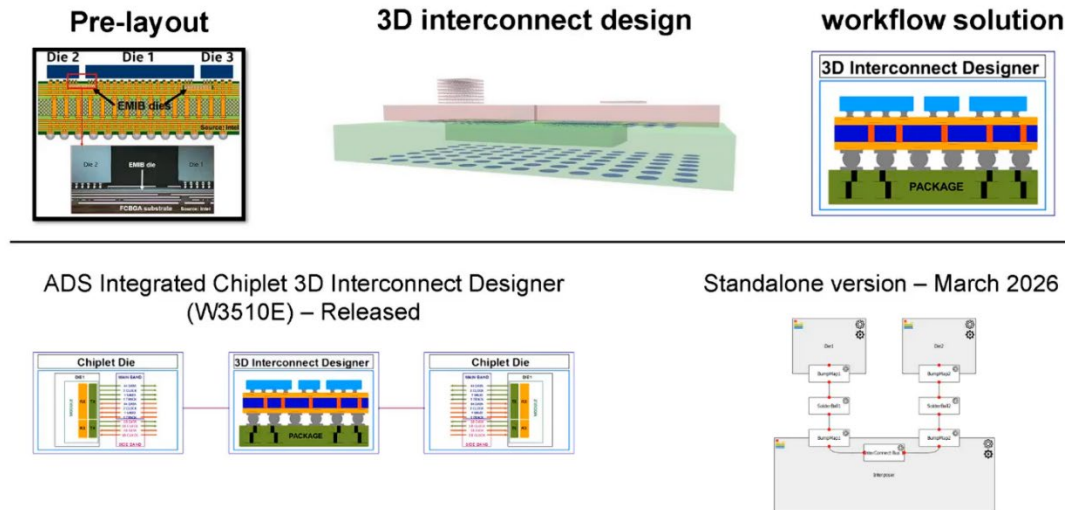


Figure 1. 3D Interconnect Designer

Design Workflow

The tool enables a structured workflow:

1. System Definition

- Define dies, interposers, and interconnect intent
- Configure UCIe or custom bump maps

2. Physical Interconnect Construction

- Define bumps, vias, and breakout regions
- Specify routing layers and geometries

3. Interconnect Bus Modeling

- Assign signal traces and ground references
- Configure hatched ground planes

4. Simulation and Analysis

- Perform hybrid EM simulation
- Extract S-parameters, insertion loss, return loss, and crosstalk

5. System-Level Integration

- Export models for use in circuit simulators
- Evaluate metrics such as eye diagrams and voltage transfer functions

Key Features

From a functionality perspective, the tool provides several key capabilities:

- Parametric definition of chiplet interconnect architectures, including dies, interposers, and bump maps
- Support for UCle and BOW standard interfaces as well as fully user-defined configurations
- Automated generation of interconnect buses from high-level connectivity intent
- Hybrid simulation combining full-wave EM and cross-sectional modeling
- Extraction of S-parameters including insertion loss, return loss, and crosstalk
- Support for near-end and far-end crosstalk analysis in multi-lane buses
- Seamless export to external circuit and system-level simulation environments

In addition, the tool provides advanced design features that allow engineers to explore variations in routing topology, ground patterning, and material selection. This enables rapid comparison of design alternatives and supports early-stage optimization before layout finalization.

Overall, the 3D Interconnect Designer translates the hybrid electromagnetic methodology into a practical engineering workflow. The automated workflow simplifies electromagnetic analysis for high-speed chiplet interconnects, enabling faster design exploration and shorter validation cycles.

Validation and Results

To evaluate the accuracy and efficiency of the proposed hybrid modeling methodology, validation was performed using both silicon interposer test structures and PCB-based implementations. These experiments were designed to assess the ability of the approach to capture the electromagnetic behavior of interconnects with patterned ground planes across a wide frequency range.

In the first validation case, a 6-inch silicon wafer test structure was fabricated, featuring a 2000 μm stripline fully surrounded by a hatched ground plane. The simulated results were directly compared against measured data without any post-measurement tuning or parameter fitting. The comparison showed strong agreement in insertion loss across the entire frequency range, indicating that the methodology accurately captures the dominant loss mechanisms. Additionally, the return loss characteristics exhibited good correlation, and the resonant frequencies were also captured well.

A second validation was performed using a flex PCB with a similar patterned ground configuration. While this structure is not directly representative of UCle interconnects, it provides a useful reference for evaluating the general applicability of the method. In this case, the simulation results closely followed the measured insertion loss trend, although a small offset was observed. Similarly, return loss showed minor deviations. These discrepancies are primarily attributed to uncertainties in material properties and manufacturing tolerances inherent in flex PCB fabrication, rather than limitations of the modeling approach itself.

Beyond accuracy, a key objective of the proposed methodology is to improve computational efficiency. A representative comparison was performed using a 1000 μm single-ended microstrip structure. When simulated using a conventional full-wave EM approach, the simulation required approximately 7.5 hours and consumed 340 GB of memory. In contrast, the hybrid methodology reduced simulation time to approximately 30 minutes while lowering memory usage to 40 GB.

Metric	Full-Wave EM	Proposed Method	Savings
Simulation time	7.5 hours	~30 minutes	~93%
Memory usage	340GB	~40GB	~88%

These results demonstrate that the proposed approach achieves a substantial reduction in computational cost while maintaining high accuracy, enabling practical simulation of complex multi-lane interconnect systems.

Design Impact

The ability to accurately and efficiently model chiplet interconnects has significant implications for the design process. By overcoming the computational limitations of full-wave EM simulation, the proposed methodology enables designers to perform detailed interconnect analysis early in the design cycle, before layout decisions are finalized. This early visibility is critical for identifying potential signal integrity issues and optimizing design parameters prior to committing to fabrication.

In particular, the approach allows for systematic exploration of ground plane patterns, interconnect geometries, and material selections. Designers can evaluate the impact of different configurations on key performance metrics such as insertion loss, return loss, and crosstalk, and can iterate rapidly to identify optimal solutions. This capability is especially important in the context of hatched ground planes, where small geometric variations can lead to significant electromagnetic effects.

Furthermore, the methodology supports full-bus analysis, enabling accurate modeling of coupling effects across wide parallel interfaces. This provides a more realistic representation of system-level behavior compared to single-line simulations, which often fail to capture critical interactions between lanes.

By enabling fast, high-fidelity simulation at design time, the proposed approach removes a major bottleneck in chiplet interconnect development. It allows engineers to move beyond conservative design assumptions and instead make informed, data-driven decisions. Ultimately, this leads to improved performance, reduced design risk, and greater confidence in the final implementation of advanced chiplet-based systems.

Conclusion

The transition to chiplet-based architectures and UCle-driven die-to-die communication has fundamentally changed interconnect design requirements. High-bandwidth signaling over short distances, combined with complex 3D packaging and non-ideal hatched ground planes, introduces electromagnetic effects that cannot be captured using traditional modeling assumptions. Although full-wave electromagnetic simulation provides the required accuracy, its computational cost makes it impractical for full-system, iterative design exploration.

This creates a critical gap in the design workflow: engineers need a modeling approach that is both electromagnetically accurate and computationally efficient enough to support early-stage optimization of complete multi-lane interconnect systems.

The mixed-domain methodology presented in this work addresses this challenge by combining selective full-wave simulation for critical discontinuities with scalable cross-sectional and unit-cell-based modeling for uniform interconnect regions. This preserves essential electromagnetic effects such as return current redistribution, coupling, and resonance behavior, while significantly reducing simulation time and memory requirements.

This methodology is implemented in 3D Interconnect Designer, which integrates the modeling approach into a pre-layout workflow that spans system definition, interconnect construction, routing, and full signal integrity analysis. The tool enables rapid evaluation of design alternatives that were previously too costly to simulate, including variations in ground patterning, trace geometry, materials, and layer stack-ups.

As a result, electromagnetic analysis becomes an iterative design capability rather than a late-stage verification step. Designers can quickly quantify system-level impacts on key metrics such as insertion loss, return loss, impedance, and crosstalk across full UCle buses, and export validated S-parameter models for downstream system simulation.

Validation against silicon interposer and PCB structures confirms strong agreement with measured results while delivering substantial gains in computational efficiency. Overall, the combined methodology and tool flow enable faster design cycles, improved system-level insight, and reduced risk in the development of high-performance chiplet interconnects.

To learn more, visit the following :

[Chiplet & 3DIC Interconnect Design Solutions | Keysight](#)

[W9100E 3D Interconnect Designer - Standalone Version | Keysight](#)



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