

Power Integrity in High-Current Systems: Understanding Ground Bounce and Electromagnetic Interference

Executive Overview

The rapid advancement of high-performance computing, Artificial Intelligence (AI), and modern semiconductor packaging technologies has fundamentally transformed the requirements placed on Power Delivery Networks (PDNs). Today's systems must support extremely high transient currents, often reaching thousands of amperes with nanosecond-scale slew rates. These operating conditions introduce significant Power Integrity (PI) challenges, including excessive power rail voltage ripple, ground bounce, and Electromagnetic Interference (EMI), all of which can impact system performance and reliability.

The increasing need for higher currents to switch millions of transistors is simultaneously driving power rail voltages ever lower to balance power consumption with performance. Power integrity is quickly evolving from a secondary design consideration into a primary system constraint. Under these conditions, PDN behavior is inherently dynamic and strongly dependent on frequency. Traditional assumptions of an ideal constant ground reference are no longer valid. Instead, the ground network is a distributed impedance structure, where voltage varies across both space and time. These variations give rise to ground bounce, which directly affects signal integrity and serves as a key contributor to EMI.

This white paper demonstrates the comprehensive framework of Keysight's ADS with PIPro for understanding, modeling, and mitigating these PDN effects in modern high-current systems. It highlights the critical role of electromagnetic (EM) simulation in capturing distributed parasitics and return path behavior, as well as the advantages of combining this with harmonic balance circuit simulators for efficiently solving transient non-linear behavior. This combination of EM models with circuit simulators in one ADS design environment simplifies the creation of an end-to-end power integrity digital twin. Creating a PI digital twin enables accurate system-level analysis that integrates voltage regulator behavior, PCB PDN characteristics, and dynamic load interactions.

By combining these methodologies, engineers can more effectively predict and manage noise mechanisms, reduce design risk, and ensure compliance with increasingly stringent performance and EMI requirements in next-generation electronic systems.

Ground Bounce as a Dynamic Phenomenon

Shared Return Path Effects

Understanding the growing system constraints around power starts with identifying key design challenges. One of the hardest to diagnose and prevent is ground bounce. In typical PCB designs, multiple power rails and signal nets share a common ground return path. When large transient currents flow through this shared impedance, voltage fluctuations occur across the ground network.

These fluctuations:

- Vary by physical location.
- Depend on the current magnitude and slew rate (di/dt).
- Affect all signals referenced to the shared ground.

Direct measurement of ground bounce is complicated by the need to separate out voltage ripple on the power net from the voltage ripple on a ground net. Instruments are designed to make differential measurements across power and ground at a measurement point. Simulators typically match measurements and use differential measurements to reduce complexity. Enabling the separation of ground bounce from other noise sources requires specialized tools for the job.

AC Nature of Power Delivery

Ground Bounce as the name describes is a dynamic problem. In general, power delivery is an AC problem rather than a pure DC one. High-speed digital loads generate transient currents that excite inductive and capacitive parasitics in the PDN.

The resulting voltage noise is dominated by the inductance in the path and can be approximated by:

$$V = L \cdot \frac{di}{dt}$$

This relationship highlights how even small inductances can produce significant voltage ripple under high $\frac{di}{dt}$ conditions. The path inductance is in both the power network and the ground return network creating voltage ripple on the power net and ground bounce on the shared return path.

Target Impedance and PDN Design

Target impedance is a foundational concept in power integrity engineering that addresses this challenge of inductance in the power delivery path. Target Impedance defines the allowable impedance of a Power Delivery Network (PDN) across frequency. It is determined by the ratio of the maximum allowable voltage ripple to the maximum expected transient current. This relationship establishes a design constraint that ensures the voltage seen by the load remains within specification under dynamic conditions.

While the definition of target impedance is straightforward, its practical application is complicated by the frequency-dependent nature of real PDNs. Impedance is not constant; it varies due to the combined effects of capacitive, inductive, and resistive elements distributed throughout the system. At low frequencies, the Voltage Regulator Module (VRM) and bulk capacitors dominate and reduce impedance. At higher frequencies, parasitic inductance becomes significant, causing impedance to rise. Between these regions, resonances can occur, producing sharp impedance peaks that may be excited by switching activity and lead to excessive voltage ripple.

As system architectures evolve toward lower supply voltages and higher current demands, the target impedance decreases dramatically, easily reaching the micro-ohm range. This scaling trend significantly increases sensitivity to parasitic elements in the PCB layout, package, and discrete components. In such regimes, even small inductances associated with vias, planes, and capacitor mounting structures can dominate the PDN response. Consequently, traditional lumped-element circuit models become insufficient, and distributed electromagnetic effects must be considered to accurately predict system behavior.

The Role of EM Simulation

Electromagnetic (EM) simulation has become an essential tool in modern power integrity design due to the distributed nature of high-speed, high-current PDNs. Unlike simplified circuit models, the full-wave EM simulation in Keysight's PPro tool captures the spatial distribution of currents and fields within the PCB, enabling accurate characterization of parasitic inductance, capacitance, and coupling effects. By importing detailed PCB layout data into a three-dimensional EM environment, designers can evaluate both DC and AC behavior, including impedance versus frequency, return current paths, and localized resonance phenomena.

In addition to electrical effects, thermal considerations play a critical role in high-current systems. As current density increases, resistive losses generate heat, which in turn alters the resistivity of the material. This DC electrothermal interaction can significantly impact PDN performance and reliability. Modern simulation workflows integrate DC IR drop analysis with thermal modeling, allowing iterative solutions that account for temperature-dependent behavior. Such co-simulation enables the evaluation of cooling strategies, including forced air and liquid cooling, and helps prevent catastrophic failures such as thermal runaway or material degradation.

The combination of electromagnetic and thermal simulation provides a comprehensive view of system behavior, ensuring that both electrical performance and thermal integrity are maintained under high dynamic current conditions.

Power Integrity Digital Twin

Target impedance and EM models of the PCB PDN are essential, but they do not tell the whole story. Real hardware performance is determined by the interaction of the dynamic control loop behavior of the switching voltage regulator and the dynamic load with the frequency dependent impedance of the PDN. A power integrity digital twin is a comprehensive system-level model that represents this complete power delivery path from the voltage regulator to the semiconductor load. This modeling approach integrates multiple domains, including the Voltage Regulator Module (VRM), the PCB power delivery network, decoupling capacitors, and the package and die. By capturing the interactions between these elements, the digital twin enables accurate prediction of both time domain and frequency domain behavior.

A critical component of the digital twin is the active switching VRM model. To achieve both accuracy and computational efficiency, behavioral models based on state-space averaging are commonly used. These models use small signal ac behavior to describe the control loop dynamics of switching regulators without requiring explicit simulation of every switching event, allowing rapid convergence while preserving essential system characteristics such as output impedance, control loop stability, and transient response. At the same time, the small signal solution can drive dynamic switches to simulate the large-signal behavior like dynamic switching ripple and nonlinear interactions with dynamic loads. In the ADS environment these models can run in traditional transient simulations or used in Harmonic Balance to quickly solve for steady state noise ripple.

Accurate passive component modeling is equally important. Capacitor models provided by vendors often include implicit parasitic elements that may not be clearly specified. Without proper validation, these models can introduce errors such as double-counting PCB mounting inductance, leading to artificial impedance peaks in simulation results. Measurement verification is therefore necessary to ensure component model fidelity. Additionally, inclusion of passive package and die PDN models is required to extend the impedance characterization across the full frequency spectrum relevant to the load.

By combining these elements into the unified ADS simulation environment, the Power Integrity digital twin enables end-to-end analysis of the PDN with static and dynamic load conditions. Utilizing PI digital twins during pre and post layout design stages enable design optimization, trade-off evaluation, and risk reduction prior to hardware fabrication.

Harmonic Balance Simulation

Advantages

Power Integrity digital twin simulations do add complexity that can cause excessive simulation times when using traditional transient simulators. To speed up simulation time and enable engineers to quickly assess steady state behavior, a less known Harmonic Balance simulator can be used. Harmonic Balance (HB) simulation is a frequency-domain technique particularly well suited for analyzing power delivery networks driven by periodic switching activity. Unlike a traditional time-domain transient simulation, which must iterate through many time steps to reach

steady-state conditions, harmonic balance directly solves for the steady-state response at individual frequencies in the frequency domain. Simulating at the fundamental frequency of a periodic active element along with hundreds of harmonics allows for Fourier theory to convert the steady state frequency behavior to steady-state time domain voltage and current transients. This makes it especially effective for systems with repetitive behavior, such as switching regulators and periodic dynamic loads.

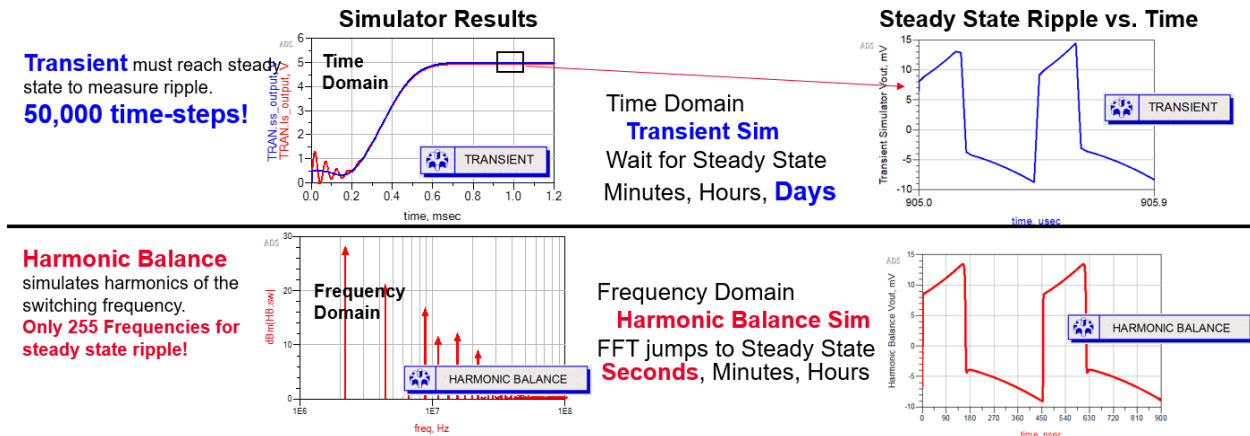
Harmonic balance offers key advantages in power integrity analysis:

- **Direct steady-state solutions**
Harmonic balance computes the steady-state response without requiring simulation of startup transients. This eliminates the need to simulate long settling times before meaningful data can be extracted, allowing engineers to focus immediately on the voltage ripple, current distribution, and spectral content under operating conditions.
- **Reduced simulation time**
By solving the system in the frequency domain using a limited number of harmonics, harmonic balance significantly reduces computational effort compared to time-domain approaches. Instead of thousands or millions of time steps, the simulation evaluates only the fundamental switching frequency and its harmonics, enabling results to be obtained in seconds or minutes rather than hours or days for complex PDNs.
- **Efficient handling of nonlinear systems**
Harmonic balance is inherently suited to systems with nonlinear components, such as switching voltage regulators and dynamic load models. It iteratively balances nonlinear device behavior in the time domain with linear network behavior in the frequency domain, enabling accurate simulation of large-signal effects, including switching ripple, duty cycle modulation, and interactions between the load and voltage regulator.

These advantages make harmonic balance an essential tool for modern power integrity workflows, particularly when analyzing high-current, high-speed systems where both nonlinear behavior and steady-state accuracy are critical.

Comparison with Transient Simulation

Selecting the appropriate simulation method is critical for balancing accuracy and computational efficiency in power integrity analysis. The integrated ADS environment has both a transient and a harmonic balance simulator that can be used for PI digital twin simulations. If the transient behavior is periodic, then harmonic balance has an advantage. This advantage is summarized in the figure below showing the fundamental differences between time-domain transient simulation and frequency-domain harmonic balance.



Method	Characteristic
Transient	Solves in the time domain Slow convergence to steady-state transient behavior
Harmonic Balance	Solves in the frequency domain Rapid steady-state transient behavior

HB simulation reconstructs periodic time-domain behavior using Fourier synthesis, significantly improving simulation efficiency.

High di/dt Load Modeling

The benefit of Harmonic Balance can be extended to dynamic load modeling. Accurate modeling of high di/dt loads is essential for predicting power integrity behavior in modern electronic systems. Advanced processors, AI accelerators, and high-speed digital devices exhibit extremely fast transient current demands, often switching hundreds or thousands of amperes within nanoseconds. These rapid transitions excite the full bandwidth of the power delivery network, making it necessary to model the load not as a static element, but as a dynamic and time-varying excitation source.

Traditional specifications are written in terms of a single turn-on step load event, or a single turn-off load dump event. In practicality, even on a test bench this step load and load dump are cycled on and off in a periodic fashion so that an oscilloscope can easily trigger on the event and capture the power rail voltage droop, kick, and resonances. This periodic nature of the load is ideal for taking advantage of fast Harmonic Balance simulations.

Dynamic loads are modeled using:

- Periodic current modulation
- A resistive switching element
- Parameterized rise/fall times

These models enable accurate representation of real-world transient behavior, including:

- Turn-on and Turn-off step loads
- Worst-case forced transient load excitation
- Nonlinear interactions with switching voltage regulators

The need for a periodic current load model in harmonic balance ends up being a benefit for the PI digital twin simulation. Not only does it allow for step load turn-off and turn-on in one simulation, but it also enables worst case forcing of system resonances with non-linear behavior.

Conducted EMI Fundamentals

Now that there is an understanding of the models that make up a Power Integrity digital twin the next step is to apply the models to a real-world PI challenge. Conducted Electromagnetic Interference (EMI) arises primarily from common mode currents, which differ fundamentally from the intended differential current flow in electrical systems. In an ideal differential configuration, current flows along a defined path and returns through a designated return path, resulting in minimal external field radiation. However, when common mode currents are present, currents flow in the same direction on both the signal and return conductors. This imbalance forces the electromagnetic fields to extend beyond the intended paths, inducing currents on unintended structures and leading to both conducted and radiated emissions.

The sensitivity of EMI compliance to common mode currents is significant. Even extremely small micro-Amps of current can produce voltage levels that exceed regulatory limits. As a result, understanding and controlling common mode behavior is critical for ensuring electromagnetic compatibility.

Standard conducted EMI testing is performed using a Line Impedance Stabilization Network (LISN), which provides a controlled impedance interface between the equipment under test and the measurement bench power source. The LISN also enables measurement of noise voltages using a spectrum analyzer. A key aspect of this setup is the presence of a reference metal ground plate, which establishes a consistent return path for measurement purposes while isolated from the ground of the electrical unit under test. Accurate EM simulation of conducted EMI must replicate these conditions, including the differential measurement configuration and the reference ground plate environment. The reference ground plate is often called a reference ground plane in simulation of multi-layer PCB structures.

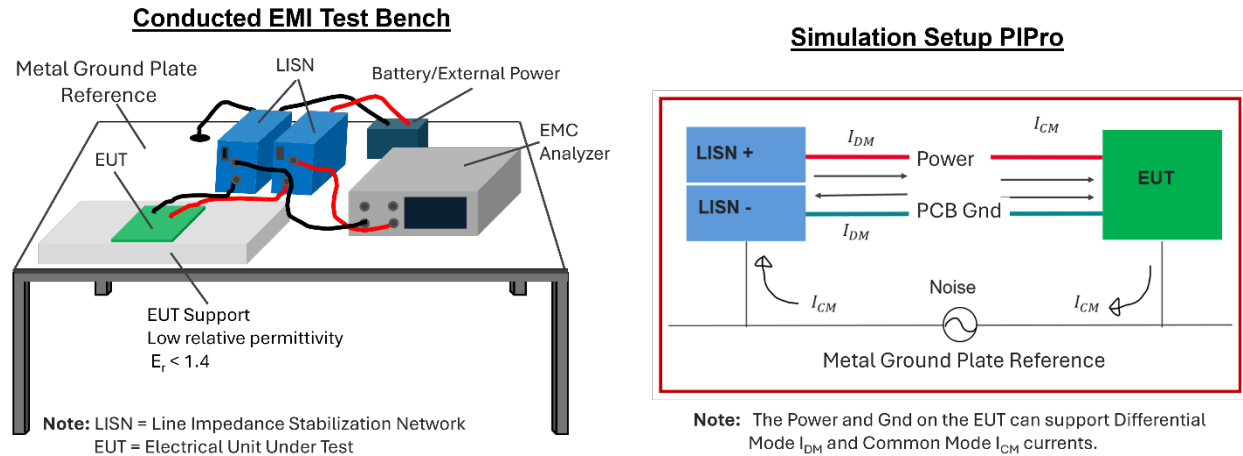


Figure 1. Conducted EMI measurements use a metal ground plate reference so that the differential and common mode currents can be measured on the power and ground nets. In simulation the PIPro EM tool automatically adds this ground plate in the Conducted EMI Analysis.

By modeling both differential and common mode currents within the ADS PIPro EM simulation framework, engineers can predict EMI performance early in the design cycle and implement mitigation strategies before physical testing.

Crosstalk and Ground Bounce Separation

The ability to simulate differential and common mode currents in a power delivery network has far reaching benefit, going beyond what is possible in measurement. While measuring conducted EMI at a power connector is well defined, physically measuring voltage and currents at any location on a PDN is not practical. Simulation on the other hand can measure anywhere in the network, and with the addition of a reference ground plane, it becomes possible to separate out ground bounce from power rail voltage ripple and net-to-net crosstalk. In multi-rail power delivery systems, noise coupling between different power domains is a critical concern. To describe this interaction, one can leverage the signal integrity terms of aggressor net and victim net, where the aggressor is a high dI/dt power rail generating significant transient currents, and the victim is an adjacent power net or a sensitive signal net. The observed noise on the victim net arises from two primary mechanisms: electromagnetic coupling between nets (crosstalk) and voltage fluctuations on the shared ground return path (ground bounce).

Distinguishing between these two mechanisms is essential for effective mitigation. Crosstalk results from capacitive and inductive coupling between adjacent conductors, allowing energy to transfer directly from the aggressor net to the victim net. In contrast, ground bounce is caused by voltage variations along the shared ground network due to the finite impedance of the return path. Since both effects can produce similar voltage disturbances at the victim node, separating them requires careful EM simulation techniques.

One effective approach used in PIPro involves the use of single-point voltage probes referenced to an external ground plane. Unlike traditional differential measurements, which capture the voltage between two nodes, this method measures the absolute voltage of a node relative to a common reference. By analyzing the common mode voltage at separate locations on the ground network, it becomes possible to quantify the contribution of ground bounce independently of direct net-to-net coupling.

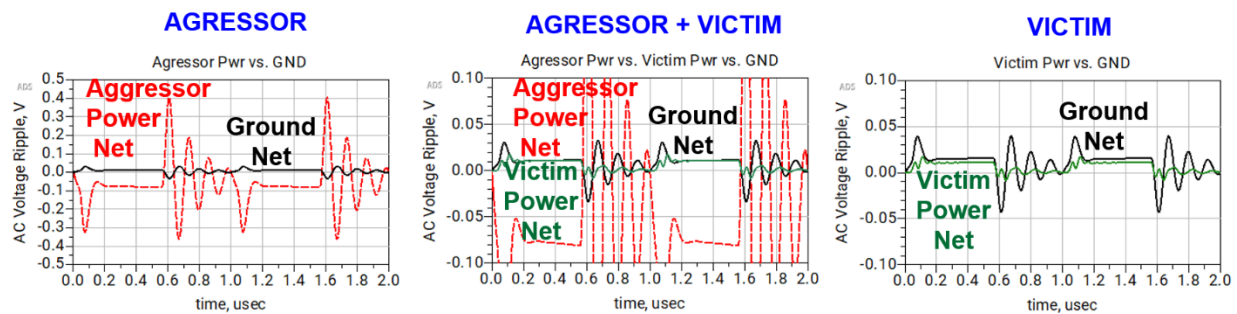


Figure 2. The plot on the left shows the voltage ripple on the Aggressor power net and ground return. The middle plot shows the Aggressor and Victim nets with the same shared ground return on the same plot with the scale zoomed in. The plot on the right keeps the same scale but only plots the Victim power net and shared ground return. The Ground Bounce is larger than the Aggressor net to Victim net coupling.

Advanced 3D EM simulation tools like PIPro enable this analysis by incorporating a reference ground plane and allowing voltage ripple to be evaluated at arbitrary points within the design. When combined with dynamic load modeling, these simulations reveal that ground bounce can vary significantly across the PCB, depending on current distribution and return path geometry. Ground bounce is often found to be the dominant contributor to noise on the victim net, exceeding the effects of direct crosstalk.

Understanding the relative contributions of these mechanisms allows designers to apply targeted solutions, such as improving return path geometry to reduce high current densities under sensitive circuits. This distinction is particularly important in high-current systems, where shared ground impedance can dominate overall noise behavior.

EM Visualization and Insight

Beyond numerical results, electromagnetic (EM) simulation provides valuable visual insight into how currents and fields propagate through the power delivery network. These visualizations help engineers better understand complex spatial interactions that are difficult to interpret from waveforms measured at a single point, enabling more informed design decisions.

3D EM simulation enables:

- Current density visualization
- Identification of coupling hotspots
- Optimization of layout and decoupling capacitor placement

Ground current distribution analysis reveals:

- Non-uniform voltage across the ground plane
- Location-dependent ground bounce

In the case of the location-dependent ground bounce the current density field plot provides a clear picture of how the ground net is not uniform. Sensing the voltage ripple at three separate locations on the same ground net will result in three different results. The variation in voltage is caused by the high dynamic current densities flowing to the main power rail of a BGA package as shown in the figure below.

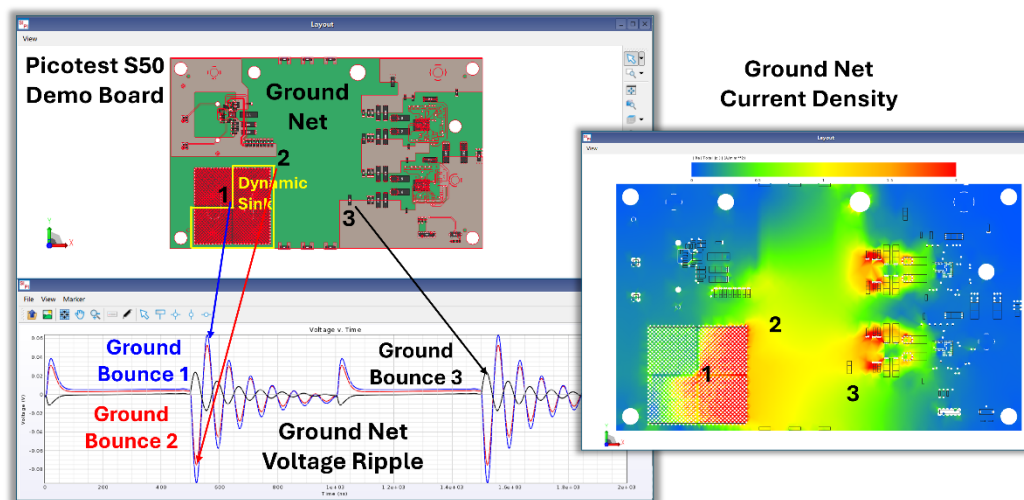


Figure 3. The Picotest S50 Crosstalk Demo Board has a shared ground net between a high current BGA core power rail and a victim low current power rail. The plot on the left shows the ground bounce voltage ripple at 3 separate locations on the shared ground net. The field plot on the right shows the spatial variation of the current density that is causing the voltage ripple to vary across the ground net.

Simulation to Measurement Validation

Measurement results align with simulation predictions, highlighting several key phenomena in high-current PDNs. Under high transient load conditions even small parasitic impedances in the micro-ohms can lead to significant power rail voltage ripple. Aggressor power rails can easily couple to adjacent power or signal nets through net-to-net crosstalk and shared return path ground bounce. Determining worst case peak-to-peak noise ripple requires end-to-end digital twin simulations to capture the non-linearity of the switching regulators. Simple step load responses no longer tell the story, rather forced response periodic excitation provides a more realistic correlation with measurement. The figure below shows how the digital twin simulation is able to predict the non-linear variation in peak-to-peak voltage ripple for the same 160 Amp load dump happening at different times relative to the switching phases of the multiphase VRM's. This same variation is seen in measurement when triggering off the edge of multiple 160 Amp load dumps and overlaying the results.

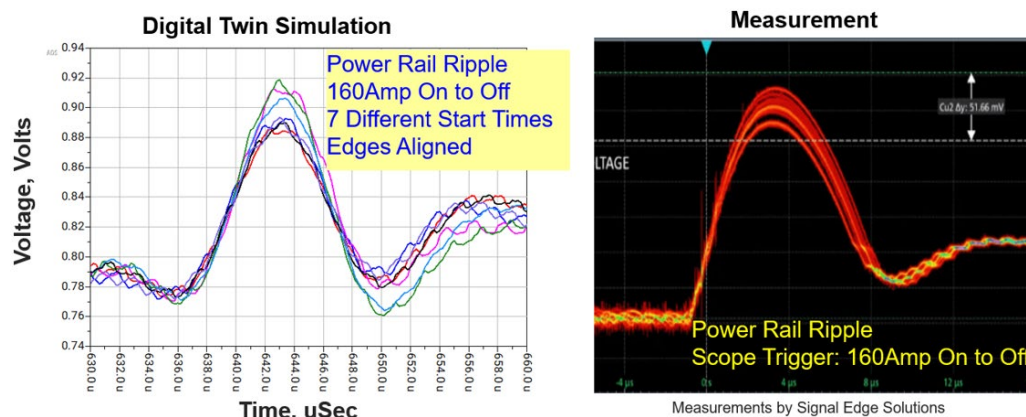


Figure 4. The digital twin power integrity simulation with high current multi-phase VRMs plus PCB PDN EM model plus dynamic periodic switching load runs quickly in Harmonic Balance. This allows the 160 Amp switching load to be simulated with seven different start times relative to the VRM phases to predict large signal switching noise and correlate well with measurement. Simulation and measurement agree that the peak-to-peak voltage ripple for a 160 Amp load dump varies depending on when the load dump happens.

These experimental observations serve to validate the accuracy of harmonic balance simulations, confirming their ability to capture steady-state dynamic behaviors under complex loading. Moreover, the results underscore the importance of modeling large-signal behavior, as traditional linear assumptions would fail to predict the intricate voltage ripple and coupling effects observed in practice.

Automation in Simulation Workflows

Resources are never unlimited, often forcing power integrity engineers to settle for limited target impedance simulations with no time for building a digital twin. Modern analysis of a power delivery network often involves complex, multi-step simulation processes. Manual setup for each scenario is time-consuming and prone to human error. Automation in simulation workflows is the key to addressing these challenges by streamlining repetitive tasks and enabling more efficient exploration of design variations. Keysight's ADS with PIPro integrates EM simulation into the classic circuit simulator environment to deliver the automation needed for power delivery digital twin simulations.

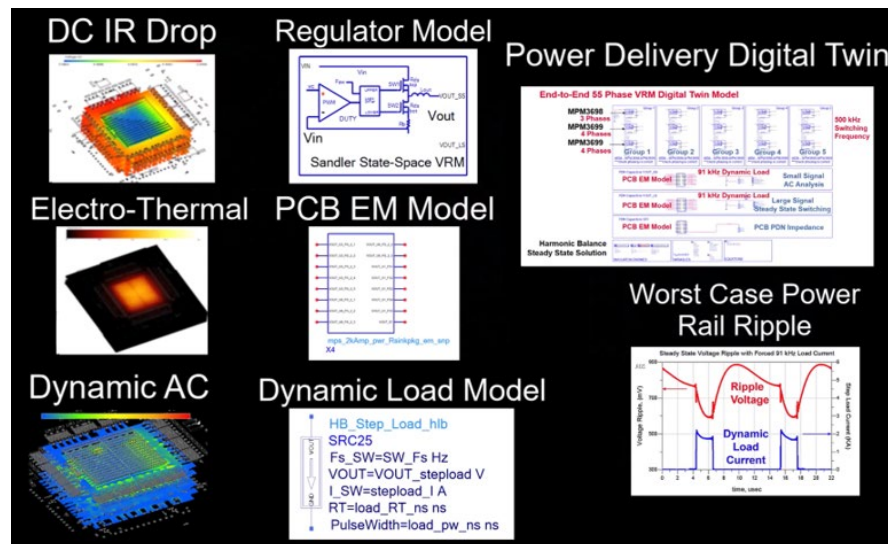


Figure 5. Keysight's ADS with PIPro provides an integrated engineering environment that brings together EM analysis with traditional circuit simulators to enable an elevated level of automation and reuse for design spins and enables the creation of power delivery digital twins to drive better simulation to measurement correlation.

Keysight's PIPro EM simulator significantly reduces complexity by:

- **Reusing DC simulation setups for DC Electrothermal, AC Impedance with Capacitor Optimization, Power Plane Resonances, Conducted EMI, and Dynamic Sink analysis** – leveraging fast DC simulations to verify setups and then simply copying to other analyses with minimal setup remaining.
- **Automatically generating ports and boundary conditions** – ensuring consistent and accurate constraints across multiple simulation runs. Including the addition of reference ground plane for the differential and common mode probing required for analyzing EMI and ground bounce.
- **Generating ready-to-run test benches** – Standard test benches used in the EM simulator for DC IR Drop, PDN impedance, conducted EMI, and dynamic sink crosstalk can all be generated as an ADS schematic with data display to minimize manual efforts and speed up the creation of a high fidelity power delivery network digital twin.

- **Rapid re-use** of model libraries, PCB stack-ups, EM setups, and test benches for re-imported PCB design spins. Faster simulation design spins avoid costly hardware re-spins with right the first-time designs.
- **Export to Python Scripts** – Reuse of simulation setups and easy access for AI/ML automation. All ADS schematics, layouts, and data displays can be exported to Python scripts and the same for PIPro, all analyses can be exported to a Python script for further processing and automation.

Benefits include:

- **Faster design iterations** – enabling quicker evaluation of multiple design alternatives.
- **Reduced setup errors** – decreasing the likelihood of mistakes that can invalidate results.
- **Improved consistency between simulation and measurement** – increasing confidence that simulated performance reflects real-world behavior.

Design Implications

Mitigation of power integrity noise issues that reduce operating margins should start with simulation. The increasing demands on high current low voltage Power Delivery Networks (PDNs) require careful attention to both static and dynamic behavior. Designers must consider not only the nominal impedance targets but also the spatial and temporal variations introduced by distributed parasitics and high-speed switching. Ignoring these factors can lead to excessive voltage ripple, crosstalk, and ground bounce that can directly compromise the signal integrity of a system's data transmission.

Modern PDN design must account for:

- **Ultra-low target impedance requirements** – ensuring stable voltage delivery even under extreme transient currents.
- **Distributed parasitic effects** – including inductance and resistance from traces, planes, and vias that influence high-frequency performance.
- **Interaction between power, ground, and signal nets** – mitigating crosstalk and ground bounce to prevent unintended coupling that can degrade overall system behavior.

Key strategies include:

- **Minimize loop inductance** – reducing the path for high-frequency currents to decrease voltage fluctuations.
- **Optimize decoupling capacitor placement** – placing capacitors close to load points to improve transient response.
- **Use EM simulation early in design** – identifying potential issues before costly prototype iterations.
- **Validate models with measurement** – ensuring simulation accuracy by correlating predicted and observed behavior in real hardware.

Conclusion

The increasing demands of AI, cloud computing, and advanced semiconductor architectures are driving power delivery systems into regimes where traditional design methods are no longer sufficient. Conducted EMI, crosstalk, and ground bounce are no longer secondary effects but primary design constraints for dynamic power delivery.

Accurate prediction and mitigation require:

- Full 3D EM simulation of the PCB PDN
- End-to-end VRM + PCB PDN + Dynamic Load digital twin modeling
- Harmonic balance analysis for steady state transient nonlinear behavior
- Careful separation of crosstalk and ground bounce noise sources

By integrating these techniques into the design process, engineers can significantly reduce the risk of late-stage failures, improve system reliability, and meet stringent design requirements. All these capabilities are integrated into Keysight's ADS circuit simulation environment with the PIPRO EM simulator.

To learn more, visit <https://www.keysight.com/us/en/product/W3623B/pathwave-ads-core-em-design-layout-hsd-ckt-sim-pipro.html>



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