

Predicting RF chip reliability with thermal simulations

■ As electronic content in vehicles continues to rise, designers must find solutions for reliability under intense heat, advises **Daren McClearn**

Heat kills semiconductors and automotive environments are notorious for their extreme heat. Accurately predicting RF chip reliability is complicated and costly for design teams using only traditional methods of physical prototyping and measurements. An underperforming design can trigger board layout changes, selection of different chips, or limited operating specifications.

Estimates and approximations

CMOS transistors follow a classical 'bathtub' failure rate curve illustrated in *Figure 1*. Burn-in screening weeds out infant mortality, but the ultimate killer is wear-out failures, setting a practical limit to the functional life of a device. To better predict wear-out in automotive-qualified processes, foundries often provide aged transistor models. Designers still have to worry about the packaging stack, board-level component spacing, spreading planes, thermal vias, heatsinking and airflow management.

To understand its Ka-band RF transceiver's lifetime, EnSilica was relying on hand calculations using physical design rules and estimates of electron migration, says Alan Wong, the company's senior vice-president of engineering. "Third-party packaging suppliers would help by telling us how hot a die might get when packaged based on their thermal dissipation experience, but it was just an educated guess, and it wasn't detailed enough to guide design decisions."

Visualising hot spots

Instrumenting a transceiver prototype with low-power temperature sensors embedded at points on a die raised questions. Are the sensors in the right spots? Is the chip in the proper operating mode for valid measurements? Test setups and chamber sweeps could take weeks.

EnSilica's RF/analogue tool stack includes Cadence Virtuoso IC, ANSYS HFSS, and Keysight's Advanced Design System (ADS) with RFPro for electromagnetic (EM) simulation. From layout in Cadence Virtuoso IC, a GDSII export enables electro-thermal modelling and simulation in ADS electro-thermal simulator.

A robust thermal model includes material properties, die layout, chip

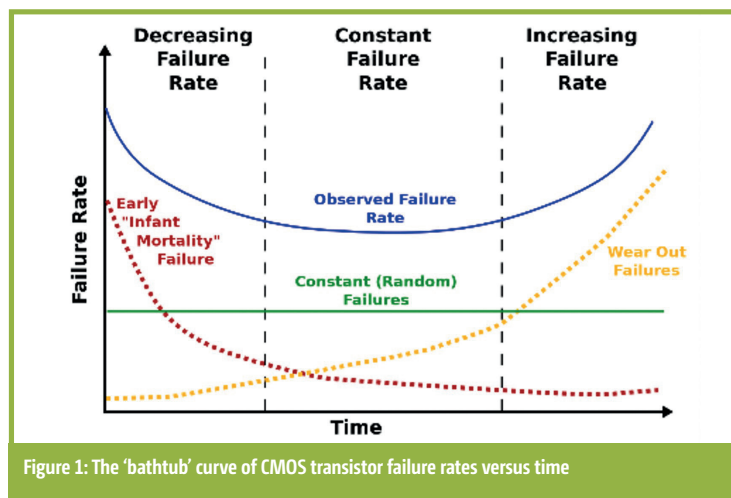


Figure 1: The 'bathtub' curve of CMOS transistor failure rates versus time

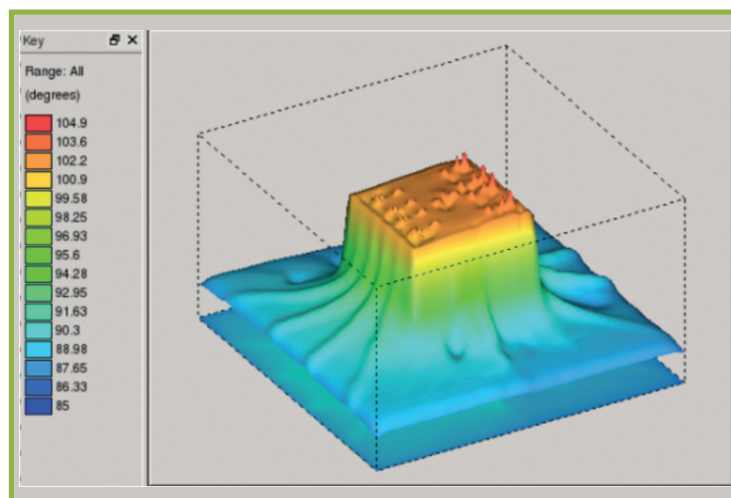


Figure 2: Hot spots revealed in electro-thermal simulation of a Ka-band transceiver, showing boundary heating effect

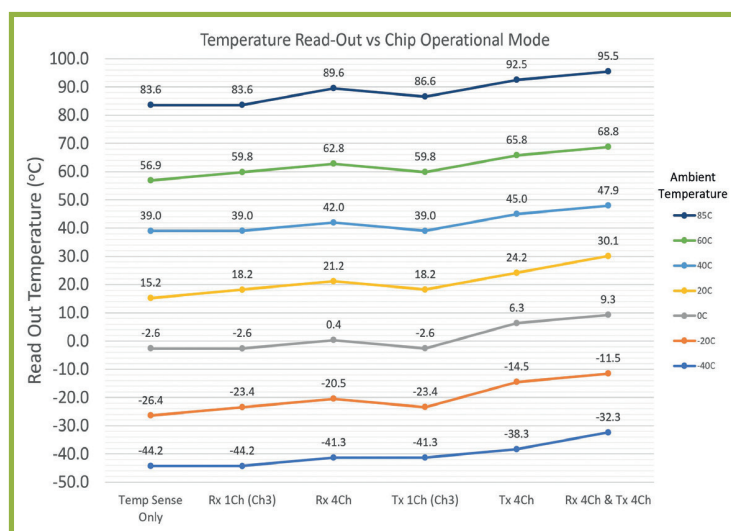


Figure 3: Physical measurements of die temperature fall within predicted results from electro-thermal simulation

package bumping and underfill details, PCB build features and stack files from EM simulation. "We worked very hard to match every aspect of our materials to realistic thermal parameters," says Samuel Wu, principal RFIC design engineer at EnSilica.

Feeding a detailed model into electro-thermal simulation delivers an accurate chip thermal profile (*Figure 2*). An immediate insight: the peaks along the right edge of the chip indicate boundary heating of 3°C influenced by an adjacent RFIC on the PCB.

The real test of the electro-thermal simulation results is a comparison to measurements on the embedded temperature sensors. Simulation predicted a maximum rise of 13°C in die temperature over ambient. Actual measurements under full-on conditions show an increase of 12.3°C (*Figure 3*).

Previously unseen details also emerged. Dark spots on the top of the elevated temperature mesa in *Figure 2* indicate VDD and VSS bumps acting as thermal pathways, cooling small areas. From that insight, chip layout changes and bumping further reduced operating temperatures in the final product.

Cadence RelXpert was used to generate aged power amplifier (PA) models for reliability simulation at a junction temperature of 100°C over 10 years of operation. The power output change between the aged PA and the 'fresh' one was only -0.4dB, indicating little degradation.

"We have greater confidence in two ways," says Wong. "The data points are bang on thermal simulations, and the reliability looks good, with a very benign PA power degradation over time. These were not givens before our virtual thermal analysis."

Accurate EM and thermal simulations help RF component design teams shift from intense physical measurements to virtual space, shortening cycles and improving prototype success. □

About the author

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