CASE STUDY



Design Team Increases Efficiency of High-Speed Digital Boards by 100%

KEYSIGHT

PATHWAVE

Organization

- Inspur Power Commercial Systems (IPS)

Challenges

- Design accurate high-speed digital PCBs for stable, reliable server and storage products

Solutions

- PathWave Advanced Design System (ADS)

Results

- Increased efficiency of high-speed digital PCBs by 100%
- Decreased design and simulation time from days to minutes for each design case

High-speed digital (HSD) standards are quickly evolving in high-speed computing and data center connectivity applications. Faster networking speeds require faster memory and serial bus communications. As an example, Peripheral Component Interconnect Express (PCIe®) expansion bus speeds are evolving from PCIe 4.0 to PCIe 5.0 to support these increased speeds. The same is true for memory, as double data rate (DDR) memory evolves from DDR 4.0 to DDR 5.0. Increasing speeds of serial data communications require changes to the design methodology.

Designers of HSD printed circuit boards (PCBs) are incorporating new tools and processes to accurately characterize loss and coupling of high-speed channels. However, companies must find ways to incorporate these new tools and processes without increasing their design and verification time. Inspur Power Commercial Systems (IPS), a leading data center and cloud computing solutions provider, found that Keysight's PathWave Advanced Design System (ADS) contained all the tools and processes it needed to design stable, reliable high-speed digital PCBs.

New Standards Bring Faster Speeds and More Factors to Consider

IPS and many other high-speed digital design teams are looking for a new design methodology that handles the complexity that faster speeds bring. One factor to consider is the need to design controlled impedance transmission lines, including modeling via effects to avoid interface failure. Integrated circuit (IC) instability is increasing due to signaling noise in ground and power planes. Designers are using new sophisticated algorithms to improve signaling interfaces for HSD designs. Even so, it is difficult to compensate for die, package, and PCB parasitics.

The new design methodology also needs high-accuracy electromagnetic (EM) simulation to accurately characterize loss and coupling of high-speed channels. Simulation techniques must be more intelligent by segmenting domains and using the strengths of multiple EM technologies to scale simulations without sacrificing accuracy. As data rates increase, a significant dilemma is the choice of which EM technology to use.

> "High-speed digital PCB design is another world compared to traditional PCB design. Traditional design methodology focuses on selecting the right components, placing them on the layout, and wiring everything up with traces, etc. However, with high-speed digital PCB design, you have so much more complexity. You must think about signal integrity, crosstalk, reflections, and more."
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> **Ye Fenghua, Product R&D Department Manager, Inspur Power Commercial Systems**

Signal and Power Integrity Analysis Are Critical to Accurate Designs

The limiting factor of 3D EM technology for signal integrity analysis is the scale and complexity of PCB designs. Signal integrity engineers need high-accuracy EM simulation to catch signal interference before prototyping. Signal integrity analysis is critical to accurate designs, even though it can require additional hours of engineering time.

Power integrity is also becoming an ever-increasing challenge in modern high-speed systems, driven by two main forces: higher device integration with lower IC supply voltages, and shrinkage of the PCB for small form factors. Because of this, a true power integrity direct current simulator is a requirement to consider the real physical layout of the power delivery network, together with inputs for materials, like plating thickness for vias.

Given the benefits of signal and power integrity analysis, IPS's design team knew it needed a design and simulation software tool specifically for HSD design. They looked for a software tool to meet all of the following design goals:

- Accurate and time-efficient performance evaluation — up to 10-15 bit error rate (BER)
- Compatibility with varied models from different vendors
- Fast sweep of IBIS-AMI model parameters
- Flexible data processing



A Single Software Tool for HSD Design

IPS selected PathWave ADS for its HSD simulation software tool. The PathWave ADS channel simulator contains bit-by-bit and statistical modes including support for the IBIS-AMI flow, which helps engineers evaluate ultralow BER performance in HSD boards and interfaces. PathWave ADS supports many IBIS-AMI models from a variety of vendors (Figure 1). The channel simulator contains eye probe components that deliver eye diagram analysis, including BER contour and bathtub display, allowing for IPS to meet its performance evaluation goals (Figure 2). PathWave ADS also provides various controllers for system analysis including batch, optimization, Design of Experiment (DOE), and statistical controllers. The system analysis helped IPS's design team use a systematic approach to an optimal and robust design. This analysis led to an efficiency increase in their high-speed PCBs of 100%, and in turn, more stable and reliable server and storage products for their customers.

IPS also used two integrated EM analysis solutions in PathWave ADS, SIPro, and PIPro, which specifically overcome signal and power integrity challenges. SIPro provided signal integrity analysis, enabling IPS's design team to characterize loss and coupling of signal nets. The team extracted an EM-accurate model from SIPro and used it in the PathWave ADS channel simulator. PIPro provided power integrity analysis of their power distribution network (PDN), including DC IR drop analysis, AC impedance analysis, and power plane resonance analysis.

From the net-driven user interface — a feature common to both SIPro and PIPro — IPS's design team could quickly select only the nets they wanted to simulate. With this workflow, IPS's design team went from layout to results in less than 20 clicks. The benefit of the integrated signal and power integrity analysis is that IPS decreased the design and simulation time from days to minutes for each design case. As a result, IPS is now using the PathWave ADS workflow for all of its HSD designs.

PathWave ADS puts power in the hands of the IPS designers, allowing them to perform the signal and power integrity analysis themselves. PathWave ADS not only decreased their design and simulation time, but also allowed them to explore design parameters leading to increased board efficiency.

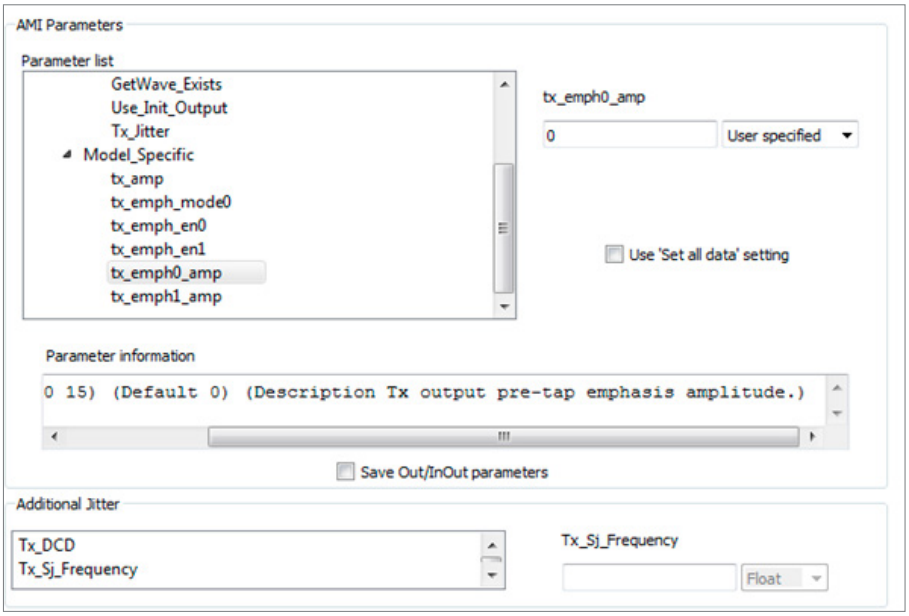


Figure 1. Example of vendor-provided IBIS-AMI model

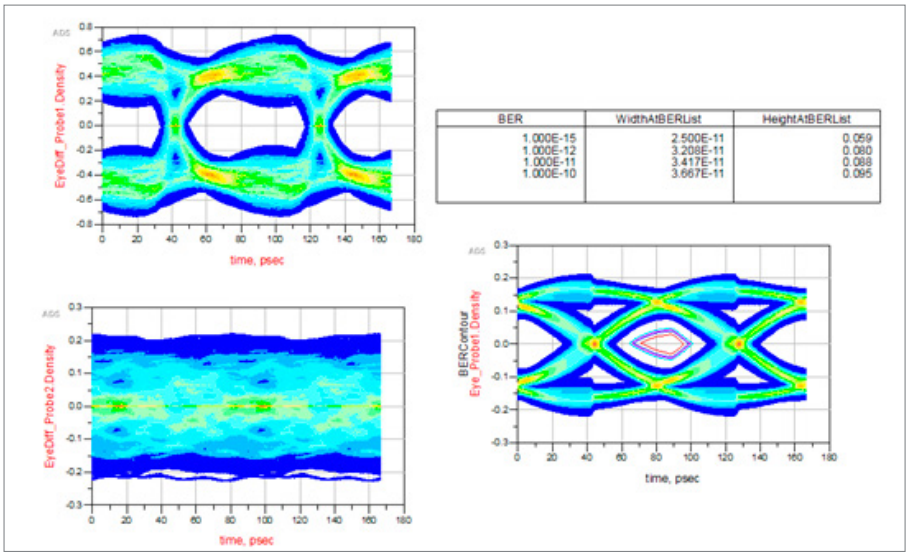


Figure 2. Time-domain analysis via eye diagrams is necessary to ensure signal integrity of HSD channels

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