CASE STUDY

PathWave ADS Memory Designer Turbocharges Design Exploration for Broadcom APD

KEYSIGHT

PATHWAVE

Efficient Simulation with Better User Experience

Organization

- Broadcom

Challenges

- Simulation efficiency
- Ease of use
- Next generation DDR transceiver design
- Signal integrity
- Channel exploration & characterization
- Equalizer options & parameter optimization

Solutions

- PathWave Advanced Design System (ADS) Memory Designer
- Design exploration
- Parameter sweeps with transceiver, channel, and signal properties

Results

- Pre-layout and silicon DDR interface design space exploration performed in a fraction of the time
- Superior user experience

Double Data Rate (DDR) Dynamic Random Access Memory (DRAM) and similar high-speed interfaces are commonly at the heart of consumer, data center and industrial devices. For each new device generation, engineers need to explore transceiver and layout design parameters to find the best solutions for signal integrity and reliability. Among these parameters are layout topology and termination, driver settings, channel encoding and equalization.

When designing new products that must perform and meet the physical requirements of customers (size, shape, EMC compliance etc.), how can you quickly and more efficiently explore the options before engineering costs exceed the project's value? How can engineers avoid dead-ends in the design cycle? The answer lies in design exploration, a key motive for simulation.

Companies have spent decades developing great engineering experience that enables specialists on staff to more quickly decide which design variations to explore. At Broadcom, there is such a global community of signal and power integrity (SI/PI) engineers across a diverse set of business groups.

One of Broadcom's SI/PI engineers is Jim Antonellis, a member of the Application Specific Integrated Circuit (ASIC) Products Division (APD). APD were seeking a superior path to perform design explorations for cutting-edge semiconductor and PCB layout design. For this, they turned to Keysight PathWave ADS with Memory Designer. Memory Designer enabled a dramatic improvement in effectively exploring all the design options for cutting-edge DDR interfaces – in silicon, package, and PCB layout.

Challenge: Accelerate design exploration

Broadcom APD excels in custom ASIC design. What sets them apart is their skill for designing for any market segment as a service to their customers. APD designs typically require high speed interfaces including DDR4/5, LPDDR4/5, HBM2/3 and newer memory interfaces, and other high-speed device interconnects. The team's specialized SI/PI engineers need to explore as many design variables as quickly as possible.

> "It had to be easy to use, enough to be able to jump in and jump out without using it every day, but not have to re-learn every time."
>
> **Jim Antonellis**

APD signal and power integrity engineers were using industry-standard tools to simulate and characterize models for silicon (TX/RX and equalization), channel (PCB, interposer, package) and device configurations (termination, drive strengths and more). However, they wanted to improve efficiency and find answers to broader scenarios more readily.

They desired to replace a cumbersome point-tool approach with a software solution that enables all exploration in one environment with a better user experience.

> "We needed a tool with libraries of pre-designed models that were flexible and would allow extensive parameter sweeping from PCB to silicon."
>
> **Jim Antonellis**

A frequent issue with the traditional SPICE based approach is that results are idealized, not at all close to real-world manufacturable silicon or PCB substrate. To get accurate results with SPICE, engineers must predict and include complex parasitic elements, stochastic signal models, and injected noise and distortion that more closely represent the real-world circuitry, a time consuming and error prone process. The ability to easily push into a block and define it to a physical level is required, but not at the expense of ease of use. Accurately defining the constituent blocks and analysis needs to be simple and accessible under one GUI.

Antonellis, Senior Signal Integrity/Power Integrity engineer for APD, set out to evaluate several products to see which best met their needs.

The criteria were:

- It had to be easy to use without compromising capabilities.
- It had to have a block diagram/schematic-based UI.
- It had to include an extensive set of modeling features such as:
  - Understand DDR signal types and timing assumptions, PRBS generation, NRZ & PAM, Equalization (DFE, CTLE, FFE) etc.
  - Transmission Line Solver with physical parameter support for sweeping.
- Not only could model parameters be set, but it had to easily support sweeping of parameters.
- Displaying and interacting with results was critical. Specifically, it had to produce accurate statistical eye diagrams and charts with markup.
- Accessibility to pre- and post-simulation data within other tools (i.e., CSV import and export to spreadsheets, etc.)
- The solution had to provide answers not just for one project, but for any high-speed signal or power integrity challenges from the endless array of designs they must produce.
- Speed of simulation, accuracy of results, and overall efficiency had to be high.

Solution: Easy block-based design

APD selected PathWave ADS with Memory Designer. Memory Designer stood out not only for its ease of use, but also because of the wide scope of building blocks (PCB to Silicon) and extensive parameter sweeping. It enabled APD to meet current and future needs more completely than any other solution.

Using Memory Designer's block-based design setup shown in Figure 1, APD was able to rapidly begin simulations with different settings using DDR4, DDR5, LPDDR4, LPDDR5, GDDR6, HBM2, and HBM3.

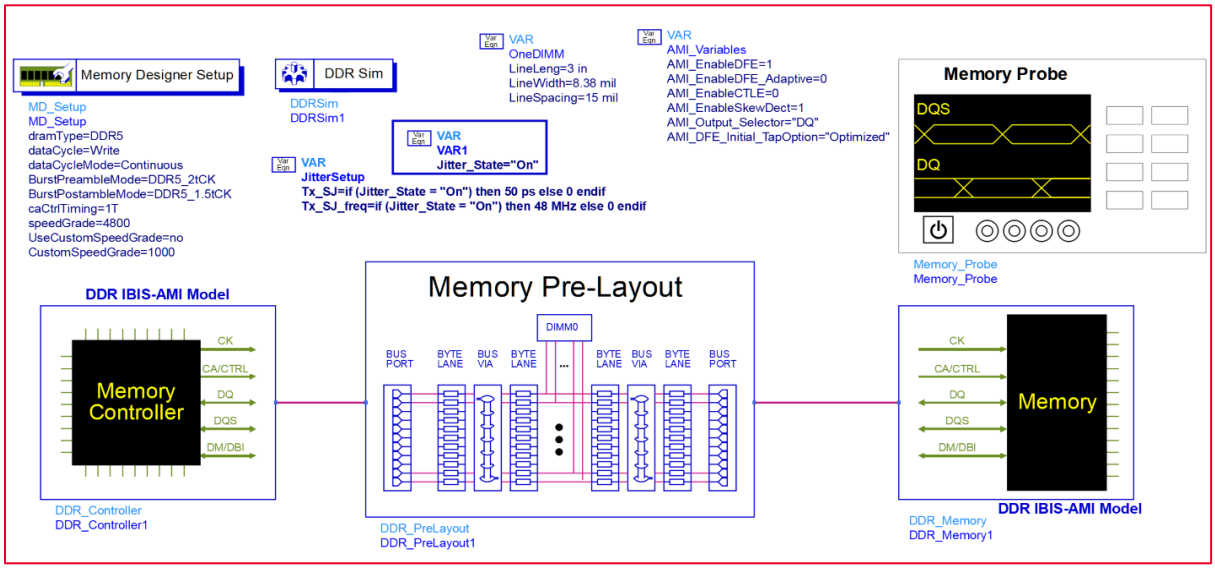


Figure 1. PathWave Memory Designer uses intuitive blocks

The primary figure of merit for the SI/PI engineer is the eye diagram seen in Figure 2. The idea is to explore different equalization types as well as different pre-layout interconnect schemes to best determine DDR interface design parameters as well as what would be recommended for Tx/Rx I/O cells and PCB/package layout for best results in the product design.

Using the Memory Pre-Layout Block, APD engineers were able to rapidly configure and simulate parameter sweeps for PCB trace impedances, impedance discontinuities and topology. For the evaluation, they concentrated on the TLINP transmission line model as it gave accurate results with the parameters they needed for variations.

APD conducted trials of different topology schemes including tee, tree/branch, and fly-by as well as point to point. These are the PCB layout topologies most frequently used with DDR in consumer and industrial designs, and lead to very difficult trade-offs. For example, when splitting a transmission line from one memory controller's transmitter to multiple DRAM receivers, each branch forms an impedance change. This could be accommodated using impedance transformers but comes at the cost of larger trace widths and insertion loss towards the DRAM receiver. By constructing these scenarios in Memory Designer, APD can easily find the optimal trade-offs between SI (insertion loss, eye closure), PCB routing density, and transceiver driver strength or power consumption.

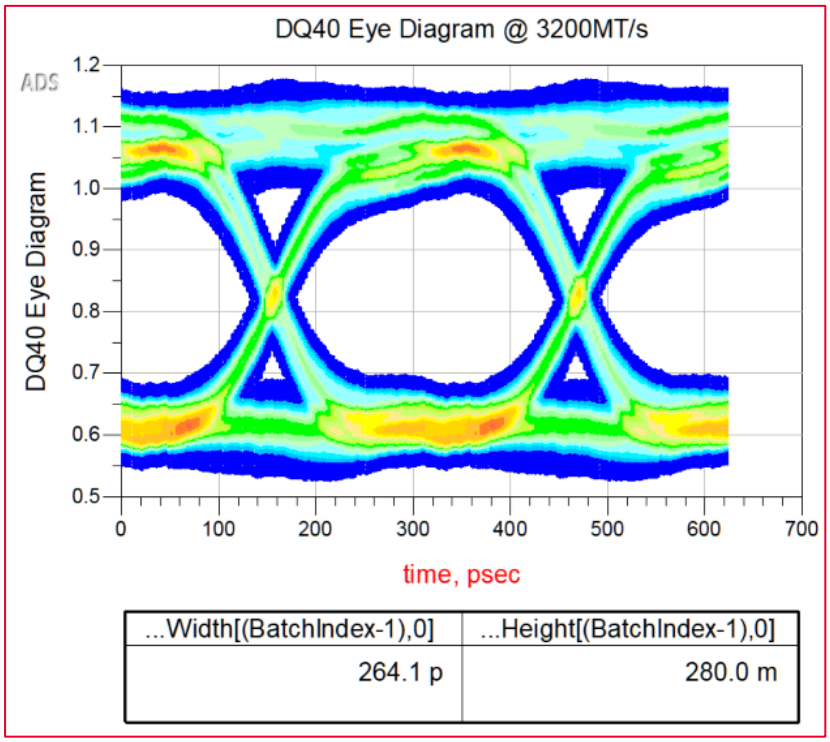
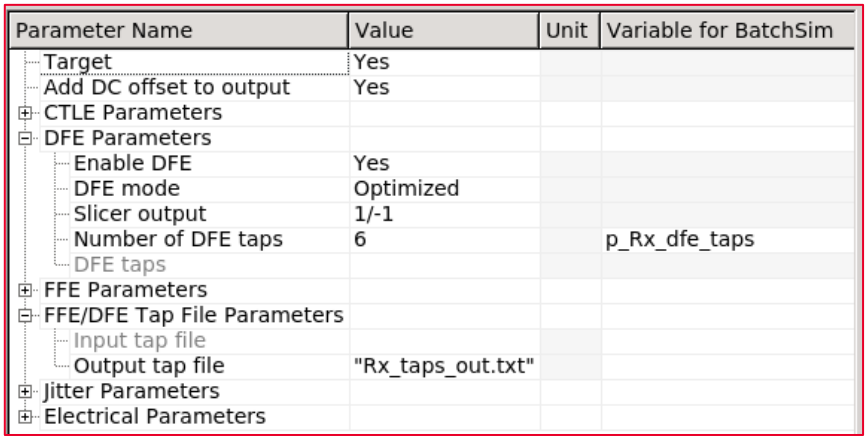


Figure 2. Eye diagram and pass/fail metrics from a Memory Designer simulation with DDR4 at 3200MTs/s

> “It provided a very convenient palette of blocks, and when you push into the blocks, you have the ability to define anything, like your equalizer type and parameters or number of taps, and your driver type. It is all pretty easy to use.”
>
> **Jim Antonellis**

Transceiver models had to support the latest channel equalization. APD were especially looking to mitigate Inter-Symbol Interference (ISI), jitter, and other distortion and noise sources for DDR. To perform these tests in Memory Designer, they used IBIS-AMI transceiver models and ran parameter sweeps with varied Decision Feedback Equalization (DFE) taps on receivers, and Feed-Forward Error correction (FFE) or Continuous-Time Linear Equalization (CTLE) transfer functions on transmitters show in Figure 3.



Parameter Name	Value	Unit	Variable for BatchSim
Target	Yes		
Add DC offset to output	Yes		
⊞ CTLE Parameters			
⊟ DFE Parameters			
Enable DFE	Yes		
DFE mode	Optimized		
Slicer output	1/-1		
Number of DFE taps	6		p_Rx_dfe_taps
DFE taps			
⊞ FFE Parameters			
⊟ FFE/DFE Tap File Parameters			
Input tap file			
Output tap file	"Rx_taps_out.txt"		
⊞ Jitter Parameters			
⊞ Electrical Parameters			

Figure 3. DFE parameters for sweeping in DDR receiver

> “Case in point: if there's enough length in your ISI you have to add more DFE taps. Having that behavioral equalization was very important.”
>
> **Jim Antonellis**

Results: Rapid optimization and data post-processing

The ability to perform parameter sweeps and create meaningful eye diagrams allowed Broadcom APD engineers to discover optimal solutions faster than ever.

In the example shown in Figure 4, the number of DFE taps in a DDR5 receiver was swept to find the minimum number of taps to “open the eye” yet minimize silicon area and power on the specified PCB substrate and DDR interconnect topology.

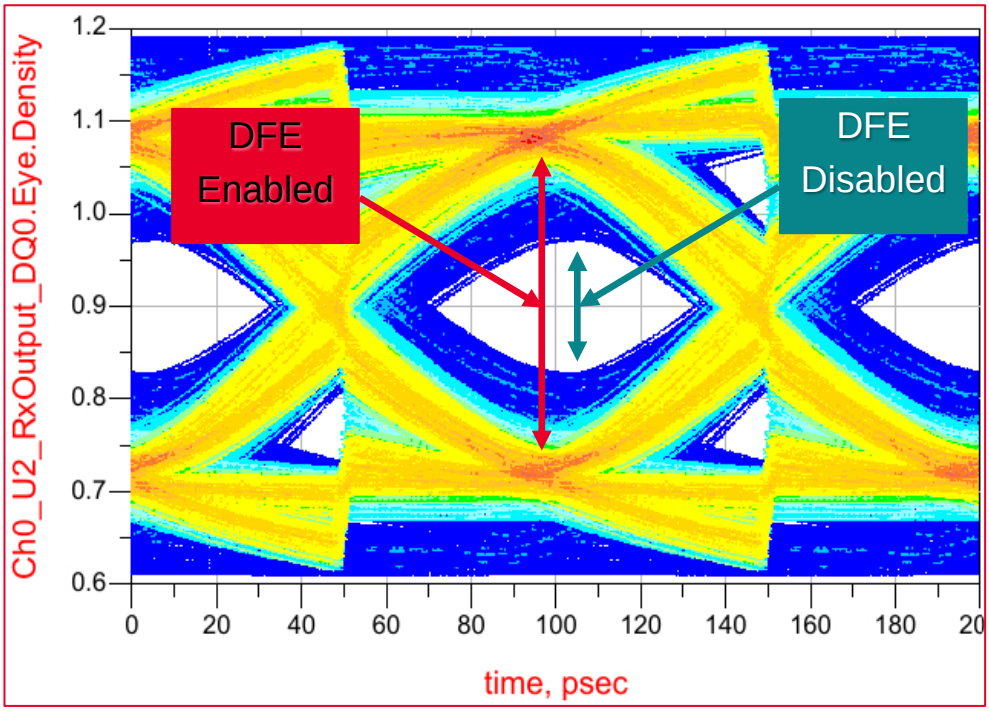


Figure 4. Results of DFE taps parameter sweep

Figure 5 shows the result of DFE tap sweep simulation in a typical oscillogram with a section of the PRBS (Pseudo-Random Bit Sequence) repeated with each DFE tap setting. This clearly indicates the positive effect of the correct number of DFE taps on the signal quality through the interconnect channel. Accurate channel models for the PCB and connectors, as well as the transceivers (including S-parameters, IBIS-AMI and others) are available to obtain results that correlate exceptionally with real world devices.

Without the benefit of using High Performance Compute (Cloud) add-ons, Memory Designer produced results from setups with complex parameter sweeps in a fraction of the time required in other EDA tools (not to mention the time saved in setup and convenience of setup in one GUI). Table 1 shows execution times from a DDR5 simulation involving 3 nodes (1 driver, 2 receivers), each with 3 termination settings, across 8-bits of data input/output signals. Even with 72 total permutations to generate all the eye diagrams and pass/fail metrics, the full set was completed in 12.5 minutes on a single desktop computer.

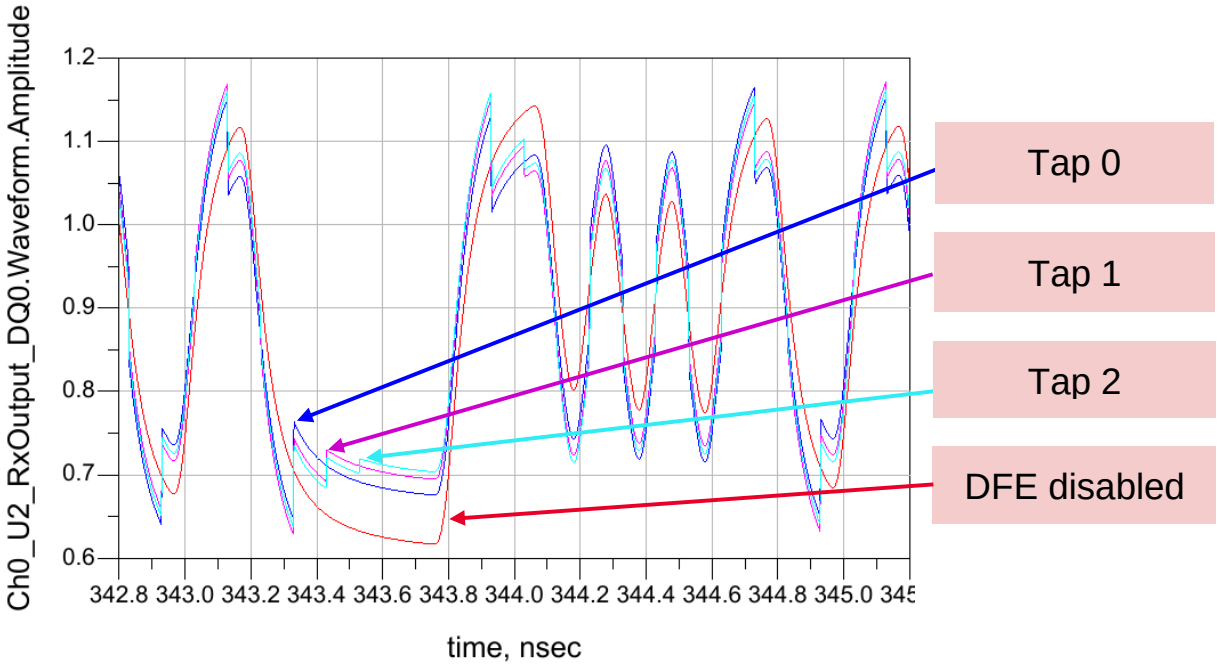
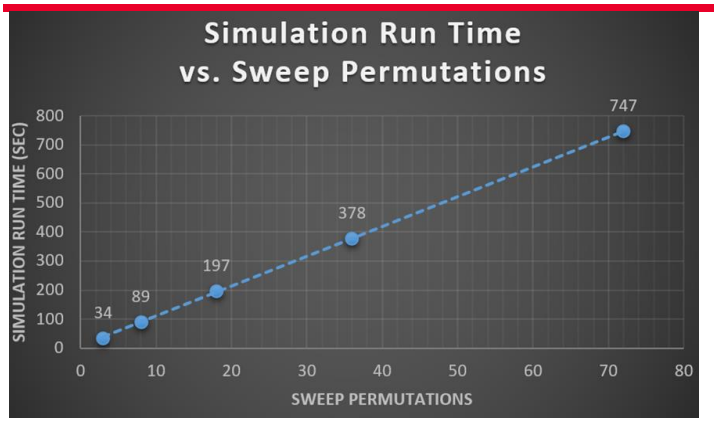


Figure 5. DFE tap sweeps in action

Table 1. Simulation times versus sweep permutations for TX drive strength

No. sweeps	Simulation time (Seconds)	Simulation time (Minutes)
3	34	0.5
8	89	1.5
18	197	3.3
36	378	6.3
72	747	12.5



A key configuration block used in memory simulation setups is the Memory Probe shown in Figure 6. APD used the built-in configurations of the Memory Probe to enable results from simulations to be captured in visual forms typically required (eye diagrams, waveforms, histograms etc.) but also to export and format data for further analysis on the engineer's desktop.

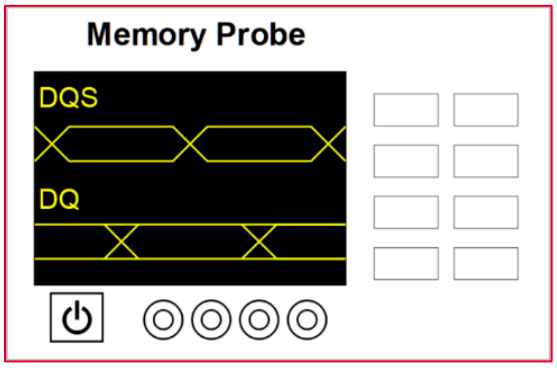


Figure 6. The Memory Probe block

The parameter sweeps were exported to CSV for easy analysis. Figure 7 demonstrates how quick and easy it was to find the best overall on-die termination settings by searching for the highest value for eye opening in the list.

Sweep Index	Sweep Setting	SDRAM Signal and Ref Des	Measurement	Value (V)	Pass Fail
1	pTxZ=25.0	Ch0_U2_DQ0	Eye Height	***0.464***	Pass
1	pTxZ=25.0	Ch0_U2_DQ1	Eye Height	0.461	Pass
1	pTxZ=25.0	Ch0_U2_DQ2	Eye Height	0.462	Pass
1	pTxZ=25.0	Ch0_U2_DQ3	Eye Height	0.462	Pass
1	pTxZ=25.0	Ch0_U3_DQ0	Eye Height	***0.464***	Pass
1	pTxZ=25.0	Ch0_U3_DQ1	Eye Height	0.461	Pass
1	pTxZ=25.0	Ch0_U3_DQ2	Eye Height	0.462	Pass
1	pTxZ=25.0	Ch0_U3_DQ3	Eye Height	0.462	Pass
2	pTxZ=50.0	Ch0_U2_DQ0	Eye Height	0.396	Pass
2	pTxZ=50.0	Ch0_U2_DQ1	Eye Height	0.395	Pass
2	pTxZ=50.0	Ch0_U2_DQ2	Eye Height	0.395	Pass
2	pTxZ=50.0	Ch0_U2_DQ3	Eye Height	0.395	Pass
2	pTxZ=50.0	Ch0_U3_DQ0	Eye Height	0.396	Pass
2	pTxZ=50.0	Ch0_U3_DQ1	Eye Height	0.395	Pass
2	pTxZ=50.0	Ch0_U3_DQ2	Eye Height	0.395	Pass
2	pTxZ=50.0	Ch0_U3_DQ3	Eye Height	0.395	Pass
3	pTxZ=75.0	Ch0_U2_DQ0	Eye Height	0.296	Pass
3	pTxZ=75.0	Ch0_U2_DQ1	Eye Height	***0.294***	Pass
3	pTxZ=75.0	Ch0_U2_DQ2	Eye Height	0.295	Pass
3	pTxZ=75.0	Ch0_U2_DQ3	Eye Height	0.295	Pass
3	pTxZ=75.0	Ch0_U3_DQ0	Eye Height	0.296	Pass
3	pTxZ=75.0	Ch0_U3_DQ1	Eye Height	***0.294***	Pass
3	pTxZ=75.0	Ch0_U3_DQ2	Eye Height	0.295	Pass
3	pTxZ=75.0	Ch0_U3_DQ3	Eye Height	0.295	Pass
			MIN:	***0.294***	
			MAX:	***0.464***	

Figure 7. Post-processing of results in a spreadsheet

> “Previously I did not have this complete, fast, easy to use environment. I would have to cobble up a lot more things across several EDA tools. And you know, that's easily a 10X order of time savings.”
>
> **Jim Antonellis**

Next steps

The APD team is currently using Memory Designer to accelerate projects that require high speed signaling, especially DDR4/5 and newer. They are leveraging the design exploration capabilities and rapid simulation setup enabled by the library of models.

Next steps to deeper analysis include:

- Adding more to the interconnect model, including PCB and package vias, and sweep parameters around via dimensions to find optimal manufacturable solutions.
- “Closing the Loop” – bring full PCB design data back into ADS for 3D electromagnetic parameter extraction of the channel and re-simulate using channel hardware design data.
- Exploring the possibilities of adding asymmetric driver settings with different drive strengths and pull-up and pull-down resistance values.
- Learning more about the power aware features of Memory Designer and implementing power integrity simulation.
- Exploring Pass/Fail metrics around input and output voltage and current specifications for logic interfaces.

Conclusion

Broadcom chose Memory Designer because it was the only solution available that “checked all the boxes.” APD adopted the Keysight memory simulation tool to achieve their primary goal of behavioral characterization of high-speed DDR interfaces and are using the results to accurately guide ASIC and interconnect product design.

They found the Memory Designer solution is easy to use, supports parameter sweeping across multiple nets with multiple parameters, and has a comprehensive set of models that can be customized to reflect the design. It provides SI/PI-engineer-friendly graphical reporting and exports results for further post-processing and analysis.

> “Of all the requirements we had, PathWave ADS with Memory Designer checked all those boxes and no one else did. It was that simple to me.”
>
> **Jim Antonellis**

Learn more about Broadcom at www.broadcom.com

For more information on these Keysight EDA solutions, please visit:

PathWave Advanced Design System (ADS)

PathWave ADS Memory Designer

Keysight enables innovators to push the boundaries of engineering by quickly solving design, emulation, and test challenges to create the best product experiences. Start your innovation journey at www.keysight.com.

KEYSIGHT

This information is subject to change without notice. © Keysight Technologies, 2023, Published in USA, September 20, 2023, 3123-1571.EN