

Predicting Ka-band Transceiver Thermal Margins, Wear, and Lifespan

Electro-thermal simulations enhance the electro-magnetic analysis capability in a multi-vendor RF EDA workflow

Thermal Analysis Crucial for “First-Time Right”

Organization

- EnSilica

Challenges

- Predicting RF chip reliability in harsh automotive settings with more confidence than estimates provide
- Design cycles slowed by time-consuming physical lab thermal test setups
- Integrate electro-thermal simulation into existing RF EDA workflow

Solutions

- Shift thermal analysis into virtual space with minimal extra steps by adding PathWave ADS Electro-Thermal Simulator, extending electro-magnetic simulation capability
- Enhance thermal models with chip packaging info, PCB layout and materials, and more

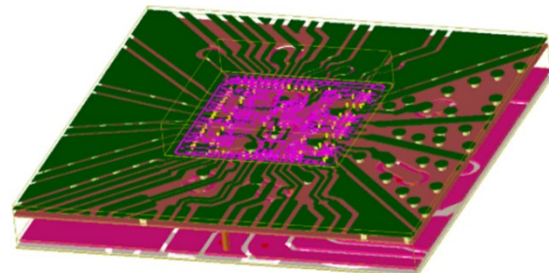
Results

- Less than 0.7°C difference between thermal simulation and measurements
- Chip layout and bumping changes improved thermal margins
- High-confidence 10-yr reliability prediction

EnSilica, Ltd., based in Abingdon, UK, is a fabless chipmaker creating custom ASICs for OEMs and system integrators and providing IC design services for companies with in-house design teams. EnSilica’s world-class expertise in RF, mmWave, mixed-signal, and high-speed digital designs helps customers in automotive, communications, industrial, healthcare, and wearable applications.

“First-time right” is EnSilica’s demanding standard for chips when frequencies and complexity rise. EnSilica has an RF/analog team of about 25 engineers based in the UK and about 130 engineers in total across offices worldwide. Their RF experience includes designs up to 40 GHz and foundry relationships for reliable processes. Domain-specific knowledge and accelerated time to market achieved through design reuse are two more reasons customers turn to EnSilica.

One use case for EnSilica’s Ka-band (26.5-40 GHz) transceivers is vehicle-mounted low-earth orbit (LEO) satellite terminals, where harsh temperatures can wear parts out faster than expected. Assessing the thermal performance of these transceivers using Keysight PathWave Advanced Design System (ADS), PathWave RFPro, and PathWave ADS Electro-Thermal Simulator is vital in understanding their thermal operating margin and lifespan. Simulations reduce time-consuming physical test setups and provide accurate, comprehensive electro-magnetic and electro-thermal analysis with fully coupled effects, in turn enabling reliability predictions with higher confidence.



Challenge: Predicting how long chips can withstand wear

Automotive environments are notorious for being one of the harshest on earth, with broad temperature ranges designers must take into account. Temperatures can span from freezing to boiling when vehicles sit outside. Engine compartments generate concentrated heat, exposing components to even higher temperatures. Sun loading can heat surfaces and passenger compartments to uncomfortable levels. Electronics also self-heat – higher frequencies and transmit power levels drive up readings.

Heat kills semiconductors. CMOS transistors follow a classical “bathtub” curve of failure rates illustrated in Figure 1. Some failures occur immediately, termed infant mortality; operational burn-in screening can weed these out effectively. Robust board-level thermal design practices, like proper component spacing, spreading planes, thermal vias, heatsinking, and airflow management can contain many hotspots.

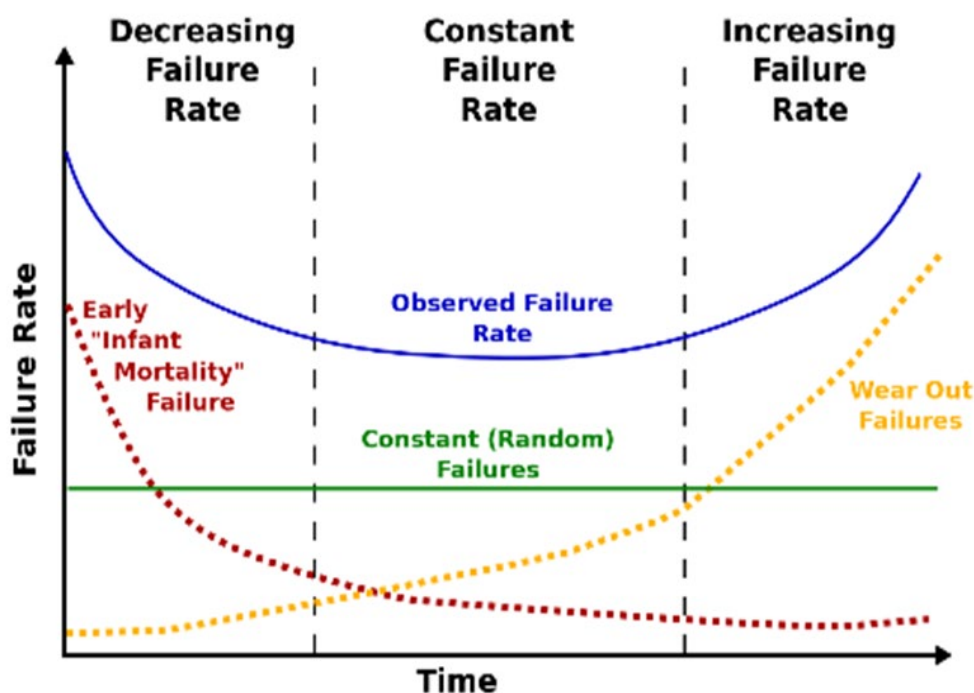


Figure 1. Classical “bathtub” curve of CMOS transistor failure rates versus time

The ultimate killer is wear-out failures, setting a practical limit to the functional life of a device. CMOS transistors age due to hot carrier injection, bias temperature instability, and electron migration. Voltage and junction temperature variations impact these effects. To better predict wear-out, foundries often provide “aged” transistor models in their automotive-qualified processes, which gives a starting point.

In complex designs, context matters. “Knowing where the edge of our chip is and caring about how customers use it is important,” says Alan Wong, Sr. VP of Engineering at EnSilica. “Customers come to us because we have a deeper understanding of system applications and how to make a chip that behaves as expected in a system.” A big part of that understanding comes from thermal analysis.

Traditionally, system vendors have performed cursory thermal simulations, then moved into physical prototypes to test and measure real-world thermal behavior in a lab. Testing can include various accelerated life cycle test (ALT) techniques. If designs underperform expectations, adjustments can be expensive – including changing board layouts, forcing the selection of different chips, or limiting operating specifications, leading to missed market windows and lost sales.

To help its customers, EnSilica decided to take on more thermal characterization of its parts. But it would not be easy. “We were relying on hand calculations using physical design rules and estimates of electron migration,” observes Wong. “Third-party packaging suppliers would help by telling us how hot a die might get when packaged based on their thermal dissipation experience, but it was just an educated guess, and it wasn’t detailed enough to guide design decisions.”

Looking for better thermal data, EnSilica began instrumenting its chip designs. Low-power temperature sensors embedded at points on a die give temperature readings. Two issues soon arise. Are the sensors placed in the right spots? And is the chip in the proper operating mode for taking valid measurements? Experience helps with sensor placement but setting up even a limited number of test conditions and sweeping the environmental chamber’s temperature takes time.

Predictions from thermal estimates lacked certainty and physical test and measurement setups for improved thermal characterization were slowing development by weeks.

Solution: Adding thermal simulation to the workflow

With the quality and efficiency of semiconductor design in mind, EnSilica’s workflow features world-class electronic design automation (EDA) tools, now with PathWave ADS Electro-Thermal Simulator added.

EnSilica RF EDA tool stack

Workflow Step	EDA Tools
Design Control	Cliosoft SOS, Subversion
Requirements Capture	Sparx Systems Enterprise Architect
System Design	The MathWorks MATLAB®, GNU Octave
Analog Environment	Cadence® Virtuoso® IC
RF/Analog Simulation	Cadence Spectre®, Keysight PathWave ADS , Siemens AFS™ Platform
Electro-Magnetic Simulation	3D EM simulation platform, Keysight PathWave RFPro
Electro-Thermal Simulation	Keysight PathWave ADS Electro-Thermal Simulator
Layout Extraction	Siemens Calibre® xRC
Physical Verification	Siemens Calibre 3DSTACK
PCB Design and Layout	Altium Designer®

Indeed, Keysight was already a trusted RF EDA tool supplier in the EnSilica workflow. Wong explains, “We were using a 3D EM solver for electromagnetic simulation but moved to Keysight RFPro because of its tighter integration with Cadence Virtuoso IC.” He also cites Keysight’s support for new tool introduction and a simple user interface as reasons they chose PathWave ADS and RFPro.

Despite the breadth of its EDA tool stack, EnSilica had not yet used a tool for thermal analysis. Keysight customer care teams pointed out Electro-Thermal Simulator integration in PathWave ADS. From layout in Cadence Virtuoso IC, a GDSII export enables electrothermal modeling of a design. More information, like stack files from electromagnetic (EM) simulation in RFPro, die stack and layout, chip package bumping and underfill details, and printed circuit board (PCB) build features, added realism to the model.

Material selections from the Keysight PathWave ADS Electro-Thermal Simulator library combined with information gleaned from other sources – including Google searches – supplied the final touches. “We worked very hard to match every aspect of our materials to realistic thermal parameters,” says Samuel Wu, Principal RFIC Design Engineer at EnSilica. “We used the Keysight libraries when appropriate. In some cases, we didn’t have exact fits for information from the foundry or our packaging provider, so we made adjustments, sometimes with the help of a Keysight application engineer.”

Results: Higher confidence in operating margins and reliability prediction

Many foundries offer automotive-certified processes operating at junction temperatures up to 150°C, including the bulk standard CMOS 40nm process EnSilica used for the Ka-band transceiver. An immediate benefit of electro-thermal simulation is a detailed visualization of the chip thermal profile showing temperature gradients, with EnSilica’s results for the Ka-band transceiver shown in Figure 2.

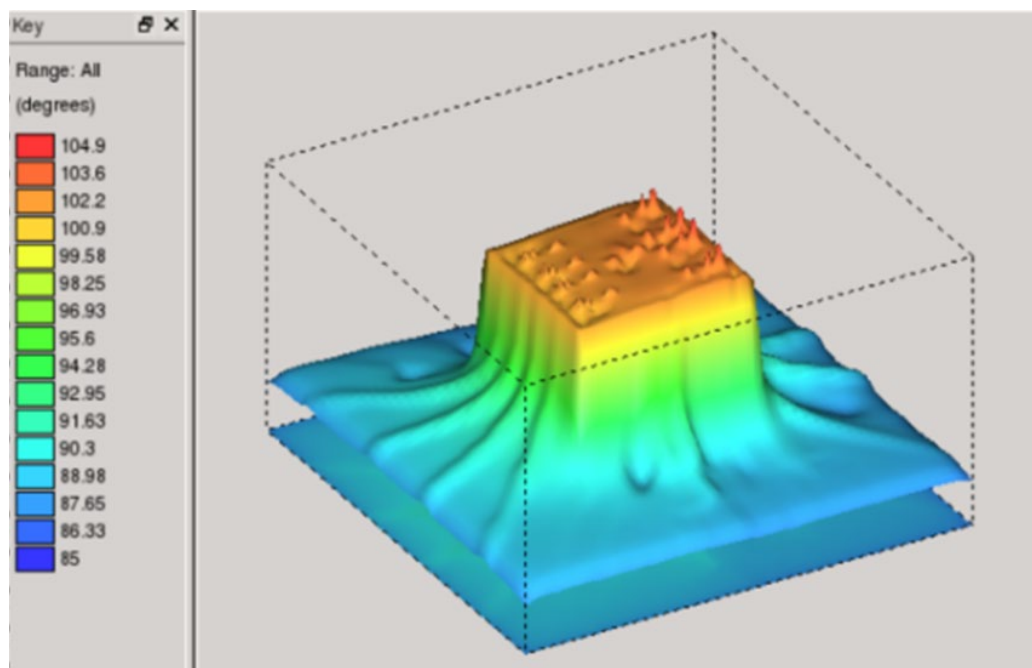


Figure 2. Hot spots revealed in an electro-thermal simulation of Ka-band transceiver with boundary heating effect

Customer inputs, including real-world effects, guided the electro-thermal simulation conditions:

- Ambient temperature is 85°C
- Switching on four Ka-band transceiver channels, at full duplex transmit and receive modes
- Power amplifier devices run at +10dBm output power, expecting a 20°C temperature rise
- An adjacent RFIC on the PCB creates boundary heating of 3°C on one edge

The real test of the simulation results is a comparison to measurements using the temperature sensors embedded in the chip. The electro-thermal simulation predicted a maximum 13°C rise in die temperature over ambient. Actual measurements on a test article under full-on conditions show a maximum 12.3°C rise, as seen in Figure 3.

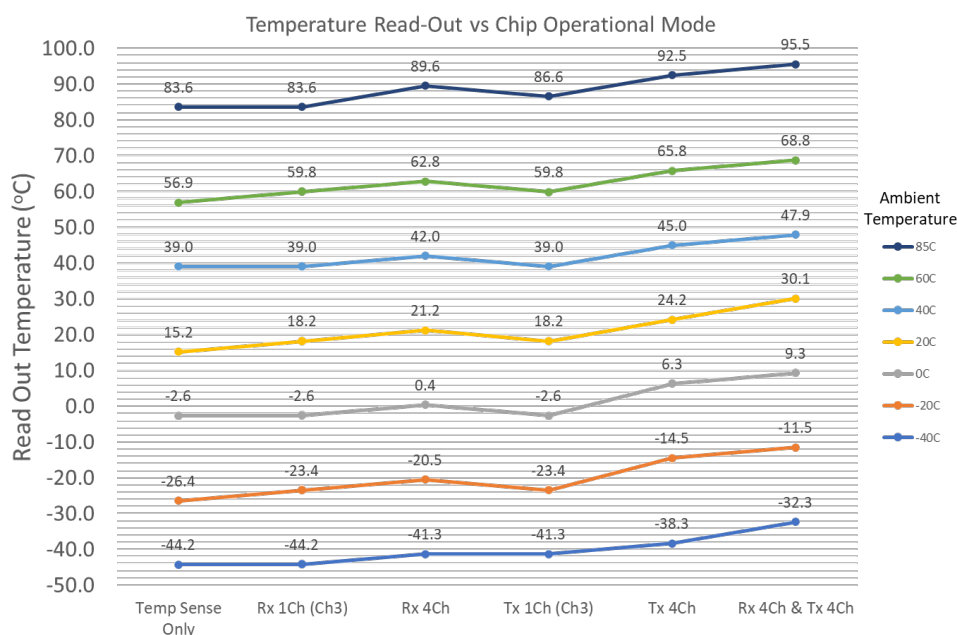


Figure 3. Physical measurements of die temperature fall within predicted results from electro-thermal simulation

Never-before-seen details also emerged. Dark spots on the top of the elevated temperature mesh in Figure 2 indicate V_{DD} and V_{SS} bumps acting as thermal pathways, cooling small areas. From that insight, chip layout changes and bumping further reduced operating temperatures in the final product.

With high-confidence temperature simulation data in hand, EnSilica then used Cadence RelXpert to simulate transistor stress and generate “aged” power amplifier (PA) device models for reliability simulation, using a junction temperature of 100°C for the required ten years of operation. The change in power output between the aged PA and the “fresh” PA was only -0.4dB, indicating little degradation.

“We have greater confidence in two ways,” says Wong. “The data points are bang on thermal simulations, and the reliability looks good, with a very benign PA power degradation over time. These were not givens before we started our virtual thermal analysis.”

“Now, we know we can drive the Ka-band transceiver a bit harder than its requirements in the customer’s system, and it’s safe to do that while still meeting the 10-year reliability goals.”

Alan Wong, Sr. VP of Engineering, EnSilica

Confidence in the simulation results means EnSilica can shift activity from intense physical measurements to virtual space, shortening the design cycle as experience accumulates. “Electro-thermal simulation is much faster than EM simulation, which drives the size of our server farm, so there’s a big return for a little time spent,” says Wu.

Looking ahead: More support for foundry and packaging data

PathWave ADS Electro-Thermal Simulator has become part of EnSilica’s standard workflow. Operating range margins are better understood, and customers have greater confidence. “Now, we know we can drive the Ka-band transceiver a bit harder than its requirements in the customer’s system, and it’s safe to do that while still meeting the 10-year reliability goals,” concludes Wong. New designs will see the same benefits. More foundry and packaging supplier support for electro-thermal models would reduce estimations and adjustments, with Keysight continuing to work on these relationships.

Learn more about EnSilica and its custom design services at:
www.ensilica.com

For more information on these Keysight RF EDA solutions, please visit:

[PathWave Advanced Design System \(ADS\)](#)

[PathWave RFPro](#)

[PathWave ADS Electro-Thermal Simulator](#)

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